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PbO Based MIS Nanostructure Device *C-V* and *I-V* Characteristics; Calculation Techniques, Comparisons

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Keywords

Barrier Hight
Ideality Factor
Lead Monoxide PbO
Series Resistance
Diode Parameter Extraction
Schottky Diode

Abstract

The electrical properties of an Al/PbO/p-Si nanostructure forming PbO based diode of MIS-type (metal-insulator semiconductor) diode have been investigated. This particular diode structure is relatively new and has limited documentation in the existing literature. The prepared heterostructure, whose capacitance and current-voltage (*C-V* and *I-V*) characteristics were measured at room temperature in dark conditions. Key parameters such as the ideality factor n, barrier height ϕ_b and series resistance R_s were calculated using multiple methods, including the Standard, Norde, Lien-So-Nicolet, and Cheung techniques. These parameters provided insight into the molecular dynamics influencing the electrical characteristics of the diode. The annealing process at 290°C for 20 minutes was found to have a significant impact on the electrical behaviour of the sample. This study highlights the potential of PbO-based diodes for use in high-performance nanostructure devices.

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1. INTRODUCTION

Silicon-based (Si) devices exhibit high sensitivity to both infrared (IR) and visible light. However, their performance in the ultraviolet (UV) range is significantly limited due to their bandgap energy, which is approximately 2.8 eV (Venkataraj et al., 2002). To enhance UV detection capabilities, metal-oxide-semiconductor (MOS) devices offer a more promising approach due to their wide bandgap. Consequently, Si-based MOS devices have emerged as viable candidates for high-efficiency UV photodetectors (Makhlouf et al., 2017).

Lead monoxide (PbO) has gained attention for its unique properties, such as high carrier mobility and strong absorption of x-rays and gamma rays (Simon et al., 2005; Coşkun & Cetin, 2023). These characteristics make PbO a versatile material suitable for applications ranging from optoelectronics to radiation shielding (El-Sayed Abdo et al., 2003; Harish et al., 2010; Pıçakçı & Yalçın, 2023). PbO can exist in two primary crystalline forms, tetragonal α-PbO (red) and orthorhombic β-PbO (yellow), with a transition temperature around 763 K. These phases differ in their electronic properties, which significantly influence their performance in devices like UV detectors and radiation sensors (Patel et al., 2015; Lee et al., 2017).

In this research, a PbO-based MOS structure was fabricated, and its *C-V* and *I-V* characteristics were analysed. The equivalent circuit model of the diode is represented in Figure 1. It includes a series resistance (R_s) and a parallel conductance (G_p), which are crucial for accurately modelling the device characteristics. In most cases, G_p is negligible. The Shockley diode equation governs the *I-V* behaviour of the diode:

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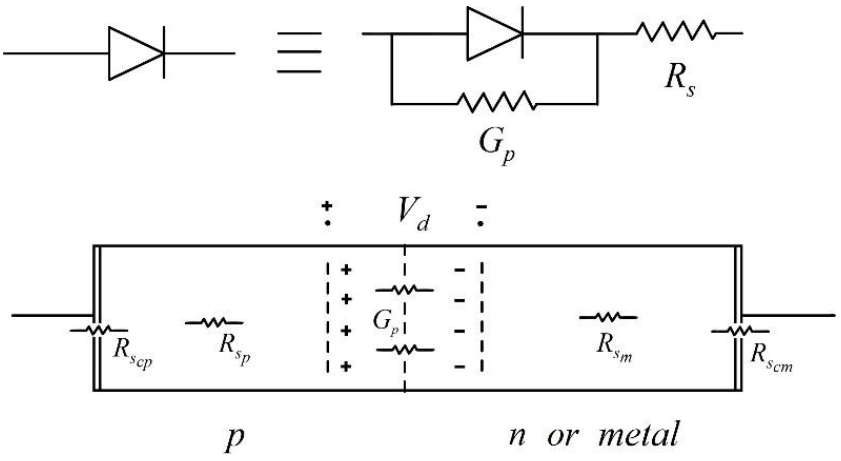

Figure 1. *Equivalent circuit of a diode*

$$I = I_s\left(e^{\frac{qV_d}{nkT}} - 1\right) \tag{1}$$

where I_s is the saturation current, q is the electronic charge, n is the ideality factor, k is the Boltzmann constant, and T is the absolute temperature. However, when considering the effect of the series resistance, the diode voltage (V_d) can be expressed as $V_d = V - IR_s$. Thus, the current equation is modified to include both series resistance and parallel conductance (Aubry & Meyer, 1994):

$$I = I_s\left(e^{\frac{q.(V-IR_s)}{nkT}} - 1\right) + G_p(V - IR_s) \tag{2}$$

This information is enough to access the Schottky diode in a circuit as an ohmic element. But it is convenient to calculate series resistor, barrier height and ideality factor, interface states in order to determine design parameters from both *C-V* and *I-V* measurements. For this purpose, several methods in the literature have been suggested. Those are Standard, Cheung, Norde, Lien-So-Nicolet Methods. Some other methods are also reported those are not employed in this study (Mahi et al., 2019; Li et al., 2020; Bashahu et al., 2022).

Fabrication and measurement of a new Schottky diode type is important for future material and sensor improvements as this work contributes. PbO based MIS structure diode investigation is very rare in the literature.

2. MATERIAL AND METHOD

PbO devices are printed on *p*-type Si (100) wafer. Its resistivity is maximum 10 Ω.cm (low resistivity with minimum value of 1, as mentioned by manufacturer) and has a thickness of 280 μm. RCA1 (Radio Corporation of America, cleaning technique 1: A laboratory invented chemical cleaning method) cleaning procedure is applied to the Si wafer (Selçuk et al., 2014; Aras et al., 2015; Kaymak et al., 2018).

The unpolished side of the wafer is coated with 99.999% Al by evaporation under a pressure of 3×10^{-6} Torr. The thickness of the coating is 124 nm. An evaporation coating system is filled with nitrogen and then vacuumed to 1×10^{-6} Torr. In this oxygen free environment, the sample is heated maximally up to 500°C, as the Al side up. This causes Al molecules penetrate Si structure. Then the surface is coated finally with Al of thickness 124 nm. A good ohmic contact is obtained.

The polished surface of the wafer is then coated with β-PbO by evaporation in a vacuum of 3×10^{-6} Torr. The thickness of the PbO coating, measured using an Edwards FTM6, is 15 nm. The sample is then annealed at 290°C during 20 minutes in the air.

Using a mask and evaporation, 128 nm deep Al disks of 1.3 mm diameter are printed above PbO coating. Figure 2 depicts the schematic of the heterostructure device. The measurements are performed at room temperature and in darkness, since the electrical behavior of the sample is easily affected by light. The *C-V* and *I-V* measurements are performed using an Agilent 4294A Impedance Analyzer and a Keithley 2400 Source Meter, respectively.

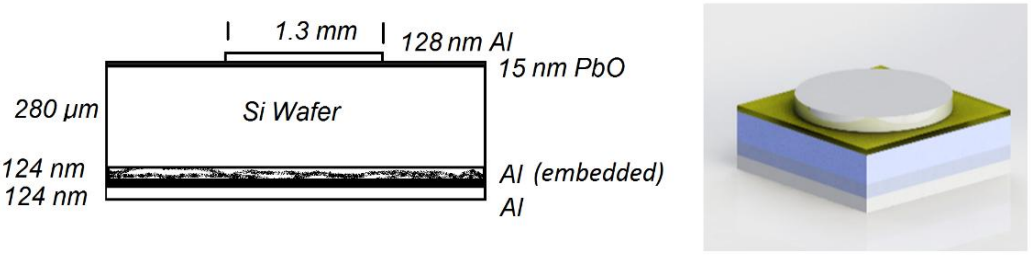

Figure 2. *Heterostructure Al/PbO/p-Si diode structure representation*

3. RESULTS AND DISCUSSION

3.1. *I-V* Measurement Analysis

The experimental results give the *I-V* and ln(*I*)-*V* curves as in Figure 3.

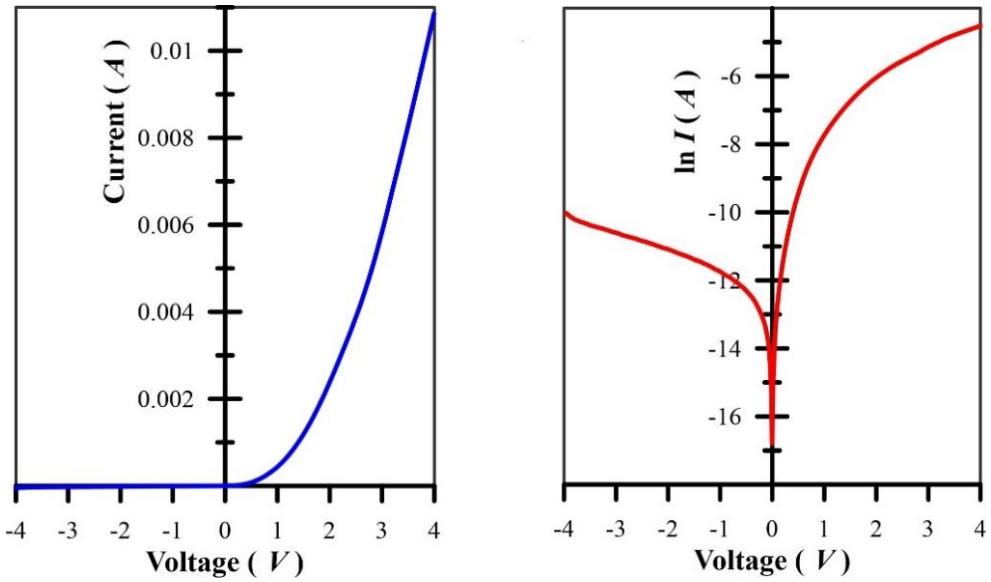

Figure 3. *Experimental curves of I-V and ln(I)-V.*

3.1.1. Standard Method

Assuming the parallel conductance G_p in the model given in Figure 1 is very low and neglecting the last term in Equation 2 results in

$$I = I_s\left(e^{\frac{q(V-IR_s)}{nkT}} - 1\right) \tag{3}$$

A voltage range (V_1, V_2) is chosen from *I-V* graphics. This range is chosen so that the variation of ln *I-V* is linear (Figure 3). Note that the measured voltage *V* is different from the junction voltage V_d, that is $V_d = V\text{-}I\,R_s$. So, the lower limit of the range (that is V_1) must satisfy the condition $V_{d1} = V_1\text{-}I_1R_s >> nkT/q$. For the certain values of series resistance R_s a computer program is employed to correct the experimental curve ln *I* vs *V* to reach ln *I* vs V_d ($=V\text{-}R_s\,J$) considering a least square fit.

3.1.2. Cheung Method

To find the values *n* and *R*, team Cheung (1986) extracted the voltage from the equation and took its derivative with respect to ln *I*. First, let's write the current I_s in terms of barrier height.

$$I_s = A_{eff}A^{**}T^2 e^{-\frac{q\phi_b}{kT}} \tag{4}$$

where A_{eff} stands for the effective area of the junction, which is approximately $0.65^2\pi$ cm^2, and A^{**} is the Richardson constant, which is 32 /cm^2.K^2. Then an approximation is made. That is, when $V_d = V\text{-}IR_s > 3nkT/q$, the term -1 in Equation 3 can be neglected. After taking the voltage out

$$V = R_s I + n\phi_b + \frac{nkT}{q}\ln\left(\frac{I}{A_{eff}A^{**}T^2}\right) \tag{5}$$

$$\frac{dV}{d\ln(I)} = IR_s + \frac{nkT}{q} \tag{6}$$

So, if the graph $dV/d\ln(I)$ vs I is sketched, then it will be a line of slope R_s and an interception value on the *y*-axis of nkT/q. Thus, *n* and R_s can be calculated in this manner. After determining *n* and R_s, we then return to the Equation 5 to find ϕ_b. If the voltage and the term with natural logarithm of *I* are put together, the remaining terms define a line at the other side of the equation. Then, the slope of this line is proportional to R_s and the *y* axis intercept can be used to calculate the barrier height ϕ_b.

$$V - \frac{nkT}{q}\ln\left(\frac{I}{A_{eff}A^{**}T^2}\right) = R_s I + n\phi_b \tag{7}$$

which is defined as $H(I)$. The graphics, obtained from Cheung method, are given in Figure 4. The correlation factor R^2 is also calculated as above 0.95.

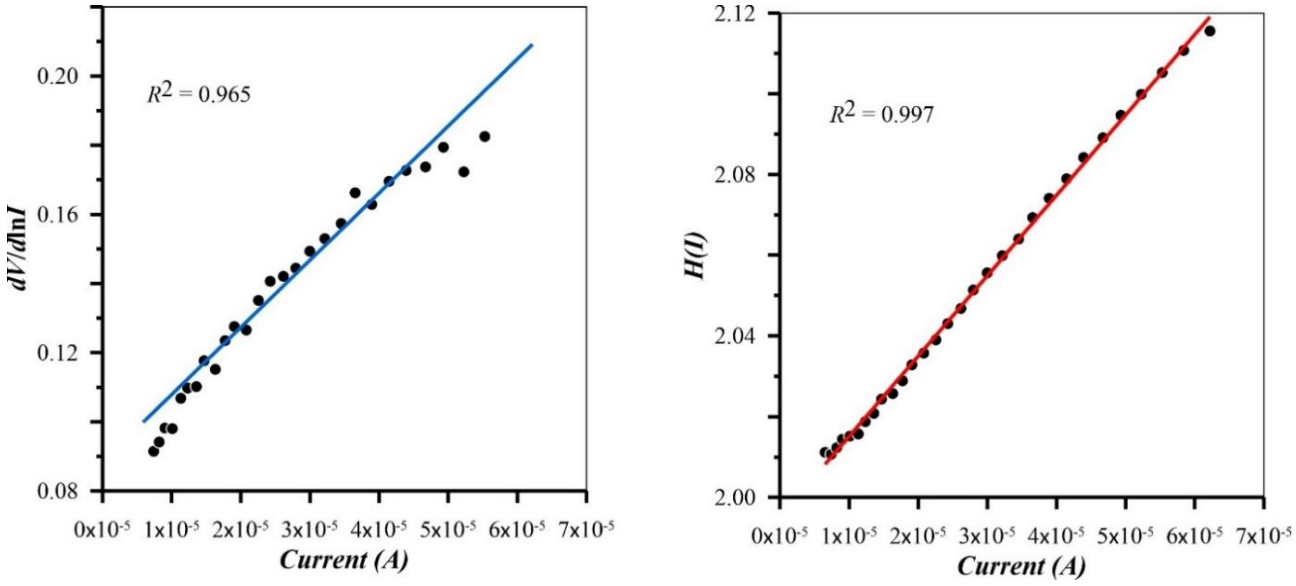

Figure 4. *dV/dln I and H(I) versus I curves of Cheung Method.*

3.1.3. Norde Method

Norde (1979) suggested a method for high series resistance values where the ideality factor n is 1. He rearranged Equation 3 such that the plot of a function $F(V)$ of voltage has some linear part when V is sufficiently high. Then the slope of this line gives the series resistance, where the interception on the y axis tells about the barrier height. $F(V)$ function graphics are shown in Figure 5.

$$F(V) = \frac{V}{2} - \frac{kT}{q}\ln\left(\frac{I}{AA^{**}T^2}\right) \tag{8}$$

Assuming $V_d >> 3kT/q$ (since $e^3 > 20$, -1 can be neglected),

$$F(V) = \phi_b + IR_s - \frac{V}{2} \tag{9}$$

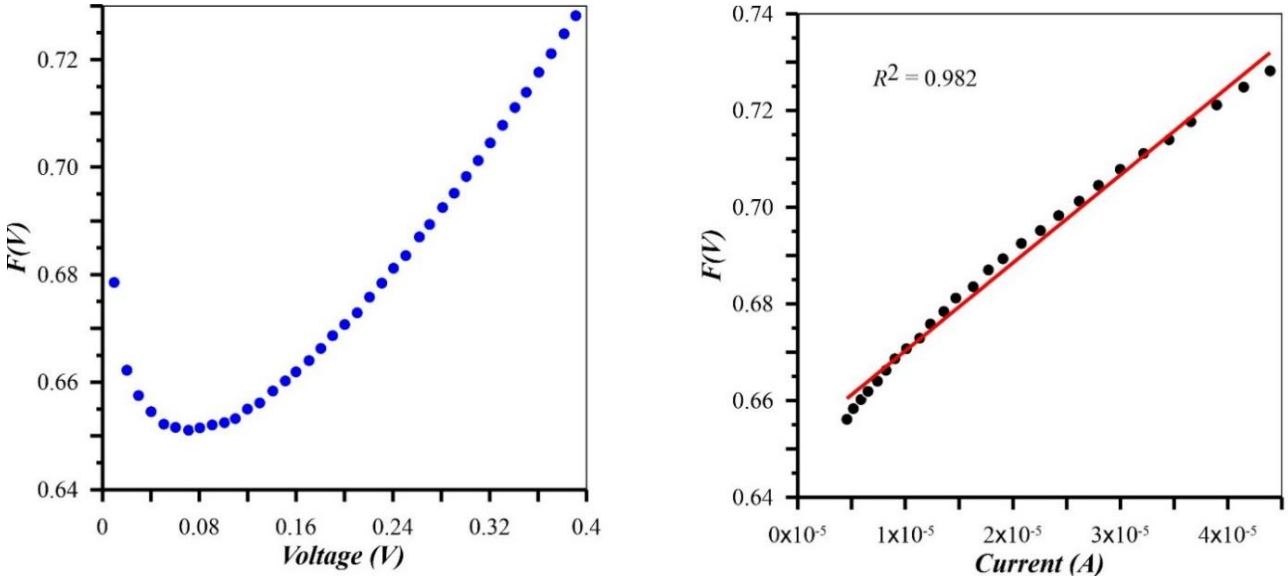

Figure 5. *F(V) curves of Norde Method*

3.1.4. Lien-So-Nicolet Method

Lien et al. (1984) suggested to consider more than one plot of the function below for different gamma values,

$$G_\gamma(V,I) = \frac{V}{\gamma} - \frac{kT}{q}\ln\frac{I}{A^{**}AT^2} \tag{10}$$

where γ is an arbitrary parameter which is greater than n. When $\gamma = 2$, then $G_2(V,I) = F(V,I)$, so it is the Norde plot. $G_\gamma(V,I)$ vs I graphics have a minimum at $I_{0\gamma} = (kT/qR_s)(\gamma\text{-}n)$. If the graphics of $I_{0\gamma}$ - γ is drawn, this will be a line with slope $m=kT/qR_s$ and its interception with the γ axis (γ_0) result in

$$R_s = \frac{kT}{qm}\ ,\ \ n = \gamma_0 \tag{11}$$

Using more than one gamma value leads using more than one data value. This may result in more accurate results and allows to use linear regression (Figure 6).

The electrical parameters of the PbO-based diode were assessed using four distinct calculation methodologies. The outcomes are presented in Table 1.

Both graphics of methods and Table 1 show that the Standard and Cheung methods yield higher n values (2.92 and 3.18), indicating significant deviation from ideal behaviour. This may be due to interface states, high recombination rates, or defects at the PbO/semiconductor interface. The Lien-So-Nicolet method shows a slightly lower n value (2.64), but it still suggests non-ideal characteristics, too. The Norde method, with its assumption of n=1, may not accurately reflect the diode's actual behaviour. As a result, this assumption may lead to inconsistencies in barrier height and series resistance calculations compared to other methods, especially in PbO/semiconductor structures with high ideality factors.

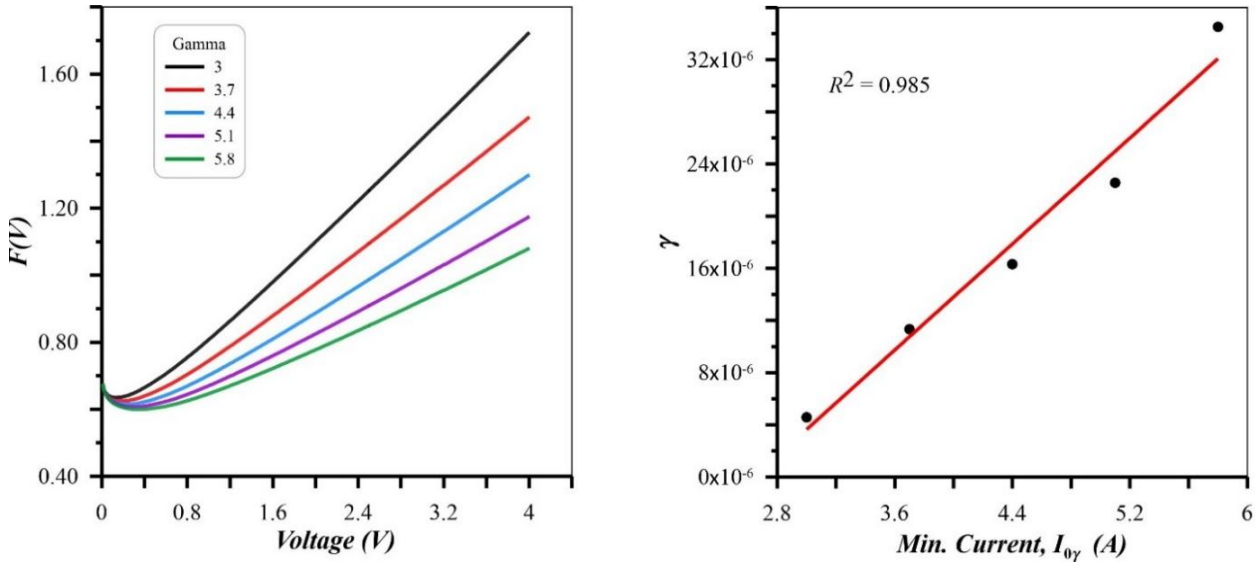

Figure 6. *F(V) and γ curves of Lien-So-Nicolet Method*

Table 1. *Calculation methods and results.*

Method	n	ϕ_b (eV)	R_s (Ohm)
Standard	2.92	0.64	-
Cheung	3.18	0.63	2097-1962
Norde	1 (assumed)	0.78	1580
Lien-So-Nicolet	2.64	-	2546

3.1.5. Interface States from *I-V* Characteristics

Card and Rhoderick (1971) predicted that MIS diodes with interface states D_{it}^{IV} would have an ideality factor n greater than unity that varies with applied potential.

$$n(V) = 1 + \frac{d_{ox}}{\varepsilon_i \varepsilon_0}\left(\frac{\varepsilon_s}{W_D} + qD_{it}^{IV}(V)\right) \tag{12}$$

By plotting the reciprocal of capacitance squared ($1/C^2$) against voltage, obtained from C-V measurements, the width of the depletion region can be determined. By analysing the forward-bias I-V characteristics of MIS diodes, it is possible to extract D_{it}^{IV}, which is in thermodynamic equilibrium with the semiconductor. Additionally, if the oxide layer thickness d_{ox} ($= \varepsilon_i \varepsilon_0 A/C_{ox}$) is unknown, it can be revealed from the accumulation region of the C-V plot (oxide capacitance C_{ox}). The effective barrier height ϕ_e is modulated by the applied bias owing to interfacial insulator layer and interface states at the semiconductor interface. This dependence of ϕ_e is incorporated into the ideality factor n.

$$\phi_e = \phi_b + \left(1 - \frac{1}{n(V)}\right)V \tag{13}$$

The energy level of the interface states, denoted as E_{ss}, is referenced against the valence band maximum in p-type semiconductors, indicating their position within the band structure and is given by

$$E_{ss} - E_v = q(\phi_e - V) \tag{14}$$

The extracted values from diode *I-V* are shown in Table 2. The values are chosen for calculation as the oxide thickness of 15 nm, dielectric constant of the oxide layer of 10.1, and the depletion layer thickness of 2196.2 Angstroms at 1 MHz.

As seen in Table 2 and Figure 7, the E_{ss}-E_v, D_{it}^{IV} values are in the range 0.607 to 0.697 eV and 5.648×10^{12} to 1.969×10^{13} /eV.cm^2, respectively. There is an increase in D_{it}^{IV} up to top of the valence band. High D_{it}^{IV} values typically indicate the presence of high density of defects at the interface, leading to a deviation from ideal behaviour. It shows that the trap levels are close to the conduction band which suggests that interface defects and traps significantly hinder the transition of charge carriers. The relatively stable range of E_{ss}-E_v values indicates that the increase in D_{it}^{IV} might correlate with an increased impact on the energy band, reflecting a more substantial effect on electronic properties. The high interface state density is likely a result of the growth of the thin orthorhombic oxide layer, as suggested by the observed trends in our measurements. The obtained results show that the investigated structure has high D_{it}^{IV} levels (order of 10^{13}/eV.cm^2), consistent with the findings in the literature.

Table 2. *Interface states energy distribution of Al/PbO/p-Si from I-V characteristics*

V (V)	**$n(V)$**	**ϕ_e (eV)**	**E_{ss} - E_v (eV)**	**D_{it} ($\times10^{13}$/eV.cm^2)**
0.075	2.596	0.771	0.696	0.565
0.109	2.987	0.798	0.688	0.711
0.161	3.580	0.841	0.680	0.932
0.211	4.078	0.884	0.673	1.117
0.260	4.469	0.927	0.667	1.263
0.311	4.749	0.970	0.660	1.367
0.362	4.935	1.013	0.652	1.436
0.410	5.059	1.054	0.644	1.483
0.460	5.164	1.096	0.636	1.522
0.511	5.276	1.139	0.628	1.564
0.560	5.412	1.182	0.621	1.614
0.611	5.589	1.227	0.616	1.680
0.661	5.812	1.272	0.611	1.763
0.711	6.093	1.319	0.608	1.868
0.751	6.364	1.358	0.607	1.969

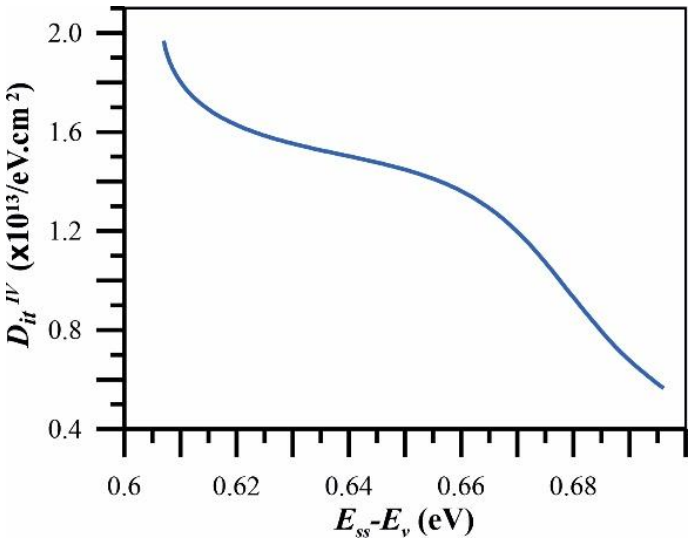

Figure 7. *Interface states versus E_{ss}-E_F plot of diode structure from I-V measurement*

3.2. *C-V* measurement Analysis

The capacitance and conductance (*C-V* and *G-V*) measurements have been performed, and the obtained $1/C^2$-*V* characteristics are illustrated in Figure 8 and 9. From *C–V* measurement, the value of barrier height ϕ_b (*C–V*) and other parameters, at frequency 1MHz, were calculated. Using $1/C^2$-*V* plot as seen in Figure 9, built-in voltage, (V_0) can be determined by finding intercept of axis of straight line with the *x*-axis where $C^{-2} = 0$. Additionally, the carrier doping density (N_A) can be revealed from slope of the line.

$$V_0 = V_D + \frac{kT}{q} \tag{15}$$

where V_D is the diffusion potential.

$$N_A = -\frac{2}{q\varepsilon_s A^2}\left(\frac{d(1/C^2)}{dV}\right)^{-1} \tag{16}$$

where *A* is the rectifying contact surface area and ε_s ($11.9\varepsilon_0$ (Sze & Ng, 2006) for Si) is the permittivity of the semiconductor. The ϕ_b (*C–V*) can be calculated from Equation 17.

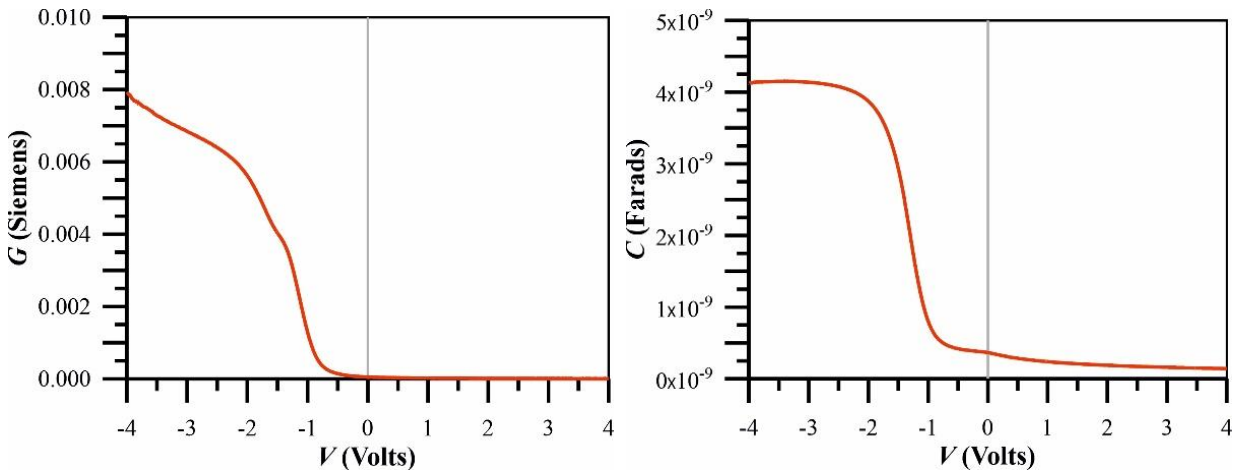

Figure 8. *C-V and G-V measurement of Al/PbO/p-Si MIS structure at 1MHz.*

$$\phi_b(C-V) = V_0 + E_F + \frac{kT}{q} - \Delta\phi_b \tag{17}$$

where $\Delta\phi_b = \sqrt{qE_m/(4\pi\varepsilon_s\varepsilon_0)}$ is called image force lowering and E_F is the Fermi energy level. Maximum electric field E_m at contact interface is given by

$$E_m = \sqrt{\frac{2qN_AV_D}{\varepsilon_s\varepsilon_0}} \tag{18}$$

E_F can be calculated by using relation

$$E_F = \frac{kT}{q}\ln\left(\frac{N_V}{N_A}\right) \tag{19}$$

where $N_V = 4.82 \times 10^{15}(T \times m_h^*/\, m_0)^{3/2}$, in the valance band of semiconductor, is the effective density of states. Effective mass of hole m_h^*, in terms of the rest mass of the electron m_0, is $m_h^* = 0.16m_0$ (Sze & Ng, 2006). The expression provides an estimate of the spatial region where charge carriers are depleted, the depletion width, can be calculated using $W_D = \sqrt{2\varepsilon_s\varepsilon_0V_D/(qN_A)}$ in the semiconductor. Based on the *C-V* measurement of structure, a barrier height (ϕ_b) was determined to be 0.835 eV (correlation factor of 0.999) with an image force lowering ($\Delta\phi_b$) of 0.027 eV, the depletion layer width (W_D) of 2196.2 Å, a carrier doping density (N_A) of 1.83×10^{16} cm^{-3} and a Fermi energy level (E_F) of 0.159 eV. The values of N_A and E_F suggest moderate carrier concentration and energy level alignment, while $\Delta\phi_b$ indicates the minor influence of image force lowering on the barrier height at the metal-semiconductor interface.

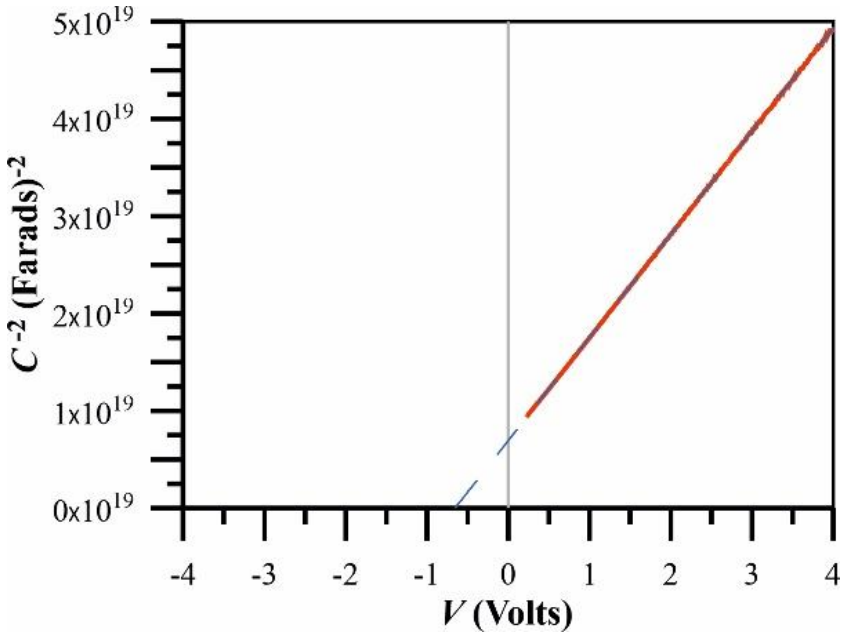

Figure 9. *C $^{-2}$-V plot of Al/PbO/p-Si MIS structure*

Additionally, series resistance (R_s) was extracted from the high-frequency *C* and *G* measurements using the Nicollian and Brews method (Nicollian & Brews, 1982). The series resistance can be calculated by considering the conductance and capacitance values at a given voltage in the accumulation region where it is strong, using the following formula.

$$R_s = \frac{G_{acc}}{G_{acc}^2 + \omega^2 C_{acc}^2} \tag{20}$$

where ω is the angular frequency. The change of the R_s of the Al/PbO/p-Si MIS structure is illustrated in Figure 10, with a peak resistance of 941.7 ohms.

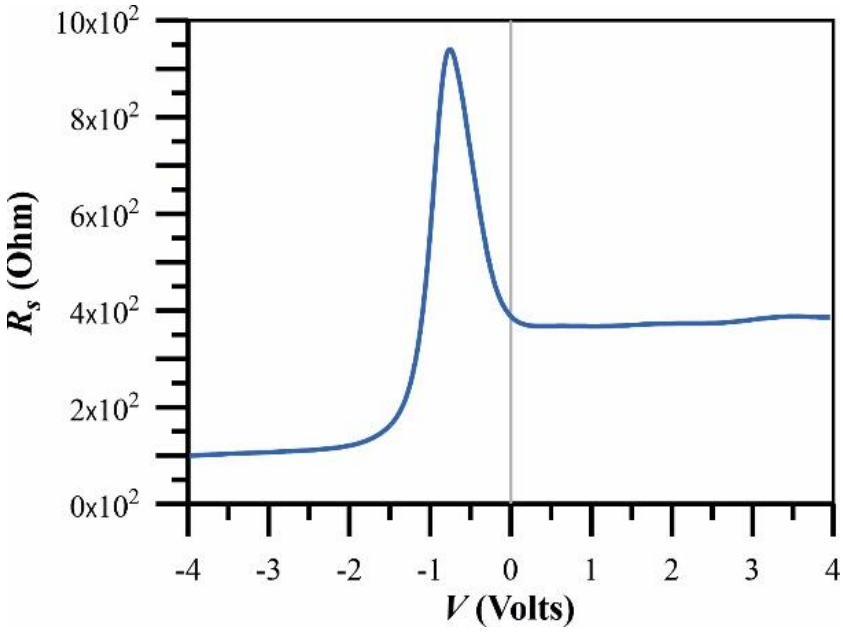

Figure 10. *Plot of series resistance of MIS structure at 1MHz.*

The interface states from capacitance measurement (D_{it}^{CV}) can evaluated by Hill-Coleman method (Hill & Coleman, 1980).

$$D_{it}^{CV} = \frac{2(G_{c,max}/\omega)}{qA\left[\left(G_{c,max}/\omega C_{ox}\right)^2 + (1 - C_c/C_{ox})^2\right]} \tag{21}$$

where C_c and $G_{c,max}$ are corrected capacitance and corrected maximum conductance, respectively. Corrected capacitance and conductance in terms of measured values can be derived from equation 22.

$$C_c = \frac{(G_m^2 + \omega^2 C_m^2)C_m}{G_m - (G_m^2 + \omega^2 C_m^2)R_s + \omega^2 C_m^2},$$
$$G_c = \frac{(G_m^2 + \omega^2 C_m^2)[G_m - (G_m^2 + \omega^2 C_m^2)R_s]}{G_m - (G_m^2 + \omega^2 C_m^2)R_s + \omega^2 C_m^2} \tag{22}$$

The calculated active and fast responding trap state density D_{it}^{CV} is 0.572×10^{13} /eV.cm^2 at 1MHz frequency. In PbO-based systems, high defect densities and oxygen vacancies tend to lead to D_{it}^{CV} values reaching the order of 10^{13}/eV.cm^2. According to theoretical analyses of MIS structures, this level indicates a high interface trap density, which can significantly affect device performance. This value implies increased recombination and reduced carrier mobility, resulting in noise and conductivity reduction, particularly in high-frequency applications.

Both *I-V* and *C-V* analyses revealed high interface state densities on the order of 10^{13} /eV.cm^2. They show consistent results, indicating a high defect density at the PbO/Si interface. This consistency between the two methods enhances the reliability of the analysis and underscores the need for improvements in the interface quality to reduce these defects. Optimizing the growth and annealing processes of the PbO layer may help reduce these defects and improve the electronic properties of the diode. Addressing these issues is essential for enhancing the performance of PbO-based MIS devices in high-frequency and sensor applications.

4. CONCLUSION

This study successfully demonstrated the fabrication and characterization of a PbO-based MIS diode on a p-type Si substrate, providing insights into its electrical properties through comprehensive different *I-V* and *C-V* analyses. The results indicate significant deviations from ideal diode behaviour, primarily attributed to high interface state densities and structural imperfections at the PbO/Si interface. The extracted parameters, including ideality factor, barrier height, and series resistance, revealed considerable variations among different evaluation methods, with barrier heights ranging from 0.63 to 0.78 eV and interface state densities on the order of 10^{13} /eV.cm^2.

The analysis also highlighted the influence of series resistance, which was found to vary depending on the evaluation method, ranging from 1580 to 2546 Ohm. High series resistance values can lead to increased power loss, voltage drops, and deviations in the *I-V* characteristics, particularly at higher forward bias conditions. By reducing the series resistance through process optimization could enhance the overall performance of the diode.

The consistency observed between the *I-V* and *C-V* analyses confirms the high defect density, emphasizing the critical role of interface states in influencing the electronic properties of the diode. These findings underscore the importance of optimizing the growth and annealing processes of the PbO layer to reduce defects and improve device performance, particularly in high-frequency and sensor applications. Future studies should focus on refining the fabrication techniques and exploring alternative passivation methods to achieve lower defect densities and enhanced material quality.

CONFLICT OF INTEREST

The author declares no conflict of interest.

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