Vol 7, Number 2, 2017
European Journal of Technique
EJT

COMPARATIVE STUDY OF 0.18MM LINEARIZED CMOS LOW NOISE AMPLIFIER

Esra İNCE*, Mustafa TÜRK

Department of Electrical and Electronics Engineering, University of Firat, Elazığ, Turkey

* Corresponding author; esraozdemir@firat.edu.tr

This paper presents a comparative study of linearization techniques for Complementary Metal Oxide Semiconductor low noise amplifier. The study is performed previously reported three different techniques; modified derivative superposition, post distortion and noise/distortion cancellation. To perform the design, cascade amplifier topology and 0.18µm Complementary Metal Oxide Semiconductor process parameters is used. These performance are studied in the frequency range of 1 GHz to 5 GHz through simulation. Simulations are performed in Applied Wave Research design environments program.The results are compared with each other and previously reported publication in ways of Input third order intercept point, Input second order intercept point, gain, input return loss, noise figure and DC power.

Keywords— *Complementary Metal Oxide Semiconductor,Low noise amplifier, linearization techniques.*

Introduction

The low noise amplifier, as its name implies, is the first block after the loop in the receiver chain that amplifies weak signals without adding noise. There is less noise than other amplifiers. As is known from the Friis expression, the total system is the first layer of the dominant floor system, which determines the sensitivity of reception because of the noises [1].

Therefore, when adding a small amount of noise to a low noise amplifying system, high gain is required, low power consumption and high sensitivity must be maintained. At the same time, it should suppress distortion for good linearity and have a fixed 50Ω input and output impedance value for maximum power transmission. Providing high linearity is achieved by improving the third-order intersection point (IIP3) of the amplifier. However, in order to achieve all these desired properties, the linearization techniques must be simple and should not adversely affect the noise and the gain at the same time [2].

In this paper, low-noise amplifier design was implemented using three methods: derivative superposition, noise / distortion cancellation, and post distortion. In order to obtain the simulation results, the appropriate low-noise amplifier topology was chosen in the first step. By applying each technique to the selected topology, desired low noise amplifiers were created. The circuits were optimized and the appropriate values of the circuit elements were selected. Later, in order to provide impedance matching in the circuits, appropriate impedance circuits were established and the final state of the circuits was obtained and the analysis results were obtained. 0.18um CMOS (Complementary Metal Oxide Semiconductor) parameters are used in the operation. Power gains (S21), input impedance matching (S11) and noise factors were found with the help of the s parameters of each of the techniques. IIP3 (Input third order intercept point) performance was measured using a dual tone test simulation.

As for the organization of the paper, Section 2 discusses the architecture of the linearization techniques and linearized LNA's (low noise amplifier). Section 3 show the simulation result and findings. In section 4, the results of the simulation results are compared with previous studies and with each other in terms of linearity, noise, impedance matching and gain.

Design Concept

LNA Architecture And Topology

Linearization Techniques and Circuit Designs

The improved derivative superposition technique is seen as a special case of the feed forward technique. With this technique, an amplifier design can be realized in which the third order interference is very low. It is a technique based on the working of the transistors in the circuit in different regions. The reason why this technique is called the "derivative superposition" is to add the third derivative (g3) of the drain current of the main and auxiliary transistor to destroy the distortion. Figure 1(a) shows the circuit connection for the MDS (modified derivative superposition) technique. Where M_a is the main transistor and M_b is the auxiliary transistor [5].

As shown in Figure 1(b), similar to the derivative superposition technique, the post distortion technique (PD) utilizes the nonlinearity of the auxiliary transistor to remove the nonlinearity of the main element, but this technique has been developed from two aspects:

1) The auxiliary transistor is connected to the output of the main element instead of being directly connected to the input to minimize the effect of input matching.

2) The operation of all transistors in saturation provides better linearity [6].

Noise / distortion cancellation, CG (MA) and CS (MB) parallel transistors are shown in Figure 1c. This circuit is realized by the supply voltage in the "IN" node. The nonlinearity of MA can be modeled as a source of current between drainage and source controlled by Vgs and Vds. Thus, the thermal noise and distortion of both channels flowing through the CG and CS paths of the MA are removed from the output when the signal is added. Noise / distortion cancellation requires Vx = Vy equality [7].

$$g_{1,MA}R_A = g_{1,MB}R_B\ (diferantial\ output) \quad (2)$$

$$g_{1,MB1}R_S = g_{1,MB1}R_A\ (single\ ended\ output) \quad (3)$$

The cascaded amplifiers provide high power gain, good noise performance, low consumption and high reverse isolation. But, the stacking of transistors in this LNA limits the available voltage hedroom. The limitation can be overcome by use of folded cascode topology.

The proposed cascade amplifier and the improved derivative superposition circuit, shown in Figure 2, are conveniently connected to form a low noise amplifying circuit.The working logic of the improved derivative superposition is to operate the transistors in different regions.Accordingly, while the main transistor is operated in the saturation region, the auxiliary transistor is biased in the weaker inversion region.The LC tank is used to set the frequency range that the operation is running.

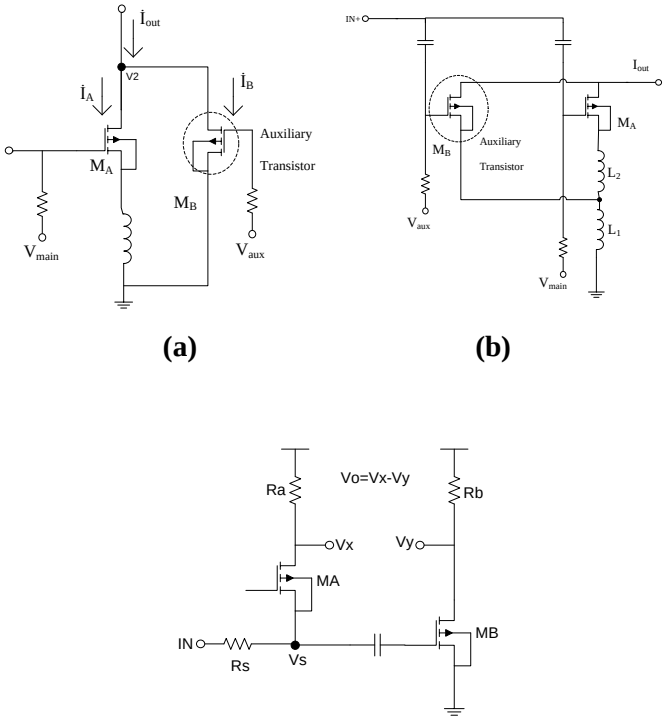


Figure 1. Circuit implementation of methods a) MDS [5] b) Post Distortion [6] c) Noise/Distortion Cancellation [7]

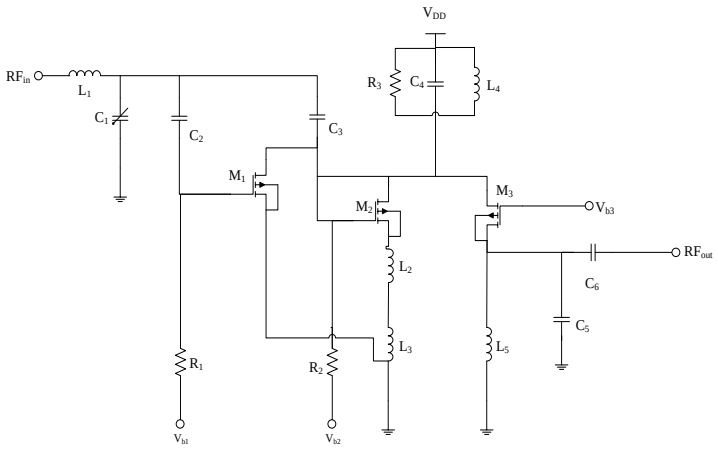


Figure 2. Linearized LNA with Modified Derivative Superposition

In post distortion method, similar to the derivative superposition method, the non-linearity of the auxiliary transistor is utilized in order to eliminate the nonlinearity of the element. To minimize the effect of input matching, the auxiliary transistor is connected directly to the output of the main element instead of being connected to the input. In addition, all of the transistors are operated in saturate mode to provide better linearity. The circuit is supplied with 0.8V voltage. The circuit diagram of the post distortion method is shown in Figure 3.

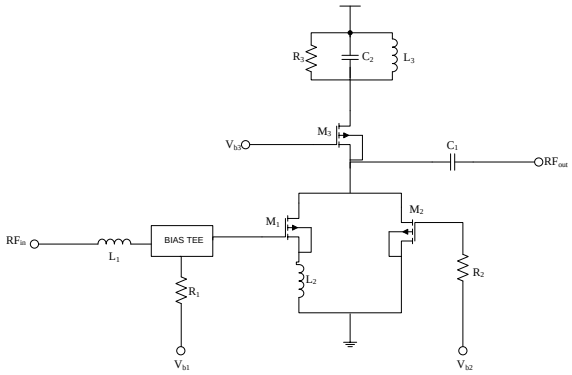


Figure 3. Linearized LNA with Post Distortion

In the noise/distortion cancellation technique, cascade low noise amplifying topology is used as in the post distortion technique. After setting the desired low noise amplifying circuit with the selected topology, the circuit element values were selected by optimization. In Figure 4, the circuit diagram of the noise cancellation circuit is given.

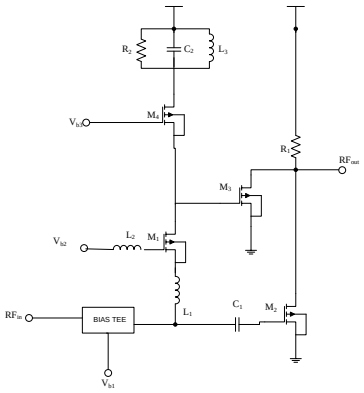
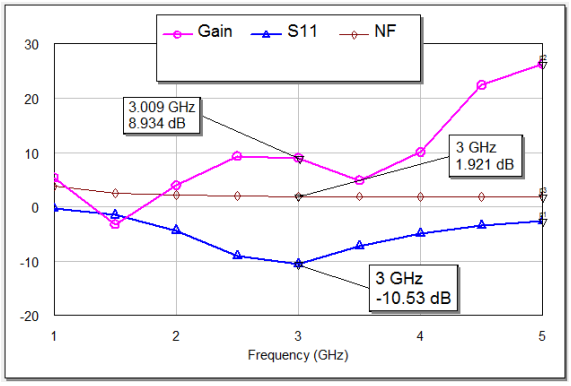


Figure 4. Linearized LNA with Noise/Distortion Cancellation

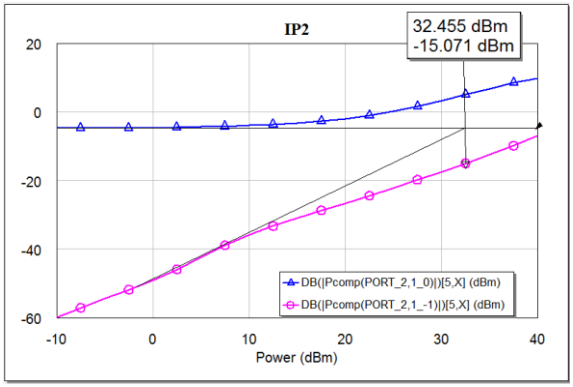
Measurement Results

The implementation of this method has been carried out at specific stages. First, the desired low-noise amplifier topology is selected. Due to its advantages such as high gain, good noise performance and low power consumption, cascade low noise amplifier topology is used. It is known that the traditional derivative superposition worsens the decay from the second level while improving the third decay. Because of this disadvantage, the modified derivative superposition method which improves the IIP3 value without damaging the IIP2 (Input second order intercept point) value is preferred. This method also minimizes the feedback from the source to the door. For this reason, after the appropriate topology has been determined, the modified superposition method is applied to the circuit and a new low-noise amplifier circuit is created.

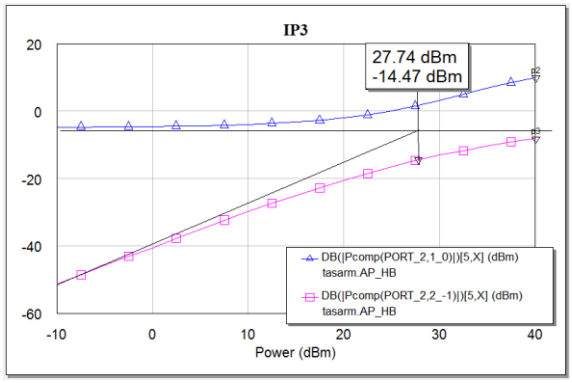
In Figure 5a, the gain, S11 and noise curves of the MDS technique are given. According to this, it is seen that the gain value is 8,934 dB, S11 value is -10,53 dB and the noise factor is 1,921 dB. The IIP2 curve is shown in Figure 5b and the IIP3 curve is shown in Figure 5c. These graphs show the linearity of the system. According to these graphs, IIP2 value is -15,071 dBm and IIP3 value is -14,47 dBm.Numerical results.



(a)



(b)

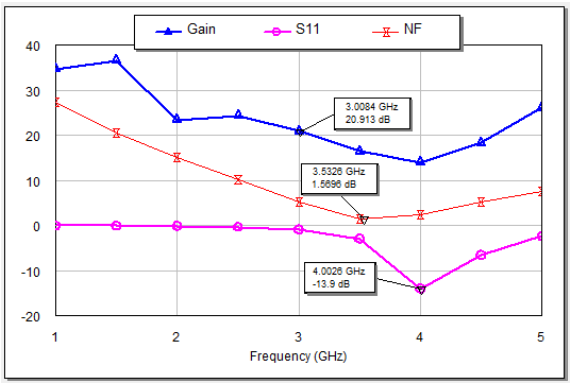


(c)

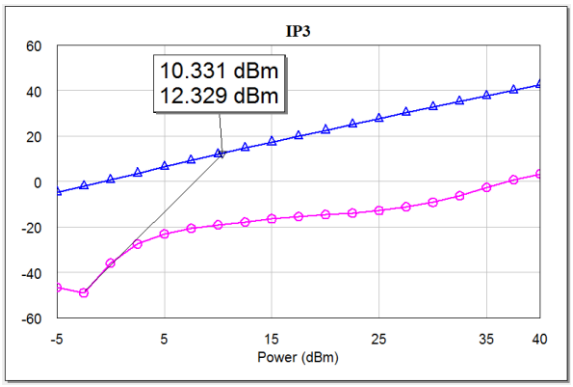
Figure 5. Simulation Results Of MDS a) Gain, S11, NF b) IIP2 c) IIP3

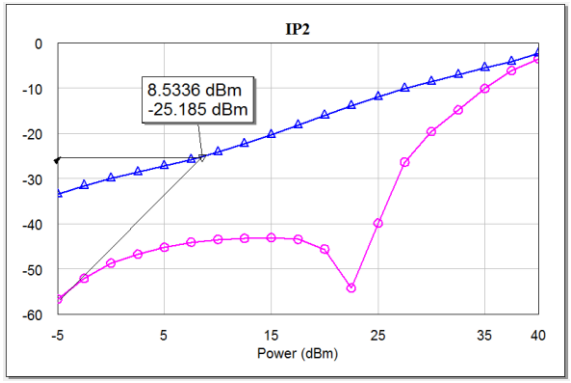
The results of the analysis of the low noise amplifier circuit generated by the post distortion technique are given. When we look at these results in general, it is seen that the second and third degree intercept values are in average values. Accordingly, the IIP2 value did not damage the IIP2 value while recovering. It has been seen that the circuit is added to the noisy minimum levels and high gain value is obtained.

In figure 6(a), curves of gain, S11 and noise values of the linearized LNA by the post distortion method are given. For gain 3 GHz frequency and for S11 and noise factor minimum points on the curve are selected. According to this results, it is seen that the gain value is 20,913 dB, the noise factor is 1,569 dB and S11 value is -13,9 dB. Figures 6b and 6c show the IIP2 and IIP3 values of the amplifier circuit.



(a)





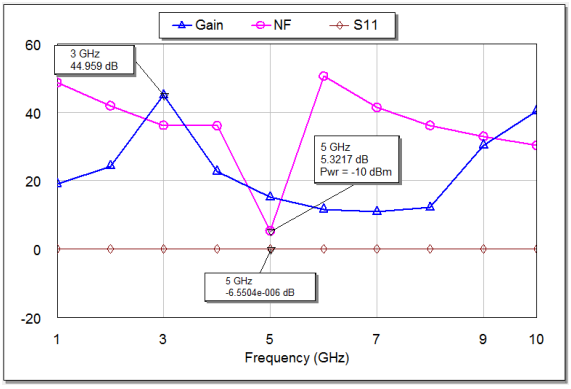
(b) **(c)**

Figure 6. Simulation Results Of Post Distortion a) Gain, S11,NF b) IIP2 c) IIP3

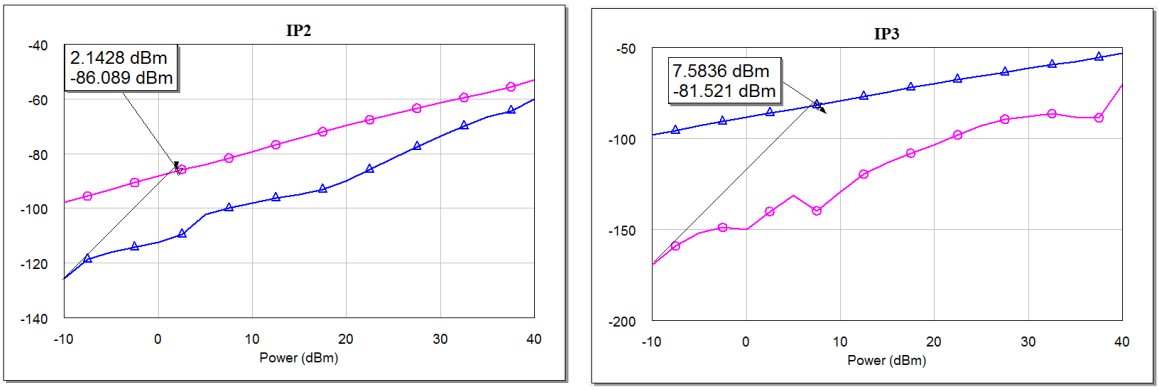
While previous techniques only compensate gm's nonlinearity, noise/distortion technique can remove all structural distortions generated by the main transistor, including non-linearity of gm and gds. After the distortion of the main transistor is removed, the distortion of the auxiliary transistor no longer suppresses the nonlinearity, which creates two terms:

1) Structural third-order distortion of the auxiliary transistor.

2) Second-order interaction from the CG-CS cascade. Operating the optimal or complementary TS of the auxiliary transistor improves the linearity.



(a)



(b) **(c)**

Figure 7. Simulation Results Of Noise/Distortion Cancellation a) Gain, S11,NF b) IIP2 c) IIP3

Conclusion

In this work, different linearization techniques have been investigated in order to overcome the distortions caused by CMOS low noise amplifiers used in RF (Radio Frequency) communication systems.

Table 1. Comparison of the performance of the linearized LNAs with MDS techniques

	CMOS Process	Supply Voltage (V)	Frequency (GHz)	Gain (dB)	İnput Return Loss,S_{11} (dB)	Noise Figure(dB)	IIP3(dBm)	DC Power (mW)
[8]	0.18 µm	1.8	1.575-2.4	13.7	<-10	3.12	-3.01	14.4
[9]	0.18 µm	0.7	2.4	11.4	-10	2.8	-8.6	2.89
[10]	0.18 µm	-	2.5	20.1	-26.4	1.44	8.9	4.36
[11]	0.13 µm	3.3	0.3-1	11 – 16	< -11	< 2.7	> 16 (µ)	16
[12]	0.18 µm	1.8	3.1 - 10.6	13.2- 14.8	<–11.5	<3	−3.1 - −8.6	23.7
[13]	0.13 µm	0.6	0.9	13.7	-27	1.1	+7.77	6.19
[14]	0.18µm	1.3	0.8 – 2.5	15.1	-	1.63	+21	6
[15]	90nm	3.3	1.3	15.4	<-14	1.36	*	132
This Work	0.18µm	1.8	1-5	8.934	-10.53	1.92	27.74	14.129

*OIP3(third order output intercept point) =33.7 dBm, IMD3=-65 dBm

The traditional derivative superposition method usually worsens degradation from the second order when improving the third order intercept point. Thus, the improved derivative superposition method is preferred. And, as a result of this application, is seen that in Table 1, IIP2 and IIP3 values are much better than the post distortion and noise / distortion cancellation methods. Besides, it is seen that the gain are lower than other methods. Input impedance loss and DC power consumption are average values.

Table 2. Comparison of the performance of the linearized lnas with post distortion techniques

	CMOS Process	Supply Voltage (V)	Frequency (GHz)	Gain (dB)	İnput Return Loss,S_{11} (dB)	Noise Figure(dB)	IIP3 (dBm)	DC Power(mW)
[16]	0.25 µm	2.6	0.869-0.894	16.2	<-10	1.2	+8	-
[17]	0.18 µm	1.8	2	12.8	-	1.4	+13.3	-
[18]	0.18 µm	1.8	2	13.7	-	1.68	+10.2	-
[19]	0.13 µm	1.3	1.5-8.1	8.6˜11.7	<-.9	3.6˜6	+11.7˜14.1	2.62
This work	0.18 µm	0.8	1-5	20.91	-13.9	1.56	10.33	14.35

In order to achieve better linearity in the post distortion method, all transistors are operated in saturation region. And when the results are examined, it is seen that in Table 2, post distortion method has a lower noise figure than the other methods. The input impedance loss, IIP2, IIP3 and DC power consumption are average values when a relatively good gain is seen.

Table 3. Comparison of the performance of the linearized lnas with noise/distortion cancellation techniques

	CMOS Process	Supply Voltage (V)	Frequency (GHz)	Gain (dB)	İnput Return Loss,S_{11} (dB)	Noise Figure(dB)	IIP3(dBm)	DC Power(mW)
[20]	0.25 µm	2.5	0.2-1.6	13.7	<-8	2˜2.4	0	-
[21]	0.13 µm	1.2	2.1	5.2	-	3.0	+10.5	12.6
[22]	0.13 µm	1.5	0.8-2.1	14.5	-	2.6	+16	-
[23]	65nm	1.2	0.2-5.2	13-15.6	-	<3.5	>0	21
This work	0.18 µm	1.07	1-5	44.95	<0	5.32	7.583	1.858

In noise/distortion cancellation method, higher gains are achieved compared to other methods. In addition, an ideal input impedance loss is achieved and very low DC power consumption is achieved. However, the noise level in the circuit is above the expected value and is not observed in the ideal values when compared with other methods. In addition, IIP2 and IIP3 are average values according to the previous studies and are lower than other methods.

As a result, in general, it can be seen that in Table 4 in the modified derivative method with the best performance of IIP2 and IIP3, the lowest noise addition to the circuit is achieved in the post distortion method and the highest gain is obtained by noise / distortion cancellation method. It is seen that these results are supported when the previously made and comparative sources and publications are examined.

Table 4. Comparison of the performance of the performed techniques

Linearization Tecniques	CMOS Process	Supply Voltage (V)	Frequency (GHz)	Gain (dB)	İnput Return Loss,S_{11} (dB)	Noise Figure(dB)	IIP2 (dBm)	IIP3 (dBm)	DC Power (mW)
MDS	0.18µm	1.8	1-5	9.016	-10.53	1.922	+32.455	+27.74	14.129
PD	0.18µm	0.8	1-5	20.95	-13.94	1.506	+8.533	+10.331	14.35
NDC	0.18µm	1.07	1-5	43.57	-1.327	6.917	+2.142	+7.583	1.858

In future work, this work is expanded to include new linearization techniques for designing a more ideal low-noise amplifier. In addition to this, it is planned to use the AWR (Applied Wave Research).

Design Environment program to implement and apply the low noise amplifier model. In this way, it is possible to compare the simulation results obtained with the application results and make a more accurate interpretation.

References

[1] Sorin, V., 2013. High-Frequency Integrated Circuits, Published in the United States of America by Cambridge University Press, New York.

[2] Anandini, C., Kumar, R., & Talukdar, F. A., A Comparative Study of Linearization Techniques of CMOS LNA, *International Journal of Recent Development in Engineering and Technology*,3 (2014), 2, pp. 2347-6435

[3] Zavarei, M. J., Kargaran, E., & Nabovati, H., Design of high gain CMOS LNA with improved linearity using modified derivative superposition, *Electronics, Circuits and Systems (ICECS), 2011 18th IEEE International Conference,* (2011),pp. 322-325

[4] Zhang, H., & Sánchez-Sinencio, E., Linearization techniques for CMOS low noise amplifiers: A tutorial, *IEEE Transactions on Circuits and Systems I: Regular Papers*, (2011), 58(1), pp.22-36.

[5] V. Aparin and L. E. Larson, Modified derivative superposition method for linearizing FET low-noise amplifiers, *IEEE Trans. Microw. Theory Tech., vol. 53*, (2005), 2, pp. 571–581.

[6] Jussila J. and Sivonen P., A 1.2-V highly linear balanced noise-cancelling LNA in 0.13-µm CMOS, *IEEE J. Solid-State Circuits, vol. 43*, (2008), 3, pp. 579–587.

[7] S. C. Blaakmeer, E. A. M. Klumperink, D. M. W. Leenaerts, and B. Nauta, Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling, *IEEE J. Solid-State Circuits, vol. 43*, (2008) , 6, pp. 1341–1350.

[8] Loong, T. T., Hashim, A., Mustaffa, M. T., & Noh, N. M., 1.575 GHz to 2.48 GHz multi-standard low noise amplifier using 0.18-µm CMOS with on-chip matching. *In Industrial Electronics and Applications (ISIEA), 2011 IEEE Symposium on*, (2011), pp. 100-103.

[9] Dehqan, A. R., Kargaran, E., & Mafinezhad, K., Design of low-voltage low-power Dual-Band LNA with using DS method to improve linearity, *In Electrical Engineering (ICEE), 2012 20th Iranian Conference, IEEE,* (2012), pp. 88-91.

[10] Dai, R., Zheng, Y., He, J., Kong, W., & Zou, S., A 2.5-GHz 8.9-dBm IIP3 current-reused LNA in 0.18-µm CMOS technology, In *Radio-Frequency Integration Technology (RFIT), IEEE,* (2014), pp. 1-3.

[11] Varga, G., Heising, C. P., Ashok, A., Subbiah, I., Schrey, M., & Heinen, S., A highly linear broadband LNA for TV white spaces and cognitive radio applications, In *Microwave Conference (GeMiC),IEEE,* (2015), pp. 296-298.

[12] Eslamifar, O., & Shirazi, R. S.,Design an ultra wide band low noise amplifier for use in WLAN applications, In *Electrical Engineering (ICEE), IEEE,* (2014), pp. 111-115.

[13] Kukde, A. A., Kumaravel, S., & Venkataramani, B., A high linearity folded cascode Low Noise Amplifier for wireless receivers, In *Circuit, Power and Computing Technologies (ICCPCT), IEEE, (2014),* pp. 1344-1348.

[14] Thacker, M. B., Awakhare, M., Khobragade, R. H., & Dwaramwar, P. A., Multi-standard highly linear CMOS LNA. In *Electronic Systems, Signal Processing and Computing Technologies (ICESC),IEEE,* (2014), pp. 63-68.

[15] Gao, W., Chen, Z., Liu, Z., Cui, W., & Gui, X., A highly linear low noise amplifier with wide range derivative superposition method, *IEEE Microwave and Wireless Components Letters*, (2015), *25*(12), pp. 817-819.

[16] Kim, N., Aparin, V., Barnett, K., & Persico, C., A cellular-band CDMA 0.25-/spl mu/m CMOS LNA linearized using active post-distortion, *IEEE journal of solid-state circuits*, (2006), *41*(7), pp.1530-1534.

[17] Kim, T. S., & Kim, B. S., Post-linearization of cascode CMOS low noise amplifier using folded PMOS IMD sinker. *IEEE microwave and wireless components letters*, (2006), *16(4)*, pp.182-184.

[18] Kim, T. S., & Kim, B. S., Linearization of differential CMOS low noise amplifier using cross-coupled post distortion canceller. In *Radio Frequency Integrated Circuits Symposium, 2008. RFIC 2008. IEEE* (pp. 83-86). IEEE.

[19] Zhang, H., Fan, X., & Sinencio, E. S., A low-power, linearized, ultra-wideband LNA design technique. *IEEE Journal of solid-state circuits*, (2009), *44*(2), pp. 320-330.

[20] Bruccoleri, F., Klumperink, E. A., & Nauta, B., Wide-band CMOS low-noise amplifier exploiting thermal noise canceling, *IEEE Journal of Solid-State Circuits*, (2004), *39*(2), pp. 275-282.

[21] Jussila, J., & Sivonen, P., A 1.2-V Highly Linear Balanced Noise-Cancelling LNA in 0.13-$\mu {\hbox {m}} $ CMOS. *IEEE Journal of Solid-State Circuits*, (2008). *43*(3), pp. 579-587.

[22] Chen, W. H., Liu, G., Zdravko, B., & Niknejad, A. M., A highly linear broadband CMOS LNA employing noise and distortion cancellation. *IEEE Journal of Solid-State Circuits*, (2008), *43*(5), pp. 1164-1176.

[23] Blaakmeer, S. C., Klumperink, E. A., Leenaerts, D. M., & Nauta, B., Wideband balun-LNA with simultaneous output balancing, noise-canceling and distortion-canceling. *IEEE Journal of Solid-State Circuits*, (2008), *43*(6), pp. 1341-1350.