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Hybrid Converter Design Based on Boost and Push Pull Topologies

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Abstract

This paper introduces a hybrid converter topology based on boost and push-pull configurations for electric vehicle (EV) charging applications. In the proposed converter structure, an RCD snubber circuit is used to reduce the thermal losses in power electronic devices and the peak voltages in individual components. Thus, by reducing the peak voltages on the switching components, the efficiency of the proposed hybrid converter structure is increased. The proposed topology aims to reduce the peak voltage and voltage stress on the switching components and to reduce the losses by reducing the transformation ratio of the transformer in the push-pull converter. In addition, another aim of the proposed topology is to provide improved continuous and rectified output current, thus extending the system's life in applications. Moreover, the proposed converter is tested in continuous conduction mode (CCM) and compared with similar existing designs. To verify the mathematical analysis, the 500 W output power converter designed using the proposed hybrid estimation structure is tested in a simulation environment. The analysis yielded continuous and direct current. As a result of the simulation analysis, a significant reduction in the peak voltages and voltage stresses on the switching elements occurred with the proposed converter topology. In addition, by reducing the transformer turns ratio, transformer losses are reduced.

Keywords: Boost topology, hybrid converter, push-pull topology

Boost ve Push Pull Topolojilerine Dayalı Hibrit Dönüştürücü Tasarımı

Öz

Bu makalede, elektrikli araç (EV) şarj uygulamaları için yükseltme ve itme-çekme yapılandırmalarına dayalı bir hibrit dönüştürücü topolojisi tanıtılmaktadır. Önerilen dönüştürücü yapısında, güç elektroniği aygıtlarındaki termal kayıpları ve ayrı bileşenlerdeki tepe voltajlarını azaltmak için bir RCD sönümleme devresi kullanılmaktadır. Böylece anahtarlama bileşenleri üzerindeki pik voltajları azaltarak, önerilen hibrit dönüştürücü yapısının verimliliği artırılmaktadır. Önerilen topolojinin amacı, anahtarlama bileşenleri üzerinde oluşan pik gerilimler ve gerilim streslerin azalmak ve itme çekme dönüştürücüdeki transformatörün dönüştürme oranını düşürerek kayıpları azaltmaktır. Ek olarak, önerilen topolojinin diğer bir amacı, iyileştirilmiş sürekli ve doğrultulmuş çıkış akımı sağlayarak uygulamalarda sistem ömrünü uzatmaktadır. Dahası, önerilen dönüştürücü sürekli iletim modunda (CCM) test edilmekte ve benzer mevcut tasarımlarla karşılaştırılmaktadır. Matematiksel analizi doğrulamak için, önerilen hibrit tahmin yapısını kullanarak tasarlanmış 500 W çıkış gücü dönüştürücüsü bir simülasyon ortamında test edilmiştir. Analiz sürekli ve doğru akım elde edilmiştir. Simülasyon analizi neticesinde önerilen dönüştürücü topolojisi ile anahtarlama elemanları üzerinde oluşan pik gerilimler ve gerilim streslerinde önemli bir azalma meydana gelmiştir. Ayrıca, transformatör dönüştürme oranının düşürülmesi ile trafonun kayıpları azalmıştır.

Anahtar Kelimeler: Boost topolojisi, hibrit dönüştürücü, itme-çekme topolojisi

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1. Introduction

The interest in the development of electric vehicles (EVs) and their power-electronic components is increasing among researchers due to the rapid pollution of the environment by fossil fuels that is causing mainly global warming. The rapid transition to electric vehicles reduces the harm to the environment (Anitha et al., 2023). In the context of the quiet and fast operation, fast charging, and efficiency of EVs, a high-gain DC-DC converter, which is a critical power electronic interface, is required to regulate the voltage for the electrical motor (Kumar and Krishnasamy, 2022).

Different topologies for charging circuits of EVs have been introduced in the literature (Choi et al., 2020; Costa et al., 2020; Hussein et al., 2021). In general, chargers include AC-DC converters and DC-DC converters, which may include isolation transformers (Choe et al., 2010; Gallardo-Lozano et al., 2011). EV charges may also contain boost-converter based power factor correction components. To provide power factors, these chargers may use uncontrolled rectifiers connected with boost converters, single step-up converters, interleaved boost converters reducing the input inductance or bridgeless circuits (Aguilar et al., 1997; Garcia et al., 2006; Lee et al., 2011; Musavi et al., 2011; Ni et al., 2011). Although conventional DC-DC step-up converters may be applied in EVs because they offer high voltage gain, due to the voltage and current ripples on the solid-state switches at high-duty cycles and unregulated characteristics during load changes they are restricted in practice (Belhimer et al., 2018; Sadaf et al., 2020; Muthusamy et al., 2021).

DC-DC converters are examined in some concepts such as unidirectional, bidirectional, single-port, and multi-port. The unidirectional converters allow the power to flow from the grid to EVs, that is, only EV batteries are charged from the grid. In contrast to these converters, bidirectional converters allow the power flow the grid to EVs and from EVs to grid, meaning, at discharge mode, EVs can inject the residual or non-residual energy into the grid. On the other hand, single-port converters have just one input and one output. Also, multi-port converters have more than one input and output (Sassi et al., 2019; Elserougi et al., 2022; Gopalasami et al., 2023). In terms of soft switching and bidirectional energy flow dual active bridge-type converters are adopted in many applications (Xu et al., 2023). However, high primary current ripples and transformer leakage inductance are its disadvantages.

The isolated step-up DC-DC converters have a key role in industrial applications due to their features such as high efficiency, high power density, high reliability, and low electromagnetic interference. In particular, the isolated DC-DC converters based on the topology of half-bridge, full-bridge, and push-pull are used to step up the voltage level in electric vehicles, renewable energy systems, and energy storage systems (Xiao et al., 2022). In contrast to bridge converters, push-pull converters have fewer switching components and low conduction losses, which makes them preferable for systems with low voltage input and high-power density (Larico and Barbi, 2011).

The push-pull converters can be basically classified into two main categories: current-fed and voltage-fed. Current-fed push-pull converters offer low input current ripple,

low diode voltage rating, low transformer turns ratio, negligible diode ringing, low duty cycle loss, and soft-switching in a wide range. On the other hand, voltage-fed converters have low conduction losses on primer sides and can switch with low voltage level that using switches with low on-state resistance. However, for the current-fed topology, high voltage spikes occur on the semiconductors. Also, the voltage-fed topology has disadvantages such as high fluctuating current at input, soft-switching in a limited range, rectifier diode ringing, and high circulating current (Xuewei and Rathore, 2014; Tandon and Rathore, 2021). Some techniques such as zero-voltage switching (ZVS) (Boonyaroonate and Mori, 2002; Chu and Li, 2009; Yuan and Wu, 2013; Chen et al., 2016; Xu et al., 2018), zero-current switching (ZCS) (Sree and Rathore, 2016; Tandon and Rathore, 2021) and active clamp (Wu et al., 2008; Jiang et al., 2021) are proposed to overcome these situations.

In Shoyama and Harada (1993), a current-fed and naturally clamped based push-pull converter is proposed which uses secondary modulation eliminating the need for passive snubbers and active clamps. In Tai and Hwu (2023), the authors proposed a push-pull converter including inductance (L) - capacitance (C) resonant circuit for energy systems. The converter consists of two sides: the primary side and the secondary side. Further, the primary side uses ZVS, and the second part uses ZCS. The L-C-L topology is proposed in Yuan et al. (2007) which is located on the primary side of push-pull converter. In Tarzamni et al. (2007), the soft switching isolated push-pull converter, containing three winding transformers, is proposed. This converter uses a voltage doubler on the secondary side and thus, high voltage control efficiency can be achieved in a wide range of input and output voltage. In Liu et al. (2023), the authors designed a push-pull class $\phi 2$ converter with harmonic-based approach. The soft switching contains zero-voltage derivative switching (ZDS). The DC-DC converter operates with adjustable power while maintaining high system efficiency with the ZDS method. A dual close-loop and bidirectional converter is introduced in Zhang et al. (2023). Also, the authors considered the operation of the push-pull DC autotransformer by analyzing the harmonic transfer function (HTF). In Wu et al. (2016), a push-pull converter with active clamp is proposed using ZVS method under wide load range.

Furthermore, the cascade connection increases the efficiency of the converter. However, there is no effective decrease in the voltage stress across the switches (Kumar and Krishnasamy, 2022). In Mukkapati et al. (2020), a quadratic boost converter (QBC) is proposed by combining two converters via one solid-state switch to overcome voltage stress and complexity. In Singh et al. (2004) and Manjrekar et al. (2000), multilevel converters are employed using more than one low-voltage semiconductor switch to ensure high power and high output voltage. Thus, the converters operated with AC currents with decreased total harmonic distortion and EMI noise. In Hussein et al. (2021), a topology with a few semiconductor switching components is proposed. However, this topology has many passive components that affect efficiency. An isolated interleaved DC-DC converter with power factor correction is proposed in Choi et al. (2020), which includes many semiconductor components and has two

half-bridge voltage-fed circuits. In Knabben et al. (2020), the authors proposed the L-L-C topology-based converter which used boundary/discontinuous conduction mode and improved the power density. The converter includes two inductors, three capacitors and two diodes are introduced in Elsayad et al. (2019). This converter offered the voltage gain and decreased the voltage stress on the power switches. A coupled inductor connected to a voltage multiplier circuit is adopted in Hassan et al. (2019). Thus, the proposed boost converter ensured a high voltage ratio and also offered adjustable gain by adjusting the ratio of the winging. In Shanthi et al. (2021), extra inductors and capacitors are used in the converter to provide effective voltage gain. This technique significantly reduced the voltage stress on the power switches. In cascade structure, voltage stress on power switches increases. However, no advantage other than effective voltage gain is guaranteed. Also, the current stress on the primary side is high in L-L-C structures that include more than one switch. This causes the conduction losses to increase and complicates the control of power switches. Using extra inductors may cause an imbalance in load current. This causes heat increase on the component. Moreover, extra components impose significant limitations. Current pulsating is inevitable while improving voltage gain. On the other hand, secondary losses are dominant in converters including coupled inductors and transformers (Zhou et al. 2021; Kumar and Krishnasamy, 2022).

There are some studies in the literature proposed about hybrid and interleaved topologies in recent years. Qin et al. (2025) presented a Boost-Sepic structure-based converter which includes a soft-switching resonant tank. The converter gets the voltage gain through two active switches and a coupled inductor. An interleaved converter is proposed (Karimi et al. 2024). The converter has a coupled inductor and a passive lossless clamp circuit for improving the voltage boost ratio. A quadratic boost converter is proposed with the voltage multiplier cells (Li et al. 2024). A modified hybrid Boost-Luo converter is proposed to supply the Brushless DC (BLDC) motor through a three-phase inverter (Maheswari et al. 2025). The converter consists of a voltage multiplier cell and a three-winding coupled inductor. Alizadeh et al. (2024) proposed a hybrid interleaved converter with quadratic voltage gain, which includes auxiliary elements, for renewable energy systems. A DC-DC converter including a phase-shifted full-bridge converter with a half-bridge LLC converter connected in series is proposed to provide a high output voltage (Jeong et al. 2024).

This study proposes a hybrid DC-DC converter based on the boost and push-pull topologies. The conventional methods which use individual structures have low voltage gain at high frequencies and voltage stress occurs on the components. Also, the design of a transformer to step up low voltage to high voltage levels is costly and difficult at high frequencies. The proposed converter combines two simple topologies, providing high voltage gain and facilitating transformer design. Moreover, the voltage stress on the semiconductor components is reduced and thermal losses are minimized. The proposed converter consists of boost topology on the primary side and push-pull topology on the secondary side. The boost side includes simple modifications such as an extra diode and a current balancing resistor. The push-pull side contains a filter

composed of series L and parallel C connected to the secondary side of the transformer and an external filter inductor that reduces the current ripple is connected to the primary side of the transformer. Furthermore, the DC-DC converter includes RCD snubber circuits to reduce voltage spikes across the semiconductor components. The main contributions of the proposed study can be given as follows:

- Different from the existing studies existing in literature, the proposed structure integrates two independent converter topologies in a cascaded hybrid configuration, where each topology retains the capability to operate independently.
- The semiconductor power electronic switching devices used in both structures are controlled independently with different control schemes, which is a distinctive feature compared to previous works. This approach effectively reduces peak voltage and voltage stress on semiconductor switching devices both during switching duration and when the switches are in the off state.
- By employing the proposed cascaded hybrid structure, two-stage voltage level conversion is achieved. Consequently, the turns ratio of the transformer designed in a push-pull converter topology is kept low, which not only offers significant advantages on high frequency transformer design but also plays a significant role in reducing eddy current and core (hysteresis) losses.

In Section 2, the proposed converter is introduced, and in Section 3, its operating modes, and the design of the boost converter and the push-pull converter sides are discussed, the proposed circuit is simulated in Section 4, the PID controller is briefly described in Section 5, and the last section contains the results and discussions.

2. Description of the converter

The structure of the ZVS converter with a step-up converter proposed in this study is shown in Figure 1. The first side of converter consists of a PWM-controlled boost converter mentioned in Parvari et al. (2018) that includes some modifications. Basically, the circuit contains an RDC snubber circuit, a semiconductor switch, a main diode, a filter capacitor and an air inductor. The air core inductor can prove the semiconductors to switch at high frequencies and reduce the charging and discharging time of the total capacitances of semiconductors (Yapici and Inan, 2024). The second side of converter consists of a push-pull converter. The basic design of the push-pull converter is mentioned in Jalbrzykowski and Citko (2013). However, a snubber circuit is used for the switching elements and a series resonant. Also, a filter circuit is connected to the secondary side of the high-frequency (HF) transformer as in Tai and Hwu (2023). The main circuit of the push-pull circuit converter side includes two semiconductor switches, L_{bus} inductance, C_{bus} capacitance, an RDC snubber circuit, an HF transformer, a resonant filter circuit, a half-bridge rectifier, output capacitors and a load resistor. C_{bus} is used to smooth and filter the output voltage of the boost converter which is applied to push pull converter as the bus voltage. Also, L_{bus} reduces the current ripple of the primary side of HF transformers.

The boost converter does not need extra parasitic capacitance. The input voltage and input current are considered constant. The fast recovery diode (D_1) provides the charging of the output capacitor. The extra load resistor connected to the output of the

boost converter stabilizes the output current and prevents the second side from overcurrent and overvoltage.

The resonant inductance L_r comprises secondary leakage inductance (L_{ts}) and primary leakage inductances (L_{tp1} and L_{tp2}). L_{tp1} and L_{tp2} are too small and can be neglected. Therefore, L_r is equal to L_{ts} and connected in series to the resonant filter circuit. On the other hand, the magnetizing inductance (L_m) of the HF transformer is very large. Thus, the magnetizing current can be assumed as $0A$ (Tai and Hwu, 2023). An output capacitor with large capacitance provides a constant output voltage to the load resistance.

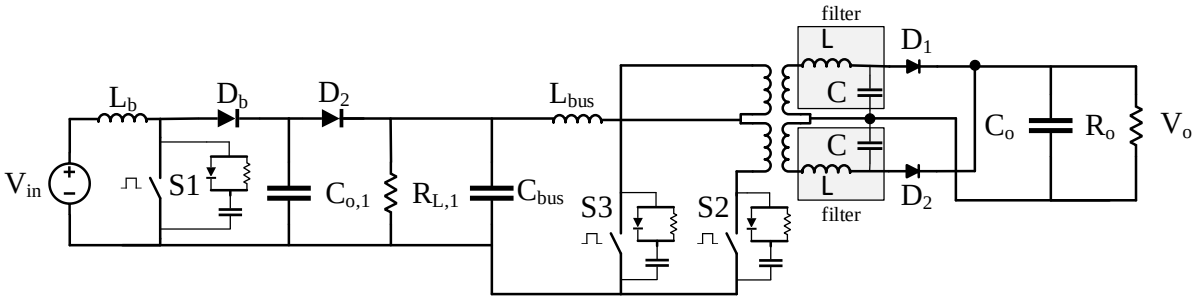


Figure 1. The proposed hybrid converter structure, which is composed of boost and push-pull topology.

The duty cycles of both converter parts are controlled by PID controllers. Note that the switching frequencies of all switches are the same and set to $40kHz$.

There are some assumptions for operation mode analysis simplification:

- All components are ideal.
- The input voltage is constant.
- All switches are equal and run at high frequency.
- The HF transformer is ideal, and the equivalent circuit is defined with L_r and L_m.
- The primary side turns $N_p = N_{p1} = N_{p2}$.

3. Operation modes of the hybrid converter

The proposed converter includes a boost converter and a push-pull converter. Switch S1 operates with a duty cycle of 0.85, while switches S2 and S3 operate with a duty cycle of 0.45. Because, in push-pull topology, the conversion is achieved by switching the two different switches in one switching period with a duty cycle cover the half period. But it is obvious that the dead-time is a crucial problem for the switches during the transient state. Therefore, a tolerance of duty cycle as 5% can be determined for each switch. The boost side and push-pull side are independent of each other. The operation modes of the boost side are examined in two intervals. Then, the operation modes of the push-pull side are examined in four intervals. The switching frequencies are equal to the frequency of the resonant circuit at the output, so the resonant network is filtered at high frequency and rectified by the half-bridge rectifier to obtain DC output voltage.

3.1 The operation of boost converter side

For mathematical analysis, the definitions of the symbols used are as follows; L_b is the inductor of the boost side, T_{on} is the ON state time, $V_{L,on}$ is the voltage of L_b at ON state, $V_{L,off}$ is the voltage of L_b at OFF state, V_{in} is the input voltage, $V_{o,b}$ is the output voltage boost converter side, D is the duty ratio, $i_S(t)$ is the snubber current, C_{OSS} is the output capacitance of S1, $I_{L,pk}$ is the peak current of the inductor, C_S is the snubber capacitor, R_S is the snubber resistor, i_L is the current of L_b, f_{sw} is the switching frequency, T_0 is the resonant time between C_S and R_S, P_o is the output power needed, $C_{o,1}$ is the output capacitor of boost convertor, $I_{D,b}$ is the current of fast recovery diode 1, $I_{D,2}$ is the current of diode 2, and I_{out} is the nominal output current of the boost side. Figure 2 indicates the operation of the boost side.

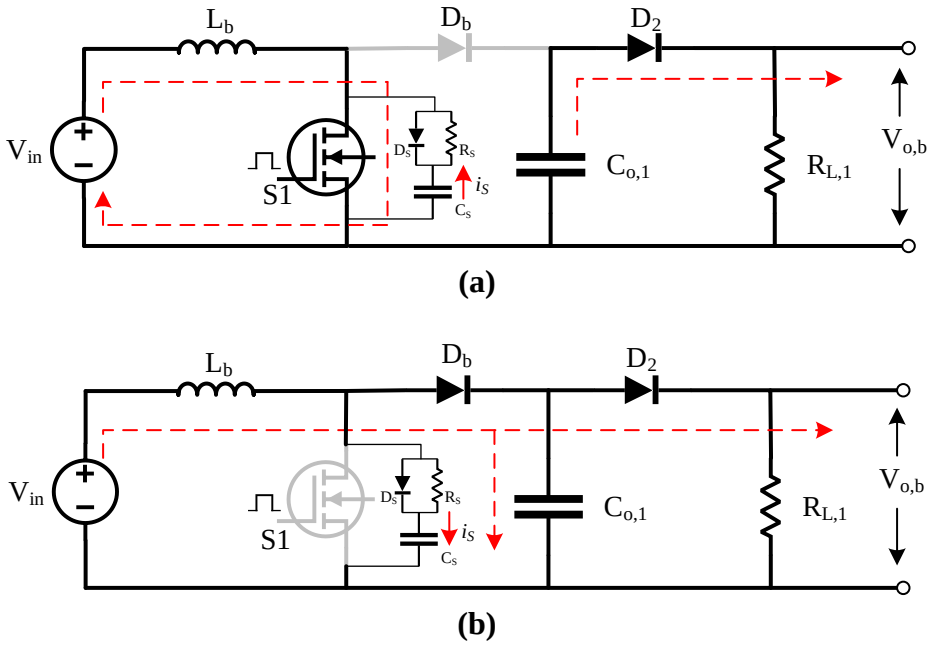


Figure 2. The operation modes of the boost side; (a) ON-state of S1, (b) OFF-state of S1.

Figure 3 illustrates the waveforms of V_{GS}, V_{DS}, i_L, $I_{D,b}$, the current pass through $C_{o,1}$ ($I_{Co,1}$), i_S, the voltage of L_b ($V_{L,b}$), $I_{o,b}$ and $V_{o,b}$. A high-value output filter capacitor should be used to reduce the ripples of the output current and output voltage. However, this value is limited due to the influence of the push-pull side filter inductor and HF transformer. This will cause prominent ripples in the output current and output voltage. The $R_{L,1}$ resistor is constant and has a high value. This resistor is added to protect the capacitor from overvoltage during idle operation.

Time interval 1 ($t_0 \leq t \leq t_1$): $S1$ is ON state. In this interval, i_L is increased as much as Δi_L. At $t = t_0$, snubber capacitor C_S starts to discharge through the snubber resistor R_S. The snubber diode D_S and the main boost diode D_b are reverse biased. D_2 remains forward biased. The load resistor $R_{L,1}$ of the boost side is supplied by the output capacitor $C_{o,1}$. Δi_L can be obtained as follows:

$$V_{L,on} = V_{in} = L_b \frac{di_L(t)}{dt}, \qquad V_{L,off} = V_{in} - V_{o,b} = L_b \frac{di_L(t)}{dt} \tag{1}$$

As taken the integration of Equation 1 a new expression can be obtained as given below:

$$\int_0^{T_{on}} \frac{di_L(t)}{dt} = \frac{1}{L_b} \int_0^{T_{on}} V_{L,on} dt \tag{2}$$

From Equation 2, Δi_L can be obtained as:

$$\Delta i_L = \frac{1}{L_b} V_{L,on} T_{on} = \frac{V_{in} D}{L_b f_{sw}} \tag{3}$$

Also, at the interval of ON state the voltage across the C_S can be expressed as below:

$$V_{CS} = V_{o,b} - R_S i_S(t), \qquad i_S(t) = -C_S \frac{dV_{CS}(t)}{dt} \tag{4}$$

and,

$$i_S(t) \approx \left(\frac{C_{OSS} I_{L,pk}}{C_{OSS} + C_S}\right)\left(1 - e^{-\frac{t}{T_0}}\right) \tag{5}$$

where,

$$T_0 = R_S \frac{C_{OSS} C_S}{C_{OSS} + C_S}, \qquad (C_S \gg C_{OSS}) \tag{6}$$

Time interval 2 ($t_1 \le t \le t_2$): $S1$ is OFF state. In this interval, i_L is decreased as much as Δi_L. At $t = t_1$, C_S starts to charge through the snubber resistor D_S. D_S and D_b are forward biased. D_2 also maintains forward bias. $R_{L,1}$ is supplied by $C_{o,1}$. Δi_L is similar to the previous interval and given as:

$$\Delta i_L = \frac{V_{in} D}{L_b f_{sw}} \tag{7}$$

At the interval of OFF state, the voltage across the C_S can be given as:

$$V_{CS} = V_{o,b} - \frac{I_{L,pk}}{C_S} t \tag{8}$$

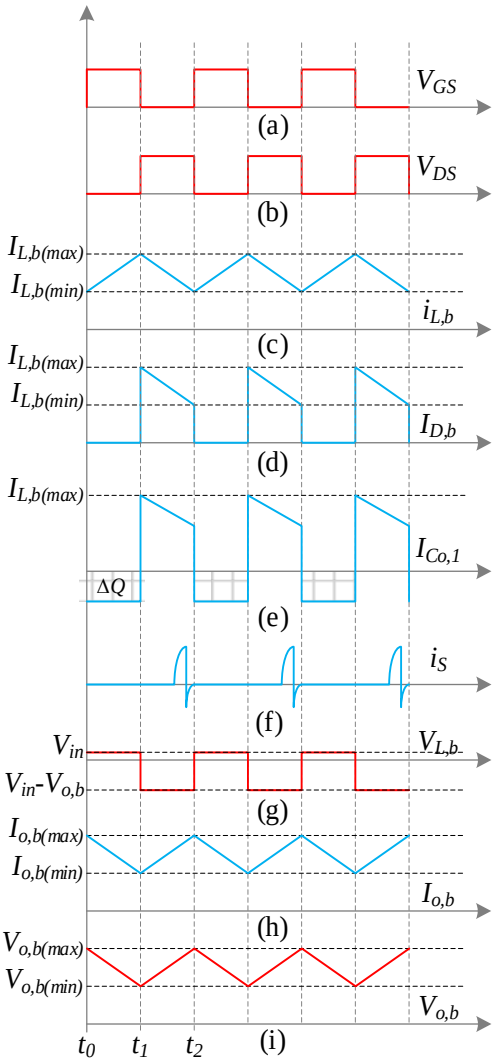


Figure 3. The waveform of the boost side; (a) the gate signal, (b) the voltage of drain-source, (c) the current pass through the boost side inductor, (d) the current pass through the main diode, (e) the current pass through the output capacitance of boost side, (f) the current of snubber circuit, (g) the voltage of boost side inductor, (h) the output current of boost side, (i) the output voltage of boost side.

3.2 The operation of push-pull side

As previously mentioned, switches S2 and S3 run with a duty cycle of 0.45 (see Figure 8). Figure 4 illustrates the situation of the components of the push-pull converter circuit under the operating modes. Figure 5

shows the waveforms of $V_{GS,1}$, $V_{GS,2}$, $V_{DS,1}$, $V_{DS,2}$, the filter current (I_{filter}), $I_{D,1}$, $I_{D,2}$, $i_{S,1}$ and $i_{S,2}$. The output signal of the transformer is filtered at high frequency by a resonant circuit and then rectified by a half-bridge rectifier to obtain output voltage. For mathematical analysis, the definitions of the symbols used are as follows; i_{Lm} is the magnetization current, i_{Lr} is the current of the series resonant inductance of the secondary windings, $V_{in,pp}$ is the input voltage of push-pull converter side ($V_{in,pp} = V_{o,b}$), V_{out} is the output voltage of the converter, I_{out} is the output current, $i_{s,1}$ is the current of snubber circuit of S1, $i_{s,2}$ is the current of snubber circuit of S2, $C_{OSS}{}'$ is the output capacitance of the each switch, $C_{S,1}$ is the snubber capacitance of S1, $D_{S,1}$ is the snubber diode of S1, $R_{S,1}$ is the snubber resistance of S1, $C_{S,2}$ is the snubber capacitance of S2, $D_{S,2}$ is the snubber diode of S2, $R_{S,2}$ is the snubber resistance of S2, Z_r is the series resonance impedance, w_{LC} is the resonant frequency of the filter circuit, L is the inductance of the filter circuit, C is the capacitance of the filter circuit, R_o is the load resistance, V_{LC} is the voltage of the filter circuit, n is the turn ratio, V_{DS} is the voltage between drain and source terminal of each MOSFET, I_{diode} is the current of the diode of the half-bridge rectifier, V_{diode} is the voltage of the diode of the half-bridge rectifier, T is period of the PWM signal, P_{out} is the output power, t_d is the dead time of both switches at the OFF state, C_{sw} is the output capacitance of the MOSFET, R_{ac} is the A resistance, and Z_o is the characteristic impedance of the resonant circuit.

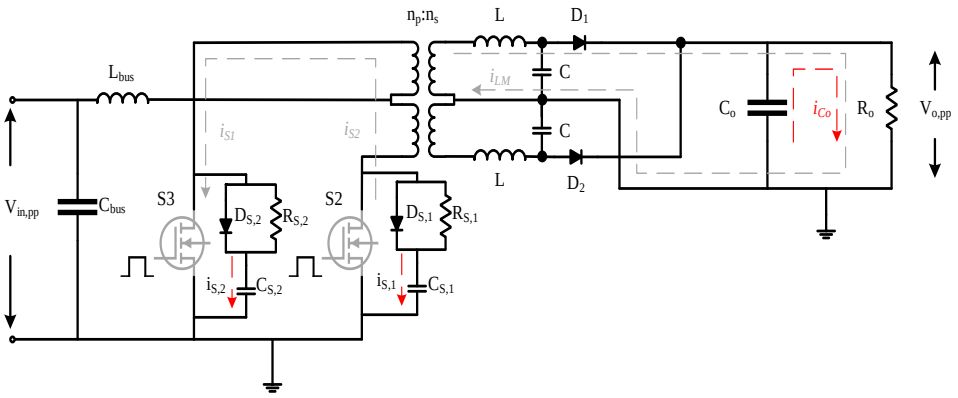
The time intervals of the four modes are described below.

Time interval 1 ($t_0 \le t \le t_1$): During this interval, S2 and S3 are turned off. i_{Lm} charges the drain-source capacitance of S1 as $2V_{in,pp}$. The changing of i_{Lm} is given in Equation 9. On the other hand, the drain-source capacitance of S2 discharges. Also, $i_{s,1}$ and $i_{s,2}$ are given in equations 10 and 11.

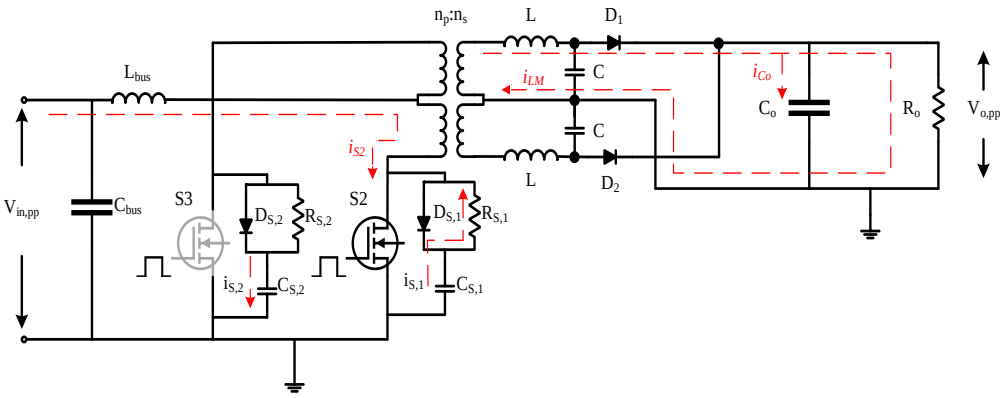
$$i_{Lm} = -\frac{nV_{in,pp}}{L_m}(t - t_0) - i_{Lm}(t_0) \qquad (9)$$

$$i_{s,1} = i_{S,1}(t_0) - \left(\frac{C_{OSS}{}'I_{pk}}{C_{OSS}{}' + C_{S,1}}\right)\left(1 - e^{-\frac{t}{T_{0,1}}}\right) \qquad (10)$$

$$i_{s,2} = i_{S,2}(t_0) - \left(\frac{C_{OSS}{}'I_{pk}}{C_{OSS}{}' + C_{S,2}}\right)\left(1 - e^{-\frac{t}{T_{0,2}}}\right) \qquad (11)$$



(a)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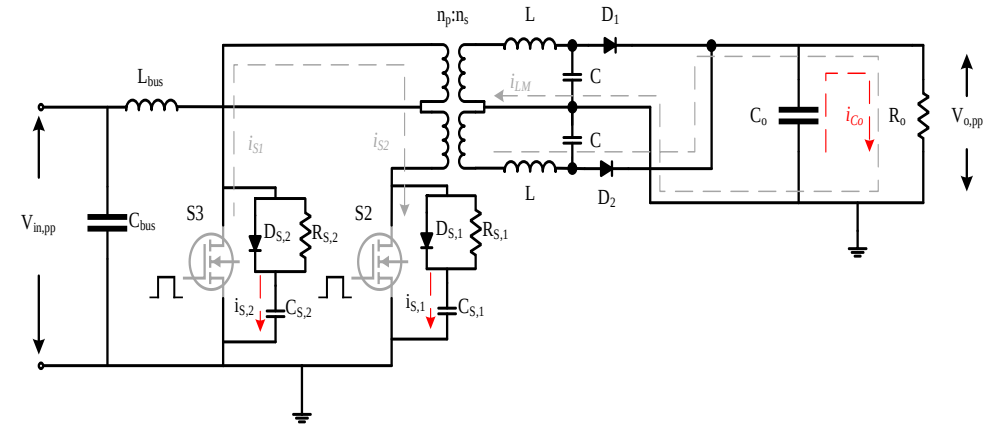
(b)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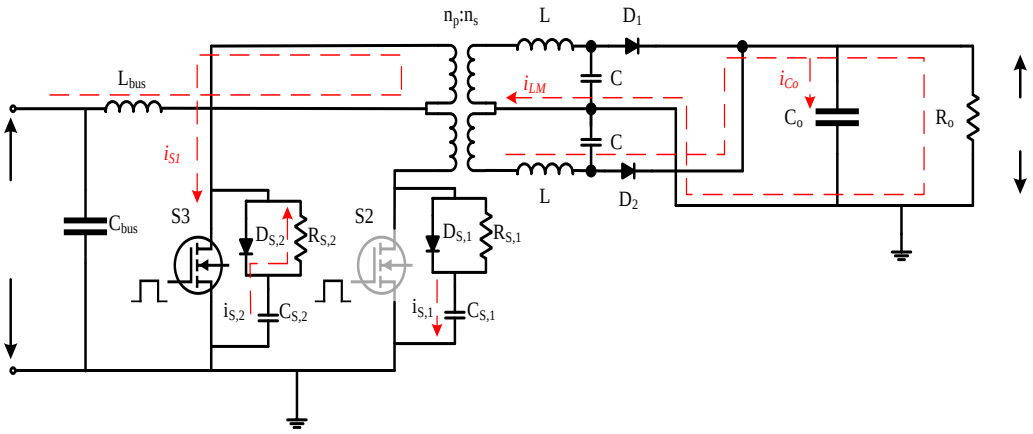
CS,2
iS,1
CS,1

(c)


np:ns
L
D1
Lbus
iLM
iS1
C
iCo
Co
Ro
C
L
D2
Cbus
S3
DS,2
RS,2
S2
DS,1
RS,1
iS,2
CS,2
iS,1
CS,1

(d)

Figure 4. The operation modes the push-pull side; (a) OFF-state of S2 and S3, (b) ON-state of S2 and OFF-state of S3, (c) OFF-state of S2 and S3, (d) OFF-state of S2 and ON-state of S3.

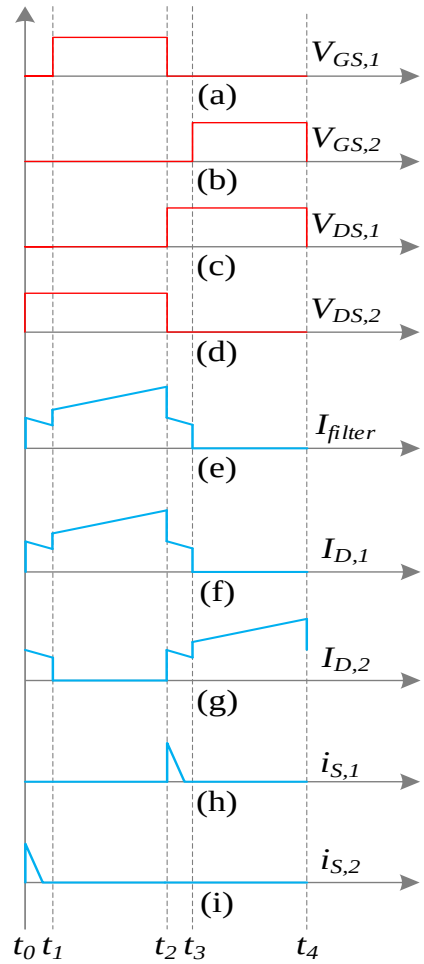


Figure 5. The waveform of the push-pull side; (a) the gate signal of S1, (b) the gate signal of S1, (c) the drain source voltage of S1, (d) the gate signal of S2, (e) the current pass through the filter at D1 side, (f) the current pass through D1, (g) the current pass through D2, (h) the snubber circuit current of S1 side, (i) the snubber circuit current of S2 side.

Time interval 2 ($t_1 \leq t \leq t_2$): At this interval, S2 is conducting and S3 is turned off. The input current passes through N_{p2} due to the ON state of switch S2. Thus, the secondary winding of the HF transformer is excited and current i_{Lr} flows through the series resonant inductance of the transformer. L_r resonates with the filter circuit. $C_{S,1}$ simultaneously discharges through $R_{S,1}$, while $C_{S,2}$ charges through $D_{S,2}$. The snubber circuit suppresses the high-frequency oscillation on the S1 started at $t = t_1$. i_{Lr} can be expressed as:

$$i_{Lr} = \frac{nV_{in,pp} - V_{out} - V_{LC}}{Z_r} \sin\left(\pi + w_{LC}(t - t_1)\right) \quad (12)$$

where,

$$w_{LC} = \frac{1}{\sqrt{LC}} \quad (13)$$

and

$$Z_r = R_o + jwL_r + jwL - j\frac{1}{wC}, (w = w_{LC}) \quad (14)$$

$$|Z_r| = \sqrt{{R_o}^2 + \left(w(L_r + L) - \frac{1}{wC}\right)^2} \quad (15)$$

Moreover, $i_{S,1}(t)$ and $i_{S,2}(t)$ can be defined in Equation 16 and Equation 17 given below:

$$i_{S,1}(t) \approx -\frac{V_{DS}}{R_{S,1}} \quad (16)$$

$$i_{S,2}(t) \approx \left(\frac{{C_{OSS}}' I_{pk}}{{C_{OSS}}' + C_{S,2}}\right)\left(1 - e^{-\frac{t}{T_{0,2}}}\right) \quad (17)$$

where,

$$T_{0,1} = R_{S,1}\frac{{C_{OSS}}' C_{S,1}}{{C_{OSS}}' + C_{S,1}} \quad (18)$$

and

$$T_{0,2} = R_{S,2}\frac{{C_{OSS}}' C_{S,2}}{{C_{OSS}}' + C_{S,2}} \quad (19)$$

Time interval 3 ($t_2 \leq t \leq t_3$): During this time interval, S2 and S3 are turned off. The voltage between the drain-source terminals of S2 is twice the input. The changing of i_{Lm} is given in (20). Moreover, the drain-source capacitance of S1 discharges.

Furthermore, $i_{s,1}$ and $i_{s,2}$ are given in (21) and (22).

$$i_{Lm} = \frac{nV_{in,pp}}{L_m}(t - t_0) - i_{Lm}(t_0) \quad (20)$$

$$i_{s,1} = i_{S,1}(t_2) - \left(\frac{C_{OSS}{}'I_{pk}}{C_{OSS}{}' + C_{S,1}}\right)\left(1 - e^{-\frac{t}{T_{0,1}}}\right) \quad (21)$$

$$i_{s,2} = i_{S,2}(t_2) - \left(\frac{C_{OSS}{}'I_{pk}}{C_{OSS}{}' + C_{S,2}}\right)\left(1 - e^{-\frac{t}{T_{0,2}}}\right) \quad (22)$$

Time interval 1 ($t_3 \leq t \leq t_4$): The operation of this time interval is analogous to the time interval 2. S2 is turned off and S3 is conducting. The input current passes through N_{p1}. Thus, the secondary winding of the transformer is excited and i_{Lr} flows through the series resonant inductance. L_r resonates with the filter circuit. $C_{S,1}$ simultaneously charges through $D_{S,1}$, while $C_{S,2}$ discharges through $R_{S,2}$. The snubber circuit suppresses the high-frequency oscillation on the S2 started at $t = t_3$. i_{Lr} can be given as:

$$i_{Lr} = \frac{nV_{in,pp} - V_{out} - V_{LC}}{Z_r}\sin\left(w_{LC}(t - t_3)\right) \quad (23)$$

Moreover, $i_{S,1}(t)$ and $i_{S,2}(t)$ can be defined as in Equation 24 and Equation 25 given below:

$$i_{S,1}(t) \approx \left(\frac{C_{OSS}{}'I_{pk}}{C_{OSS}{}' + C_{S,1}}\right)\left(1 - e^{-\frac{t}{T_{0,1}}}\right) \quad (24)$$

$$i_{S,2}(t) \approx -\frac{V_{DS}}{R_{S,2}} \quad (25)$$

where, Z_r , w_{LC} , $T_{0,1}$ and $T_{0,2}$ are mentioned previously in interval 2 and $T_{0,1} = T_{0,2}$.

3.3 Design considerations of the converter

The design phase is discussed in two main parts: the design of the boost side and the design of the push-pull side. The main purpose is to design a hybrid converter which has an input of $12V$ and an output of $\sim 400V$.

3.3.1 Design of the boost converter side of the proposed hybrid converter

In this subsection, a boost-type converter with an input voltage of $12V$ and an output voltage of $100V$ and has $500W$ output power capacity is designed and analyzed in simulation. In the context of the duty ratio of D equals to $1 - V_{out}/V_i = 0.5$, and the switching frequency of $40kHz$, from Hauke (2009), the main parameters and limitations of the designed boost converter can be determined as follows:

1. The boost side main inductor L_b is calculated as:

$$L_b{}^{maximum} = \left(\frac{V_{out}}{2f_{ws}\frac{P_o}{V_o}}\right)(D(1 - D)^2) \quad (26)$$

2. The boost side output capacitor $C_{o,1}$ is defined with the equation below:

$$C_{o,1}{}^{minimum} = \frac{P_{out}D}{f_{sw}\Delta V_{out}V_{out}} \quad (27)$$

where, ΔV_{out} is assumed as 0.1 V to avoid choosing too large capacity.

3. To define the limits of semiconductor switch, the maximum current is calculated as:

$$I_{sw}{}^{maximum} = \frac{\Delta i_L}{2} + \frac{I_{out}{}^{maximum}}{1 - D} \quad (28)$$

where

$$\Delta i_L = \frac{V_{in}{}^{minimum}D}{f_{sw}L_b} \quad (29)$$

and

$$I_{out}{}^{maximum} = \left(\frac{V_{out}}{2f_{sw}L_b}\right)(D(1-D)^2) \quad (30)$$

4. To select diodes, the forward currents of diodes must be equal to the $I_{out}{}^{maximum}$. So, the minimum forward currents of $I_{D,b}$ and $I_{D,2}$ are determined as:

$$I_{D,b}{}^{minimum} = I_{D,2}{}^{minimum} = I_{out}{}^{maximum} \quad (31)$$

The capacitor in RCD can absorb more energy due to the current flowing through the diode. Moreover, during the switching transients highest di/dt can be observed. Thus, the recovery characteristics of snubber diode D_S and the minimization of the stray inductances should be considered Sic MOSFET (2020). To determine the Cs, Rs and Ds, it is assumed that L_b is transferred all energy to Cs. The values of the components of the snubber circuit can be calculated from the expressions given below:

1. The value of the snubber capacitor Cs is determined as:

$$C_S > \frac{L_b I_{L,pk}}{{V_{DS^+}}^2 - {V_{out}}^2} \quad (32)$$

where,

$$V_{DS^+} = \frac{V_A e^{-\frac{a}{w}\left(\tan^{-1}\left(\frac{a}{w}\right)+\emptyset\right)}}{1+\frac{a}{w}} + V_{out}, \quad (33)$$

$$V_A = \sqrt{{V_{out}}^2 + \frac{a}{w}^2 \left(R_{off}I_{L,pk} - V_{out}\right)^2}, \quad (34)$$

$$\emptyset = \tan^{-1}\left(\frac{V_{out}}{\frac{a}{w}\left(R_{off}I_{L,pk} - V_{out}\right)}\right), \quad (35)$$

$$a = \frac{1}{R_{off}C_{OSS}}, \quad (36)$$

and

$$w = \frac{1}{\sqrt{L_b C_{OSS}}}\sqrt{1-\left(\frac{\sqrt{\frac{L_b}{C_{OSS}}}}{R_{off}}\right)^2} \quad (37)$$

R_{off} is the resistance of semiconductor switch while the switch is OFF state and generally very high (R_{off}~$4.10^9\Omega$). V_{DS^+} is the upper voltage value of oscillation of drain source voltage, V_A is oscillation voltage, $\emptyset$ is the phase angel between gate signal and drain source voltage, a is the oscillation frequency of semiconductor switch, w is the oscillation between the inductor and switch. The snubber resistor Rs is determined as:

$$R_S < \frac{-1}{f_{sw}C_S \ln\left(\frac{V_{DS^+} - V_S}{V_{DS^+}}\right)} \quad (38)$$

Here, V_s is the discharge voltage

($V_S = 0.9 \times V_{DS^+}$).

2. Any fast recovery diode is suitable for the design.

3.3.2 Design of the push-pull converter side

A push-pull-type converter with an input voltage of 100V and an output voltage of ~400 V with approximately $500W$ is designed and examined in this subsection. In the context of the signal with duty ratio of 0.45, and the switching frequency of 40 kHz, from Tai and Hwu (2023), the main components can be selected as the steps below:

1. The turn ratio of the HF transformers is determined as:

$$n = \frac{V_{out}^{minimum}}{2V_{in,pp}^{minimum} D^{maximum}} \quad (39)$$

In order to provide a hybrid converter design which is highly efficient, in the design procedure, the efficiency is targeted to be kept at 85% for push-pull side, $V_{in,pp}^{minimum} \geq (P_{out}/0.85)/(input\ current \times 2 \times D^{maximum})$, where, $input\ current = n(V_{out}/R_{load})$.

So, $V_{in,pp}^{minimum} \geq 79.88V$, $V_{out}^{minimum} \geq 323.53V$, and $D^{maximum} = 0.45$.

2. For choosing semiconductor switches, the voltage of drain source can be calculated by selecting 30% more than the input voltage, excluding the voltage increase caused by leakage inductance.

$$V_{DS} = 1.3 \times 2V_{in,pp}^{maximum} \quad (40)$$

So, the MOSFET with a breakdown voltage higher than $260V$ can be selected at $V_{in,pp}^{maximum} = 100V$.

3. The voltage of half-bridge diodes can be calculated as:

$$V_{diode} = nV_{in,pp}^{maximum} \quad (41)$$

$$I_{diode} = \frac{P_{out}^{maximum}}{V_{diode}} \quad (42)$$

where, $P_{out}^{maximum} = 1.1P_{out}$, $P_{out} = 500W$, thus, the diode with a reverse voltage higher than $475V$ and with a forward current higher than $1.05A$ can be selected.

4. The magnetizing inductance L_m is defined as:

$$L_m < \frac{T \times t_d}{8C_{sw}} \quad (43)$$

and $T = {}^{1}/_{f_{sw}}$, $t_d = 2.5\mu s$.

5. The parallel resonant capacitance of the filter circuit is defined as:

$$C = \frac{1}{2\pi f_r R_{ac} Q} \quad (44)$$

The switching frequency over the resonant frequency reduces the output voltage. The output voltage can be increased by minimizing Q. However, the frequency range converges to the resonant frequency at a small Q value of the gain. In this case, the converter also operates in DCM (discrete conduction mode). To eliminate this problem, the Q value should be at a value that obtains the output voltage to provide the switching frequency while ensuring ZVS (Ngo, 1987; Murai and Lipo, 1992; Erickson and Maksimović, 2020). Thus, for the ZVS condition to be met, f_{sw} must be higher then f_r (Salem et al., 2018).

$$Q = \frac{Z_o}{R_o},\ Z_o = \sqrt{\frac{(L_r+L)}{C}} \quad (45)$$

and

$$R_{ac} = \frac{8}{\pi^2}R_o = \frac{8}{\pi^2}\frac{V_{out}}{I_{out}} \quad (46)$$

6. The series resonant inductance $(L_r + L)$ is defined as:

$$L_r + L = \frac{1}{(2\pi f_r)^2 C} \quad (47)$$

4. The Simulation of The Converter

The proposed hybrid converter is analyzed using MATLAB Simulink to verify the mathematical analysis. The converter's parameters are given in Table 1. The current and voltage waveforms of the boost topology which is the first part of the proposed hybrid converter are shown in Figure 6. The current and voltage waveforms obtained from the push-pull circuit of the proposed hybrid converter are shown in Figure 7. The switching voltage for the gate signal of the MOSFETs is applied as $12V$.

Table 1. The specification of the parameters.

Parameter	Symbol	Specification
Input voltage	V_{in}	~12V
Output voltage	V_{out}	~400V
Output power	P_o	~500W
Switching frequency	f_{sw}	40kHz
Duty cycle	D	~0.45
Turns ratio	$n_{p,1}:n_{p,2}:n_s$	10:10:45
Magnetization inductance	L_m	1mH
Boost side inductor	L_b	850µH
Boost side output capacitor	$C_{o,1}$	220µF
Boost side constant resistor	$R_{L,1}$	22kΩ
Boost side snubber resistor	R_S	33kΩ
Boost side snubber capacitor	C_S	0.47µF
Snubber resistor of S2	$R_{S,1}$	270Ω
Snubber capacitor of S2	$C_{S,1}$	0.33µF
Snubber resistor of S3	$R_{S,2}$	270Ω
Snubber capacitor of S3	$C_{S,2}$	0.33µF
Input filter inductor	L_{in}	2.5µH
Input filter capacitor	C_{in}	10µF
Output filter inductor (both side)	L	44µH
Output filter capacitor (both side)	C	0.1µF
Output capacitor	C_o	100µF
Constant output resistor	R_o	220Ω

Figure 6 points out V_{GS}, V_{DS}, $V_{L,b}$, $V_{o,b}$, i_L, i_S , $I_{D,b}$ and $I_{o,b}$. Note that the initial switching moment is ignored and S1 is turned on with the ZVS method. Figure 6 (b) shows that the drain-source terminal voltage is about $100V$. Thus, the source provides a current of slightly over $100A$ as seen in Figure 6 (c). The snubber circuit connected to the switches prevented the high-frequency oscillation on the MOSFET and minimized the voltage stress over the drain-source terminal. It is seen in Figure 6 (d), that the snubber circuit draws low current and reduces the oscillation. Then, the snubber capacitance immediately discharged to approximately 0V through the snubber resistance at the beginning of the ON state interval. Figure 6 (e) and (f) show the inductance voltage and main diode current, respectively

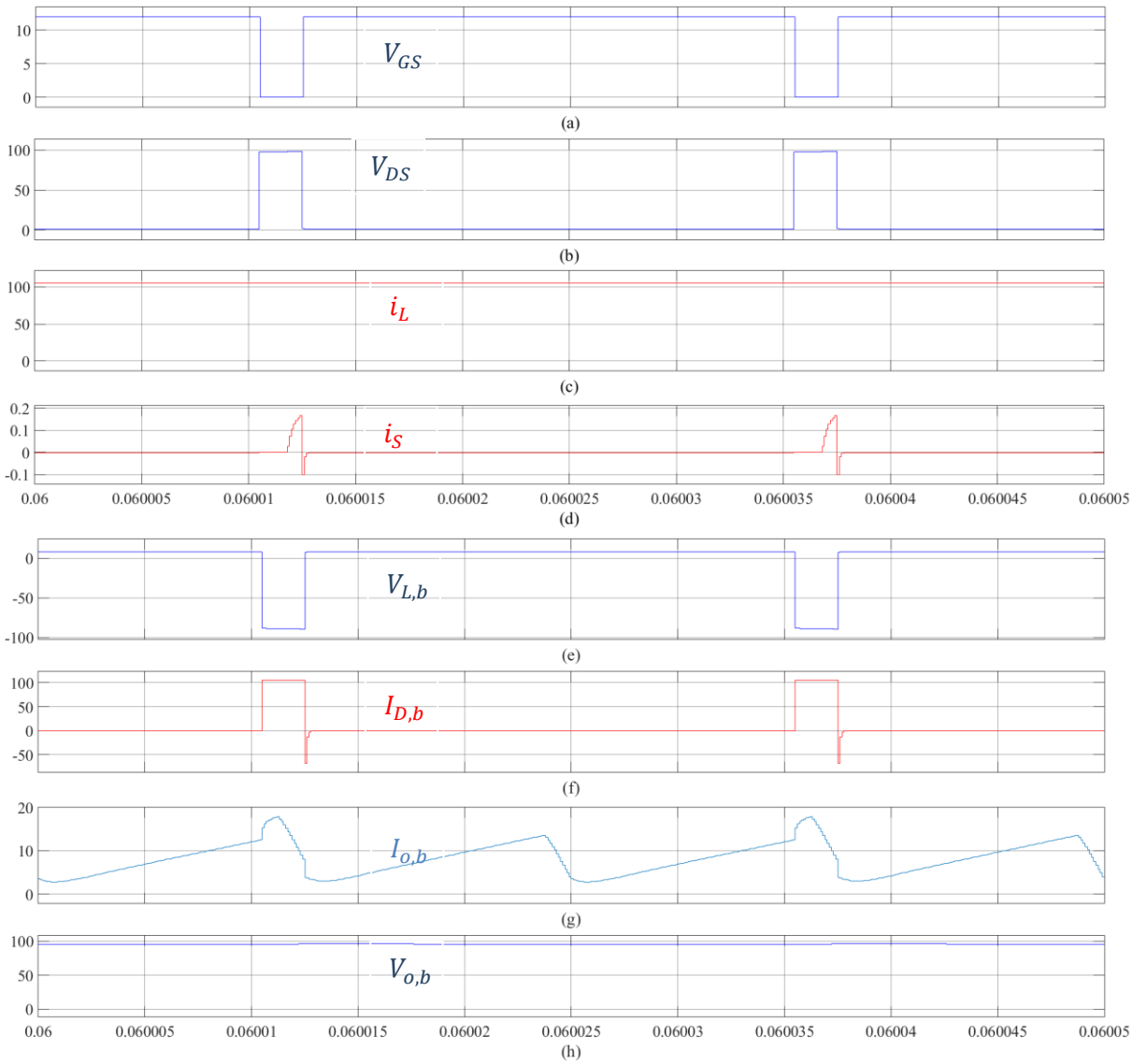
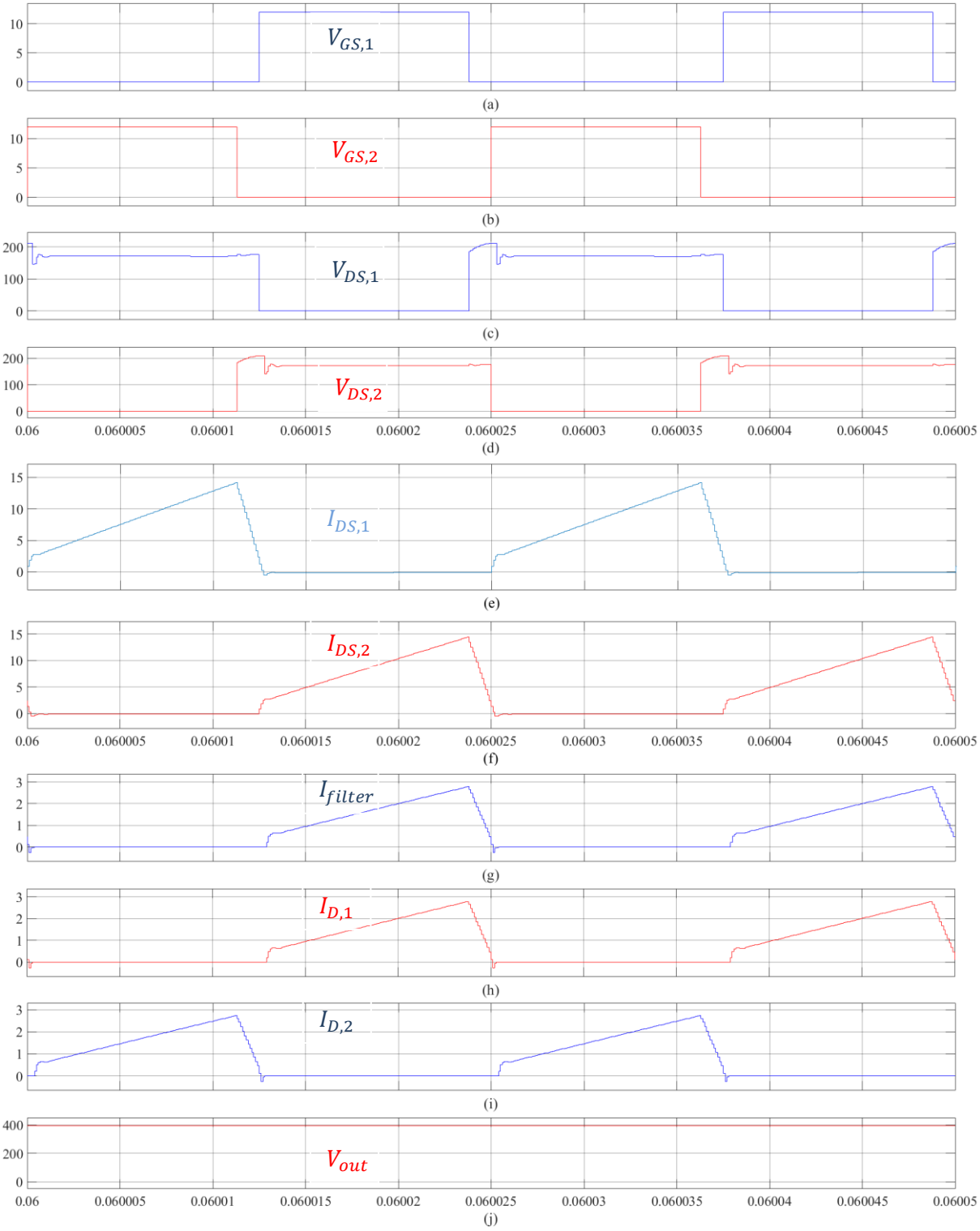


Figure 6. The boost side current and voltage waveforms. (a) the waveform of V_{GS}, (b) the waveform of V_{DS}, (c) the waveform of i_L, (d) the waveform of i_S, (e) the waveform of $V_{L,b}$, (f) the waveform of $I_{D,b}$, (g) the waveform of $I_{o,b}$, (h) the waveform of $V_{o,b}$.

It can be seen in Figure 6 (g) that the boost side output current fluctuates due to the value of the push-pull side inductance. Although this situation is expected, the ripple of the output current is increased due to the low inductive value. If the inductance value is selected as large enough, the voltage oscillation of the push-pull side switches increases. The necessity of this inductance is stated below. It can be seen in Figure 6 (h) that the boost side output voltage is about $100V$ As seen in Figure 7(a) and (b), the duty cycle ratio is selected as 0.45 and a dead time interval is allowed between the turn-on and turn-off states of the MOSFETs. Thus, the saturation of the HF transformer can be reduced. Figure 7(c) and (d) show the drain-source terminal voltage of switches S1 and S2, respectively. The drain-source terminal voltages are equal to approximately $2V_{in,pp}$. Since the LC filters connected to the HF transformer output are equivalent, the current of only one filter is shown in Figure 7 (e). Figure 7 (f), (g) and (h) show the currents passed through the diodes and the output voltage of

the proposed converter, respectively. As a result, the output voltage is obtained as approximately $400V$.



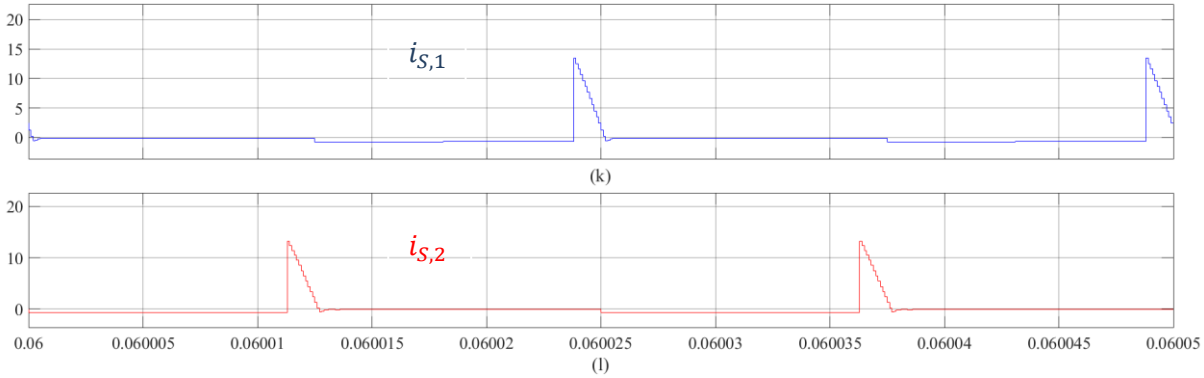


Figure 7. The push-pull side current and voltage waveforms. (a) the waveform of $V_{GS,1}$, (b) the waveform of $V_{GS,2}$, (c) the waveform of $V_{DS,1}$, (d) the waveform of $V_{DS,2}$, (e) the waveform of $I_{DS,1}$, (f) the waveform of $I_{DS,2}$, (g) the waveform of I_{filter}, (h) the waveform of $I_{D,1}$, (i) the waveform of $I_{D,2}$, (j) the waveform of V_{out}, (k) the waveform of $i_{S,1}$, (l) the waveform of $i_{S,2}$.

Converter efficiency at different duty cycles for the boost side is given in Table 2. At a duty cycle of 0.85, the converter exhibits an efficiency of approximately 72%. Although the proposed converter can achieve a maximum efficiency of up to 92% on the boost side, in practical applications, the efficiency tends to decrease due to losses in the inductor typically present in boost converters. It can be seen from Equation 48 that the resistance of the inductor r_L reduces efficiency. The voltage gains and efficiency characteristics of conventional boost converters considered in practical applications are illustrated in Figure 8 (Hart, 2011). As shown in Figure 8(a), the voltage gain is higher when the duty cycle is around 0.85. Moreover, Figure 8(b) indicates that the efficiency is higher within the duty cycle range of 0.8–0.9.

$$\eta = \frac{1}{1 + r_L R_{load}(1-D)^2} \qquad (48)$$

where, η is the efficiency, R_{load} is the load resistance

Table 2. The efficiency analysis for different duty ratios of boost side.

Duty Cycle	P_i(W)	Boost Side Output Power P_o(W) (W)	V_o(V)	η_{boost}(%)	$\eta_{pushpull}$(%)	η(%)
0.1	59.11	50.33	9.01	53.85	85.1463	17.8820	15.2259
0.2	76.15	66.26	12.01	61.4	87.0125	18.1105	15.7584
0.3	101	89.03	15.77	71	88.1485	17.7131	15.6139
0.4	139.9	127.79	22.01	84.12	91.3438	17.2236	15.7327
0.5	208.47	187.99	33.08	102.94	90.1760	17.5967	15.8680
0.6	325.62	296.87	54.66	129.26	91.1707	18.4121	16.7864
0.7	548.81	501.9	194.74	174.2	91.4524	38.8006	35.4840
0.8	627.01	576.36	416.45	264.08	91.9220	72.2552	66.4184
0.85	690.22	638.5	492.11	360.05	92.5067	77.0728	71.2976
0.9	807.92	742.64	495.12	401.23	91.9200	66.6703	61.2833

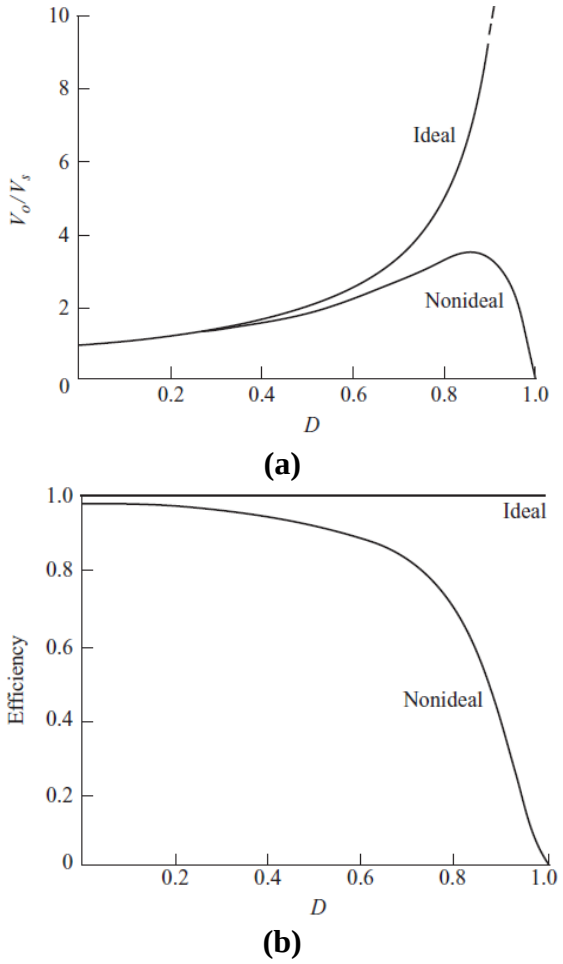


Figure 8. Boost converter for a nonideal inductor. (a) Output voltage; (b) Boost converter efficiency.

In Figure 9, output power, output current ripple, ripple voltages on switches and maximum output voltage changes are analyzed using different duty cycles. It should be noted that the values in the figure are given as per unit ($p.u.$). The proposed hybrid converter operates more stable with D= 0.45 and provides higher power to the load. Moreover, with the duty-cycle of D=0.45, less output current ripple and lower voltage stress are observed between drain-source terminals of switches. However, it is provided that a voltage above 400 V at the output of the converter with the duty-cycle of D=0.48 since approximately 400V output voltage is obtained from the converter when the duty-cycle of the switching period is taken as at D=0.45. With this output voltage, the proposed converter provides approximately 500W output power. With the proposed hybrid converter, it is achieved that the operation performance with less than 1% output current ripple and 0.5080 $p.u.$ voltage ripple occuring between drain-source terminals of switch S1. In addition, during the operation with the duty-cycle of D = 0.45 there is a voltage ripple of 0.4454 $p.u.$ measured from between the drain-source terminals of S2 and S3 switches and thus it can be concluded that lower voltage stress is generated on the switches S1, S2 and S3 rather than the case of operating the duty-cycle D=0.48. Moreover, Table 3 shows the output voltage, power, and efficiency at different duty cycles for push-pull side. The output voltage and load current waveforms of the proposed hybrid converter are given in Figure 10 and Figure 11. and these figures show the effectiveness of the proposed converter.

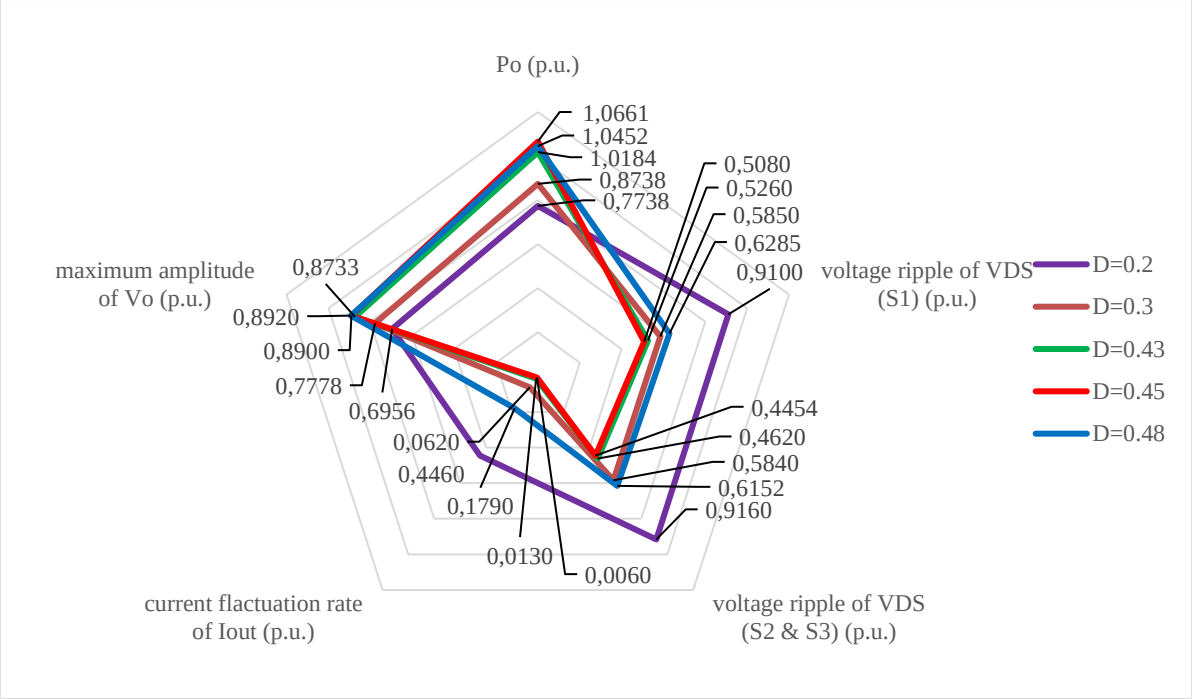


Figure 9. The changing of the output power, the output current ripple, the ripple voltages on switches and the maximum output voltage at various duty cycles.

Table 3. The efficiency analysis for different duty ratios of push-pull side.

Duty Cycle	**fluctuation rate of I_{out}** (%)	**Voltage ripple of S1** (%)	**Voltage ripples of S2&S3** (%)	V_o(V)	P_o(W)	$\eta_{pushpull}$(%)
0.2	44.60	91.00	91.60	306.0642	371.4244	57.1415
0.3	6.20	58.50	58.40	384.2517	419,4241	64.5268
0.43	1.30	52.60	46.20	342.2320	488.8320	75.2049
0.45	0.60	50.80	44.54	391.5987	511.7280	78.7274
0.48	17.90	62.85	61.52	392.4805	501.6960	77.1840

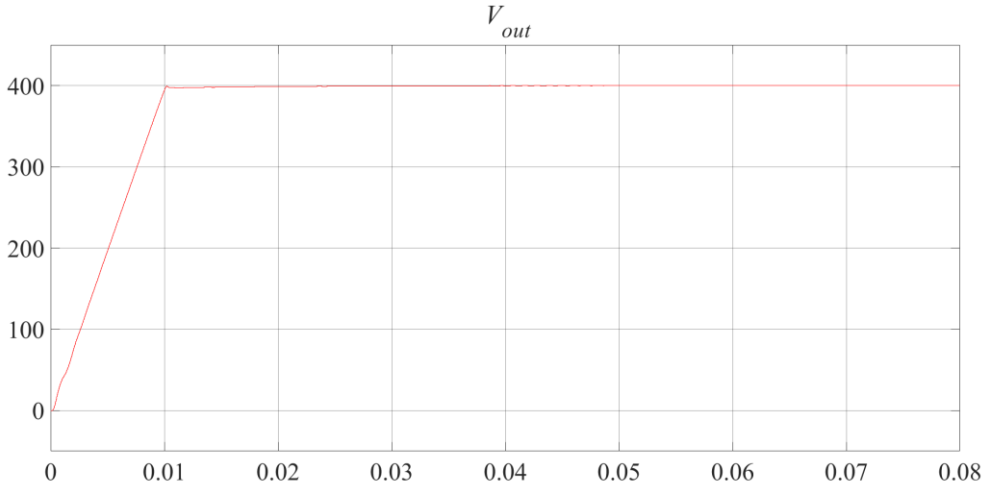


Figure 10. Output voltage of proposed converter.

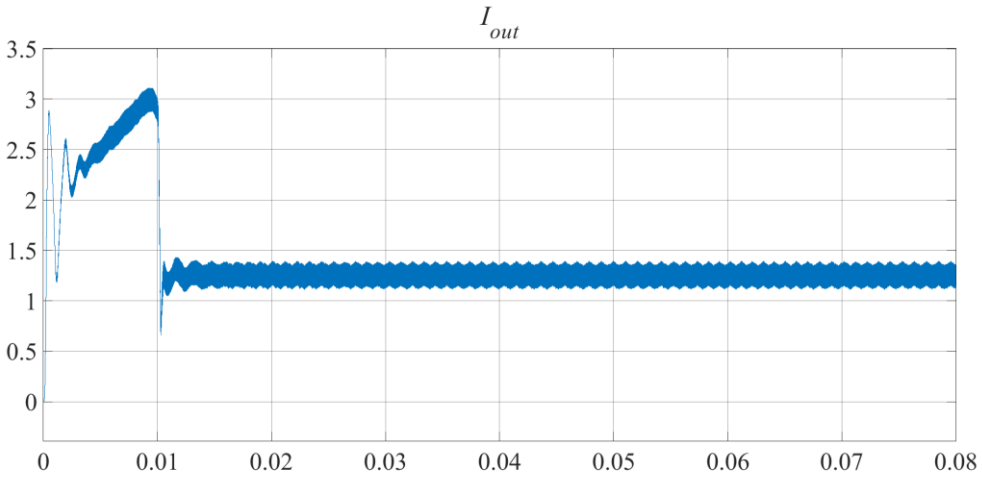


Figure 11. Output current of proposed converter.

Also, the efficiency of the proposed converter is compared to other converter topologies that existed in literature. The results of the comparison are given in Table 4.

Table 4. The comparison of the main parameters.

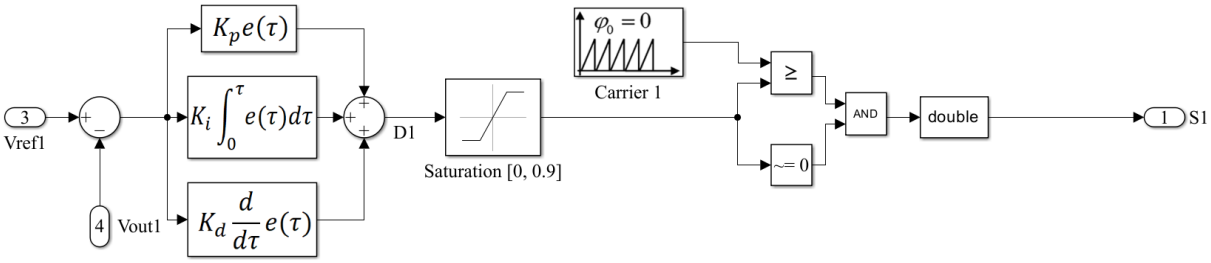
Converter	Number of Switches	Switching Loss	Voltage Stress of Switches	Voltage Gain	Number of Capacitor	Number of Inductor, Coupled Inductor, and transformers	Number of Diode
Luo-Boost [K]	2	Low	$\frac{V_o}{2n+D+3}$	$\frac{2n+D+3}{1-D}$	4	3	3
Three Phase Parallel Boost Converter [N]	3	Low	for S1: $\frac{V_i}{D}$ for S2, S3: $\frac{V_i}{1-D}$	$\frac{3D+D^2+n(1-D)}{D(1-D)}$	4	4	3
Quadratic Boost Converter [H]	2	Low	for S1: $\frac{V_i}{1-D}$ for S2: $\frac{V_i}{(1-D)^2}$	$\frac{1+n(2-D)^2}{(1-D)^2}$	6	3	5
Hybrid Converter [D]	4	Low	-	$\frac{1}{1-KD}$, $K=\frac{L_1+L_3}{L_3-L_2}$	4	3	2
Boost-Luo [E]	1	Low	$\frac{V_o}{3+2n_2+n_3}$	$\frac{3+2n_2+n_3}{1-D}$	5	1	5

Interleaved Boost [L]	2	Low	$\frac{(2-D)V_i}{(1-D)^2}$	$\frac{1+n(1-D)}{(1-D)^2}$	4	3	4
Phase-Shifted Hybrid Converter [G]	4	Low	nV_i	$\left(\frac{n_1}{4}(1+2D)\left(1+\frac{1}{D}\sqrt{D^2+\frac{4A}{Vi}(D-0.5)+\frac{8A^2}{V_i^2}}\right)\right)n_1+0.5n_2,$ $A=nL_{leakage}I_of_s$	3	4	10
Proposed Converter	3	Low	for S1: $\frac{V_i}{1-D}$ for S2, S3: $\frac{V_o}{n}$	$\frac{n}{(1-D_1)(1-D_2)}$	4	3	4

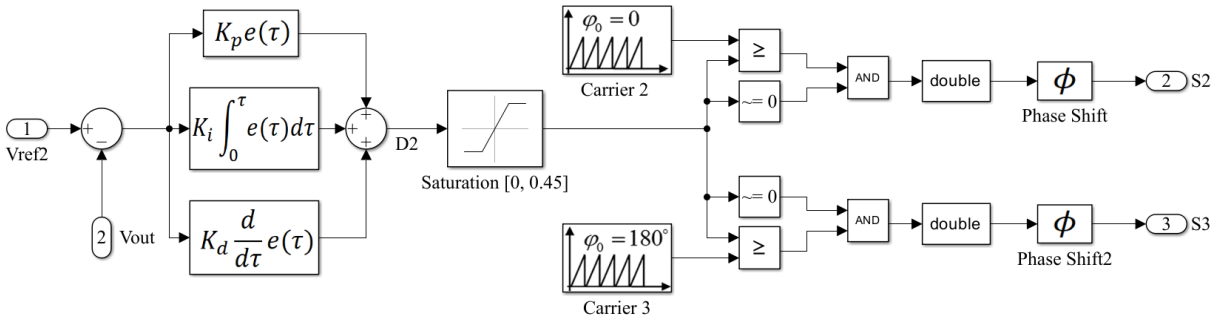
* n and n_i $\{i = 1,2,3\}$ are the turn ratios, D is the duty ratio.

5. Design of The Controller

The proposed hybrid converter comprises three semiconductor switches, which are controlled using the Pulse Width Modulation (PWM) technique. Through this method, the output voltage can be regulated and maintained at a desired constant value by adjusting the duty cycle of the PWM signal. The control strategy involving the PWM signal and duty cycle is illustrated in Figure 12. As shown in Figure 12(a), to maintain a constant output voltage on the boost side, V_{out1} is subtracted from a reference voltage V_{ref1}. Simultaneously, in Figure 12(b), to ensure voltage regulation on the push-pull side, V_{out} is subtracted from another reference voltage V_{ref2}. The resulting error signals in both cases are fed into PID control blocks. Subsequently, the output signals from the PID blocks are limited by a saturation block, and the constrained signals are compared with a carrier signal at the switching frequency in the corresponding comparator blocks. As a result, PWM signals are generated, which are then used to control the semiconductor switches.



(a)



(b)

Figure 12. PID controller for the control strategy; (a) PID controller of boost side, (b) PID controller of push-pull side.

The parameters of the PID controller for the transfer function are given as below:

$$K_p + \frac{K_i}{s} + K_d s = 10 + \frac{0.001}{s} + 3s \quad (49)$$

where, K_p is proportional constant, K_i is the intergral constant and K_d is the derivative constant.

6. Conclusions

In this study, a hybrid DC-DC converter design including boost and push-pull converter topologies is proposed with the purpose of operation with the load of required approximately 500W medium power. The proposed hybrid converter is designed by a cascade structure in which the DC bus voltage of the push-pull converter is regulated and boosted with a DC-DC boost converter. The novel hybrid converter is implemented in simulation the performance tests are realized in simulation. With the proposed hybrid converter, it is aimed to reduce the voltage stress that may occur on semiconductor switching devices placed on the converter hardware. It is observed that the voltage stresses and the peak voltages that occur between the terminals of the switches and increase related to the operation voltage are significantly reduced with the proposed novel hybrid converter. Thus, the difficulty of the converter design, including the HF transformer, is also alleviated. Furthermore, by reducing the transformer turn ratio, eddy current and core (hysteresis) losses are significantly minimized. The determined parameters of the proposed hybrid converter are analyzed, and it is seen from the simulation results that the proposed hybrid converter operates stable with these parameters. The duty-cycle of the boost side switch is determined as D=0.85 while the push-pull side switches are D=0.45. With these conditions, the proposed converter provides 400V output voltage. An LC filter composed of a leakage inductance L_{bus} and capacitor C_{bus} is used on the primary side of the transformer. In this way, the ripple of the output current of the boost converter reduces. In addition, an external LC filter circuit is used on the secondary side of the HF transformer in order to reduce the losses that arise from the ZVS switching on the primary side of the HF transformer and the ZCS switching on the secondary side. As a result, the switches have soft switching that allows operation at high frequencies. Thus, the losses of the switches can be reduced. The proposed hybrid topology provides a high-power density and has a compact structure. The

proposed topology can be used in various applications such as energy storage in power systems, maximum power point tracking part of the photovoltaic system and uninterruptible power supply. The future studies will be on the real-time implementation and performance tests of the proposed novel hybrid converter under different load conditions. Also, the converter will be improved in the context of higher power density.

Author contribution

All studies for the article, such as material procurement, data collection, data processing, literature review, writing, and critical review, were carried out by Hamza YAPICI and Remzi INAN.

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Conflict of Interest Statement

The author(s) declare that they have no conflict of interest.

Ethical standards

No Ethics Committee Approval is required for this study

References

Aguilar, C., Canales, F., Arau, J., Sebastián, J., Uceda, J. (1997). An integrated battery charger/discharger with power-factor correction. *IEEE Transactions on Industrial Electronics*, 44(5), 597-603. https://doi.org/10.1109/41.633453

Alizadeh, D., Babaei, E., Sabahi, M., Cecati, C. (2024). Hybrid interleaved DC-DC step-up converter based on coupled inductor. *International Journal of Circuit Theory and Applications*, 52(6), 2655-2685. http://doi.org/10.1002/cta.3873

Anitha, P., Kumar, K.K., Kamaraja, A.S. (2023). An improved design and performance enhancement of Y-source DC-DC boost combined phase shifted full bridge converter for electric vehicle battery charging applications. *Journal of Electrical Engineering and Technology*, 18(4), 2983-2996. http://doi.org/10.1007/s42835-023-01414-1

Belhimer, S., Haddadi, M., Mellit, A. (2018). A novel hybrid boost converter with extended duty cycles range for tracking the maximum power point in photovoltaic system applications. *International journal of hydrogen energy*, 43(14), 6887-6898. http://doi.org/10.1016/j.ijhydene.2018.02.136

Boonyaroonate, I., Mori, S. (2002, March). A new ZVCS resonant push-pull DC/DC converter topology. *In APEC 7th Annual IEEE Applied Power Electronics Conference and Exposition*, 10-14 March 2002, Dallas, TX, USA.

Chen, Z., Wu, Q., Yuan, Y. (2016). A novel zero-voltage-switching push–pull high-frequency-link single-phase inverter. *IEEE Journal of Emerging and Selected Topics in Power Electronics*, 4(2), 421-434. http://doi.org/10.1109/JESTPE.2015.2505171

Choe, G.Y., Kim, J. S., Lee, B.K., Won, C.Y., Lee, T.W. (2010). A Bi-directional battery charger for electric vehicles using photovoltaic PCS systems. *In 2010 IEEE Vehicle Power and Propulsion Conference*, 01-03 September 2010, Lille, France.

Choi, S.W., Oh, S.T., Kim, M.W., Lee, I.O., and Lee, J.Y. (2020). Interleaved isolated single-phase PFC converter module for three-phase EV charger. *IEEE Transactions on Vehicular Technology*, 69(5), 4957-4967.

http://doi.org/10.1109/TVT.2020.2980878

Chu, C.L., Li, C.H. (2009). Analysis and design of a current-fed zero-voltage-switching and zero-current-switching CL-resonant push–pull dc–dc converter. *IET power electronics*, 2(4), 456-465. http://doi.org/10.1049/iet-pel.2008.015

Costa, P.J.S., Ewerling, M.V.M., Font, C.H.I., Lazzarin, T.B. (2020). Unidirectional three-phase voltage-doubler SEPIC PFC rectifier. *IEEE Transactions on Power Electronics*, 36(6), 6761-6773. http://doi.org/10.1109/TPEL.2020.3037480

Elsayad, N., Moradisizkoohi, H., Mohammed, O. A. (2019). A single-switch transformerless DC-DC converter with universal input voltage for fuel cell vehicles: analysis and design. *IEEE Transactions on vehicular technology*, 68(5), 4537-4549. http://doi.org/10.1109/TVT.2019.2905583

Elserougi, A., Abdelsalam, I., Massoud, A. (2022). An isolated-boost-converter-based unidirectional three-phase off-board fast charger for electric vehicles. *IET Electrical Systems in Transportation*, 12(1), 79-88. http://doi.org/10.1049/els2.12039

Erickson, R.W., Maksimović, D. (2020). Resonant conversion. *Fundamentals of power electronics*. ISBN: 978-3-030-43879-1, Cham: Springer International Publishing.

Gallardo-Lozano, J., Milanés-Montero, M.I., Guerrero-Martinez, M.A., Romero-Cadaval, E. (2011). Three-phase bidirectional battery charger for smart electric vehicles. *In 2011 7th International Conference-Workshop Compatibility and Power Electronics (CPE)*, 01-03 June 2011, Tallinn, Estonia.

Garcia, O., Zumel, P., De Castro, A., Cobos, A. (2006). Automotive DC-DC bidirectional converter made with many interleaved buck stages. *IEEE transactions on power electronics*, 21(3), 578-586. http://doi.org/10.1109/TPEL.2006.872379

Gopalasami, R., Chokkalingam, B., Muthusamy, S. (2023). A novel method for hybridization of super lift luo converter and boost converter for electric vehicle charging applications. *Energy Sources, Part A: Recovery, Utilization, and Environmental Effects*, 45(3), 8419-8437. http://doi.org/10.1080/15567036.2023.2226104

Hart, D.W., and Hart, D.W. (2011). *Power electronics* (Vol. 166). New York: McGraw-Hill.

Hassan, W., Lu, D.D.C., Xiao, W. (2019). Single-switch high step-up DC–DC converter with low and steady switch voltage stress. *IEEE Transactions on Industrial Electronics*, 66(12), 9326-9338. http://doi.org/10.1109/TIE.2019.2893833

Hauke, B. (2009). Basic calculation of a boost converter's power stage. *Texas Instruments, Application Report* November, 1-9.

Hussein, B., Abdi, N., Massoud, A. (2021). Development of a three-phase interleaved converter based on SEPIC DC–DC converter operating in discontinuous conduction mode for ultra-fast electric vehicle charging stations. *IET Power Electronics*, 14(11), 1889-1903. http://doi.org/10.1049/pel2.12157

Jalbrzykowski, S., Citko, T. (2013). Push-pull resonant DC-DC isolated converter. *Bulletin of the Polish Academy of Sciences Technical Sciences*, 61(4), 763-769. http://doi.org/10.2478/bpasts-2013-0082

Jeong, H.W., and Lim, C.Y. (2024). Hybrid DC–DC Converter with novel clamp circuit in wide range of high output voltage. *IEEE Access*, 12, 7775-7785.

http://doi.org/10.1109/ACCESS.2024.3352443

Jiang, L., Wan, J., Li, Y., Huang, C., Liu, F., Wang, H., Sun, Y., Cao, Y. (2021). A new push-pull DC/DC converter topology with complementary active clamped. *IEEE Transactions on Industrial Electronics*, 69(6), 6445-6449. http://doi.org/10.1109/TIE.2021.3088357

Karimi, K., Babaei, E., Karimi, M., Alizadeh, D., and Mousavi, S.M.J. (2024). An interleaved high step-up DC–DC converter based on coupled-inductor. *IET Power Electronics*, 17(3), 473-485. http://doi.org/10.1049/pel2.12662

Knabben, G.C., Scähfer, J., Kolar, J.W., Zulauf, G., Kasper, M.J., Deboy, G. (2020). Wide-input-voltage-range 3 kW dc-dc converter with hybrid LLC and boundary/discontinuous mode control. *In 2020 IEEE Applied Power Electronics Conference and Exposition (APEC)*, 15-19 March 2020, New Orleans, LA, USA.

Kumar, M.A.B., Krishnasamy, V. (2022). Enhanced quadratic boost converter based on voltage lift technique for fuel cell powered electric vehicle. *Computers and Electrical Engineering*, 102, 108256. http://doi.org/10.1016/j.compeleceng.2022.108256

Larico, H.R.E., Barbi, I. (2011). Three-phase push–pull DC–DC converter: Analysis, design, and experimentation. *IEEE Transactions on Industrial Electronics*, 59(12), 4629-4636. http://doi.org/10.1109/TIE.2011.2177609

Lee, C.S., Jeong, J.B., Lee, B.H., Hur, J. (2011). Study on 1.5 kW battery chargers for neighborhood electric vehicles. In 2011 *IEEE Vehicle Power and Propulsion Conference* (pp. 1-4). IEEE. http://doi.org/10.1109/VPPC.2011.6043129

Li, H., Zhang, Y., Zhao, Q., Li, Y., Zhao, J., Cheng, X.F., and Li, T. (2024). An ultra-high gain boost converter with low switching stress for integrated multi-energy storage systems. *Scientific Reports*, 14(1), 22513. http://doi.org/10.1038/s41598-024-73208-y

Liu, Y., Jayathurathnage, P., Kyyrä, J. (2023). A new simplified method and design guidelines for the optimization of push–pull class $\phi 2$ converters for wireless power transfer applications. *IEEE Transactions on Power Electronics*, 38(8), 10442-10459. http://doi.org/10.1109/TPEL.2023.3272840

Maheswari, E., Kommula, B.N., Rajesh, K., and Sharma, S. (2025). Optimized maximum power point tracking for PV fed hybrid DC-DC converter-based BLDC motor driven electric vehicles. *Electrical Engineering*, 107(1), 965-986. http://doi.org/10.1007/s00202-024-02561-y

Manjrekar, M.D., Steimer, P.K., Lipo, T.A. (2000). Hybrid multilevel power conversion system: A competitive solution for high-power applications. *IEEE transactions on industry applications*, 36(3), 834-841. http://doi.org/10.1109/IAS.1999.805943

Mukkapati, A.B.K., Krishnasamy, V., Kaur, R. (2020). Genetic algorithm assisted fixed frequency sliding mode controller for quadratic boost converter in fuel cell vehicle. *IET Electrical Systems in Transportation*, 10(1), 81-88. http://doi.org/10.1049/iet-est.2019.0015

Murai, Y., Lipo, T.A. (1992). High-frequency series-resonant DC link power conversion. *IEEE transactions on industry applications*, 28(6), 1277-1285. http://doi.org/10.1109/28.175278

Musavi, F., Edington, M., Eberle, W., Dunford, W.G. (2011). Evaluation and efficiency comparison of front end AC-DC plug-in hybrid charger topologies. *IEEE Transactions on Smart grid*, 3(1), 413-421. http://doi.org/10.1109/TSG.2011.2166413

Muthusamy, K., Muthusamy, M., Kaur, R., Krishnasamy, V. (2021). An intelligent hybrid interfacing converter of fuel cell powered telecom loads for efficient power conversion. *Computers and Electrical Engineering*, 90, 106941. http://doi.org/10.1016/j.compeleceng.2020.106941

Ngo, K.D. (1987). Analysis of a series resonant converter pulsewidth-modulated or current-controlled for low switching loss. *IEEE Transactions on Power Electronics*, 3(1), 55-63. http://doi.org/10.1109/63.4331

Ni, L., Patterson, D.J., Hudgins, J.L. (2011). High power current sensorless bidirectional 16-phase interleaved DC-DC converter for hybrid vehicle application. *IEEE Transactions on Power electronics*, 27(3), 1141-1151. http://doi.org/10.1109/TPEL.2011.2165297

Parvari, R., Zarghani, M., Kaboli, S. (2018). RCD snubber design based on reliability consideration: A case study for thermal balancing in power electronic converters. *Microelectronics Reliability*, 88, 1311-1315. http://doi.org/10.1016/j.microrel.2018.06.072

Qin, L., Zhen, L., Sun, Q., Zheng, S., and Li, J. (2025). Soft-switching high step-up DC-DC converter based on active switched-inductor units. *Journal of Electrical Engineering and Technology*, 1-18. http://doi.org/10.1007/s42835-025-02175-9

Sadaf, S., Bhaskar, M.S., Meraj, M., Iqbal, A., Al-Emadi, N. (2020). A novel modified switched inductor boost converter with reduced switch voltage stress. *IEEE Transactions on Industrial Electronics*, 68(2), 1275-1289. http://doi.org/10.1109/TIE.2020.2970648

Salem, M., Jusoh, A., Idris, N.R.N., Das, H.S., Alhamrouni, I. (2018). Resonant power converters with respect to passive storage (LC) elements and control techniques–An overview. *Renewable and Sustainable Energy Reviews*, 91, 504-520. http://doi.org/10.1016/j.rser.2018.04.020

Sassi, H.B., Errahimi, F., Essbai, N., Alaoui, C. (2019). V2G and Wireless V2G concepts: State of the Art and Current Challenges. *In 2019 International Conference on Wireless Technologies, Embedded and Intelligent Systems (WITS)*, 03-04 April 2019, Fez, Morocco.

Shanthi, T., Prabha, S.U., Sundaramoorthy, K. (2021). Non-isolated n-stage high step-up DC-DC converter for low voltage DC source integration. *IEEE Transactions on Energy Conversion*, 36(3), 1625-1634. http://doi.org/10.1109/TEC.2021.3050421

Shoyama, M., Harada, K. (1993). Zero-voltage-switching realized by magnetizing current of transformer in push-pull current-fed dc-dc converter. *In Proceedings of IEEE Power Electronics Specialist Conference-PESC'93*, 20-24 June 1993, Seattle, WA, USA

SiC MOSFET. (2020). Snubber circuit design methods. *ROHM Semiconductor, Application Note*, 1-7.

Singh, B., Singh, B.N., Chandra, A., Al-Haddad, K., Pandey, A., Kothari, D.P. (2004). A review of three-phase improved power quality AC-DC converters. *IEEE Transactions on industrial electronics*, 51(3), 641-660. http://doi.org/10.1109/TIE.2004.825341

Sree, K.R., Rathore, A.K. (2016). Analysis and design of impulse-commutated zero-current-switching single-inductor current-fed three-phase push–pull converter. *IEEE Transactions on Industry Applications*, 53(2), 1517-1526. http://doi.org/10.1109/TIA.2016.2626248

Tai, Y.K., Hwu, K.I. (2023). A novel ZVS/ZCS push-pull LC resonant dc-dc converter for energy sources. *Energies*, 16(6),

2892. http://doi.org/10.3390/en16062892

Tandon, S., Rathore, A.K. (2021). Analysis and design of series LC partial-resonance-pulse-based ZCS current-fed push-pull converter. *IEEE Transactions on Industry Applications*, 57(4), 4232-4241. http://doi.org/10.1109/TIA.2021.3074109

Tarzamni, H., Babaei, E., Esmaeelnia, F.P., Dehghanian, P., Tohidi, S., Sharifian, M. B.B. (2019). Analysis and reliability evaluation of a high step-up soft switching push–pull DC–DC converter. *IEEE Transactions on Reliability*, 69(4), 1376-1386. http://doi.org/10.1109/TR.2019.2945413

Wu, Q., Wang, Q., Xu, J., Xiao, L. (2016). A wide load range ZVS push–pull DC/DC converter with active clamped. *IEEE Transactions on Power Electronics*, 32(4), 2865-2875. http://doi.org/10.1109/TPEL.2016.2577639

Wu, T.F., Hung, J.C., Tsai, J.T., Tsai, C.T., Chen, Y.M. (2008). An active-clamp push–pull converter for battery sourcing applications. *IEEE transactions on Industry Applications*, 44(1), 196-204. http://doi.org/10.1109/TIA.2007.912748

Xiao, H., Wu, Q., Xi, H. (2022). Analysis and design of a wide range ZVS/ZCS push–pull DC/DC converter with voltage clamped. *IET Power Electronics*, 15(5), 422-433. http://doi.org/10.1049/pel2.12242

Xu, G., Qu, Y., Li, L., Xiong, W., Xia, Z., Sun, Y., Su, M. (2023). Magnetizing Current Injection Based Push-Pull Dual Active Bridge Converter with Optimized Control to Achieve Full Load Range ZVS for the Distributed Generation System. *IEEE Transactions on Energy Conversion*, 38(3), 1589-1601. http://doi.org/10.1109/TEC.2023.3257000

Xu, J., Wu, Q., Wang, Y. (2018). Magnetising-current-assisted wide ZVS range push–pull DC/DC converter with reduced circulating energy. *IET Power Electronics*, 11(2), 272-279. http://doi.org/10.1049/iet-pel.2016.1016

Xuewei, P., Rathore, A.K. (2014). Naturally clamped zero-current commutated soft-switching current-fed push–pull DC/DC converter: analysis, design, and experimental results. *IEEE Transactions on Power Electronics*, 30(3), 1318-1327. http://doi.org/10.1109/TPEL.2014.2315834

Yapici, H., İnan, R. (2024). An Improved Resonant Gate Driver for MOSFETs in DC-DC Converters. *Acta Polytechnica Hungarica*, 21(8), 263-287. http://doi.org/10.12700/APH.21.8.2024.8.14

Yuan, Y., Chang, L., Song, P. (2007). A new LCL-resonant push-pull DC-DC converter for inverter applications. *In 2007 Large Engineering Systems Conference on Power Engineering*, 10-12 October 2007, Montreal, QC, Canada.

Yuan, Y., Wu, Q. (2013). One zero-voltage-switching three-transistor push–pull converter. *IET Power Electronics*, 6(7), 1270-1278. http://doi.org/10.1049/iet-pel.2013.0054

Zhang, G., Xiang, W., Han, M., Zuo, W., Zhou, M., Wen, J. (2023). DC impedance modeling of push-pull DC autotransformer for MMC and LCC HVDC interconnections. *IEEE Transactions on Power Delivery*, 38(4), 2441-2453. http://doi.org/10.1109/TPWRD.2023.3243887

Zhou, X., Sheng, B., Liu, W., Chen, Y., Wang, L., Liu, Y.F., Sen, P.C. (2021). A high-efficiency high-power-density on-board low-voltage DC–DC converter for electric vehicles application. *IEEE Transactions on Power Electronics*, 36(11), 12781-12794. http://doi.org/10.1109/TPEL.2021.3076773