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# Intelligent Control of a New High Voltage Gain Interleaved DC-DC Converter for Fuel Cell Applications

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## Highlights

- An interleaved non-isolated high-step up DC-DC converter for fuel cell applications is proposed.
- The proposed converter takes advantage of the quadratic-boost and switched-capacitor networks.
- An intelligent control method based on a single-input fuzzy-logic controller is developed.
- A detailed simulation study is realized for the proof of concept.

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**Abstract**

As important elements of the hydrogen economy, fuel cells (FCs) require high step-up DC-DC converters. To this end, a new high voltage gain interleaved DC-DC converter benefiting from expandable quadratic-boost and switched-capacitor networks is proposed in this paper. A switching model shows that the proposed converter reaches a voltage gain of about 10, semiconductor voltage stresses are half of the output voltage or less, and current stresses are cut in half when compared to the non-interleaved version. Besides, according to a dynamic simulation study, the newly proposed single-input fuzzy-logic controller-based control method allows less than half the settling time and 5% less voltage overshoot than the current mode control; moreover, it attains a perfect current sharing while voltage mode control fails by having a current unbalance factor of up to 0.33. Finally, an average model demonstrates the accomplished operation of the offered system under an office block power demand.

## 1. INTRODUCTION

The recent advancements in power electronics technology and increased penetration of direct-current (DC) loads and DC sources motivate researchers to work on DC distribution systems [1]. Among DC sources, hydrogen fuel cells (FCs) have gained an important research interest employing their continuous power production ability, high power density, and efficient operation [2]. FCs usually combine hydrogen and oxygen for electricity generation by promising an environmentally friendly operation with only by-products of heat and water [3]. Moreover, serious consideration of the hydrogen economy concept, motivated by the global carbon neutrality goal, further highlights the importance of FCs [4, 5]. Nevertheless, FCs bear the burden of low producible voltage, nearly 1 V/cell at the no-load condition [6]; this drawback therefore dictates using high-step DC-DC converters when linking them to a high-voltage DC bus [7]. Isolated DC-DC converters, such as the ones in [8-10], provide galvanic isolation between the input and output ports through transformers or coupled inductors helping to attain high conversion ratios at the risk of increased cost, size, and losses [11]. Therefore, non-isolated DC-DC converters can be declared more feasible for FC applications [12]. Since the classical boost converter (CBC) has a limited voltage-boosting capability and suffers from low efficiency in the high duty cycle region, innovative approaches are necessary for the DC-DC high step-up converting [13]. For example, a quadratic boost (QB) converter and a quasi-Z source converter (qZSC) are studied in [14] and [15] for high step-up applications, respectively; these converters still have limited voltage gains and do not offer flexibility in terms of extra stages. Besides, researchers have investigated several voltage-boosting techniques allowing the addition of extra stages, such as, the switched-capacitor (SC) [16], switched-inductor (SI) [17], and hybrid SC/SI [18]. Moreover, there are some

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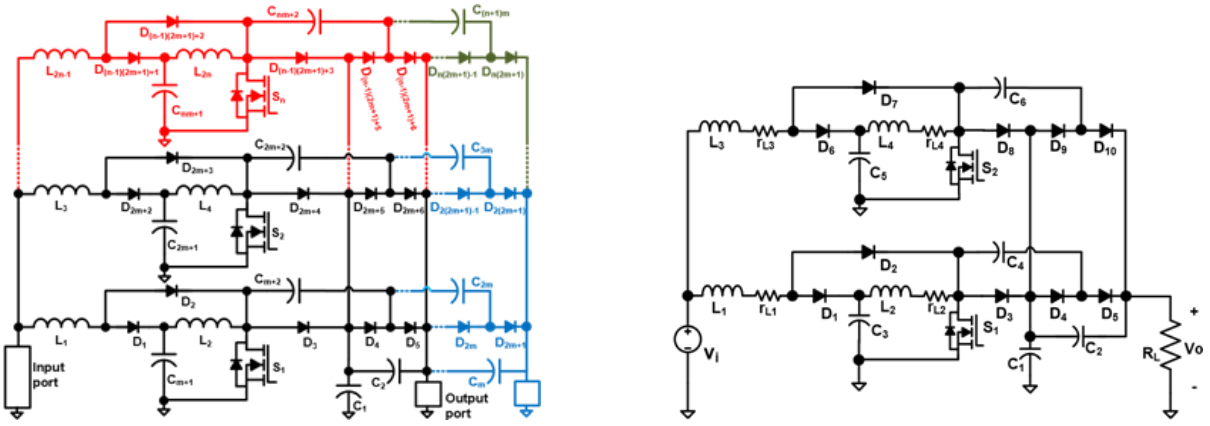
important efforts for voltage-gain improvement of QB converters and qZSC thanks to SC networks like in [19-21].




*(a)* *(b)*

***Figure 1.*** *The proposed converter: a) generalized version, b) analysed version*

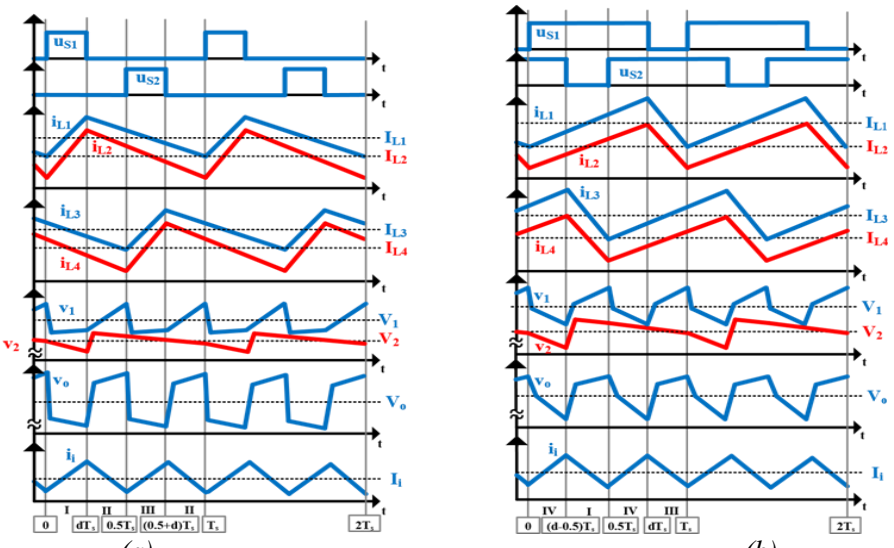
Despite their valuable contributions, non-interleaved high step-up converters, such as those proposed in [14-21], require large input inductors to minimize input current ripple, which is essential for preventing degradation of the FC's electrochemical components and ensuring stable and long operation.Fortunately, interleaved converters reduce inductor sizes by processing power in parallel stages offering several advantages, such as improved efficiency and minimized electromagnetic interference (EMI) [22]; In addition to these advantages, they minimize the input current ripple ofinterleaved conveConsidering these advantages, many papers, such as [23, 24], discuss building FC power systems with the interleaved versions of CBC; however, these attempts fail to meet the high step-up requirement. Thus, agglomerating the benefits of interleaved and high step-up converters has recently become a research trend. For instance, a cascaded topology is proposed in [25] where an interleaved CBC and an interleaved new type of boost converter are connected in series; so, the efficiency is limited and the structure is complex. Moreover, an interleaved SI based boost converter is studied in [26]; although this topology offers flexibility in terms of phases and SI levels, it suffers from complexity and low efficiency when phases and SI levels increase. Additionally, another high step-up interleaved converter is successfully implemented in [27] where utilization of multiple SI and SC networks is offered for voltage-gain improvement; however, this converter offers no common ground which may result in EMI problems [28]. Two interleaved converters with no common ground are proposed in [29] and [30]; these converters reach high voltage gains thanks to the expandable hybrid SC/SI networks and SC networks, respectively; unfortunately, they can have only up to two phases. Furthermore, an interleaved converter with a common ground is studied in [31] in which expandable Cockcroft–Walton voltage-multiplier cells and multiple phases can be used; although the steady-state operation is demonstrated in this reference; no details about the controller performance are given.

In this paper, a new interleaved high step-up converter is proposed by inspiring the non-interleaved structure given in [19], which is a hybrid converter based on the QB and SC network. The proposed converter is illustrated in Figure 1, which presents both the generalized and analyzed versions of the topology. As seen in Figure 1a, the proposed converter promises a high voltage gain and minimized input current ripple owing to the n-number of phases and m-level of SC networks; additionally, it is advantageous in terms of limiting EMI since it has a common ground between its input and output. Another contribution of this paper is on the closed-loop control, which is invariably required in a DC-DC converter due to the non-linearity. The most basic control technique in the literature is the voltage-mode control (VMC) consisting of a single controller with a voltage feedback [32]. However, the dynamic performance of VMC is limited under disturbances and uncertainties [33]. For achieving better control performances, the literature has widely examined Fuzzy Logic Controller (FLC)-based control implementations in DC-DC converters. For instance, back in the 2000s, authors in [34] successfully realized the real-time control of a forward converter by FLC, besides, authors in [35] designed a FLC and implemented it effectively in a buck converter. There are also many up-to-date efforts; for example, the papers in [36] and [37] discuss the FLC-based voltage

control of newly proposed high step-up converters. Moreover, the control performances of a FLC and a PID controller are compared in [38] for a boost converter. Although the mentioned FLC-based techniques perform well in non-interleaved converters, they fail to provide satisfactory current sharing between individual inductors in an interleaved converter. Fortunately, the current mode control (CMC) helps to eliminate the deficiencies of the touched VMC and FLC-based techniques. In CMC, current loops regulate the individual inductor currents while a voltage-loop determines the current references. Besides having improved dynamic performance, CMC allows precise current sharing between inductors thanks to current feedbacks. Typically, the proportional-integral (PI) controllers are used in voltage and current loops in CMC applications as in [6, 27]. Unfortunately, this approach shows good performances only in a narrow operation area since PI controllers are designed based on the small signal analysis considering a quiescent operating point [23]. Therefore, the applications of various modern control methods to the DC-DC interleaved converters have been examined in recent years; for instance, the model predictive control [39], sliding mode control [40], and active disturbance rejection control [41]. The papers in [39-41] concentrate on the voltage loop and use PI controllers in current loops since current loops can be treated as being ideal because of their comparatively larger bandwidths [42]. Despite their good performances, the mentioned modern techniques suffer from complexity and dependence on the mathematical models of utilized converters. In consideration of the findings, this work suggests to use a single-input FLC (SIFLC) in determining the current reference, and then to regulate inductor currents by PI controllers. SIFLC has only one input and one-dimensional rule vector; therefore, it allows considerable simplification without making any control concessions when compared to the classical FLC [43-45].

## 2. ANALYSIS OF THE PROPOSED CONVERTER

The 2-phase and 2-level version of the proposed converter is examined in this work. As shown in Figure 1b, the converter consists of four inductors ($L_1$ −$L_4$), six capacitors ($C_1$ −$C_6$), ten diodes ($D_1$ −$D_{10}$), and two switches ($S_1$ and $S_2$). The diodes $D_1$, $D_2$, $D_6$, and $D_7$ are responsible for the quadratic operation while other diodes ($C_1$, $C_2$, $C_4$ and $C_6$), called SC capacitors in this work, for voltage multiplying capability in a way of forming a SC network. In the analysis, it is assumed that all elements but inductors are ideal, capacitors are large enough to maintain constant voltages, and the converter operates in continuous current mode (CCM). Moreover, the duty cycles of switches, denoted by $d_1$ and $d_2$, are same at $d$. Figure 2 shows the specific waveforms of the key elements in two switching cycles ($T_s$) considering the cases of $d < 0.5$ and $d > 0.5$. As can be seen there is 180 phase shift between the gate signals of switches ($u_{S1}$ and $u_{S2}$) due to the interleaving operation. The related equivalent circuits with the switching stages ($I$–$IV$) indicated in Figure 2 can be seen in Figure 3. Please note that green and blue arrows in these circuits show the charging and discharging currents of capacitors, respectively; and the inductor currents are denoted by $i_{L1}$−$i_{L4}$ while the capacitor voltages are by $v_1$−$v_6$.




(a) (b)

***Figure 2.*** *Typical waveforms when a) d < 0.5, b) d > 0.5*

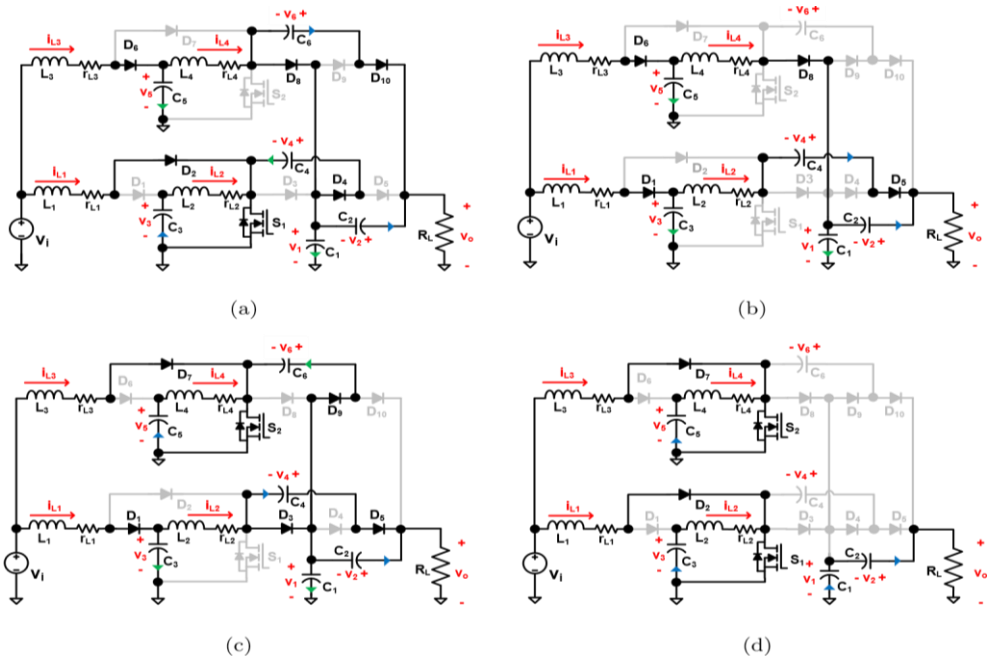



***Figure 3.*** *Equivalent circuits in the switching states a) I, b) II, c) III, d) IV*

### 2.1. Steady-State Analysis

The steady-state waveforms for $d < 0.5$ are demonstrated in Figure 2a. There are three different switching stages in this case. In the switching state-I (Figure 3a), $S_1$ is *ON* and $S_2$ is OFF. Therefore, $D_2$, $D_4$, $D_6$, $D_8$ and $D_{10}$ conduct. $L_1$ and $L_2$ are charged while $L_3$ and $L_4$ are discharged. At the beginning of this stage, $C_1$ first discharges rapidly to clamp to $C_4$ (not illustrated here), then both are started to be charged by the $i_{L4}$. Moreover, $C_2$ and $C_6$ discharge to feed the output load. The switching state-II (Figure 3b) starts when both switches are opened. Here all inductors discharge so their currents decrease. In this stage, $D_1$ and $D_6$ conduct to carry $i_{L1}$ and $i_{L3}$. Here, $D_{10}$ becomes reversed-biased thus $C_6$ keeps its energy and $C_1$ charging current increases. Shortly after this stage starts, $C_2$ first charges to clamp to $C_4$, then two capacitors discharge and feed the load. Similarly, opening $S_2$ while $S_1$ is conducting makes $D_5$ reversed-biased thus $v_4$ is constant and $C_2$ clamps to $C_6$, which is not shown in this paper. Turning $S_2$ ON starts the switching stage-III (Figure 3c) which is similar to the first stage. This time, $C_6$ is charged through $D_9$ while $C_4$ discharges through $D_5$ to the output. Furthermore, $i_{L3}$ and $i_{L4}$ increase while $i_{L3}$ and $i_{L4}$ continue to decrease.

Furthermore, Figure 2b shows the typical waveforms when $d > 0.5$. As illustrated in Figure 3a and Figure 3c, the states of elements in this case are the same as the ones when $d < 0.5$. However, this time, $C_2$ is first charged to clamp $C_6$ and $C_4$ shortly after the switching states I and III start, respectively. Then, two associated capacitors discharge to the output. Besides, $C_1$ is charged along with $C_4$ or $C_6$ in these two stages. In the switching state-IV, both $S_1$ and $S_2$ are *ON* at the same time; so all inductor currents rise. Besides, all diodes except $D_2$ and $D_7$ are *OFF* thus $v_4$ and $v_6$ are constant. Here, $C_1$ and $C_2$ are responsible for supplying the load.

Based on the steady state analysis, the state-space averaging technique allows obtaining the dynamic model of the proposed converter as in (1) and (2),

$$\frac{d}{dt}\begin{bmatrix} i_{L1} \\ i_{L2} \\ i_{L3} \\ i_{L4} \end{bmatrix} = \begin{bmatrix} (v_i - v_3 d' - i_{L1} r_1)/L_1 \\ (v_i - (v_o - v_4) d' - i_{L2} r_2)/L_2 \\ (v_i - v_5 d' - i_{L3} r_3)/L_3 \\ (v_i - v_3 d' - i_{L1} r_1)/L_4 \end{bmatrix} \tag{1}$$

$$\frac{d}{dt}\begin{bmatrix} v_3 \\ v_5 \\ v_o \end{bmatrix} = \begin{bmatrix} (i_{L1}d' - i_{L2})/C_3 \\ (i_{L3}d' - i_{L4})/C_5 \\ ((i_{L2} + i_{L4})d' - 2v_o/R_L)/C_o \end{bmatrix}. \tag{2}$$

In (1) and (2), $d'$ is equal to $1-d$, and $C_o$ denotes the output capacitor, simply calculated based on the switched capacitor behaviour by $C_o = C_1C_2/(C_1+C_2)$.

### 2.2. Voltage Gain Analysis

First of all, one notices that the switched capacitor behavior lets the DC values of all SC capacitors be equal to half of the output voltage as $V_1 = V_2 = V_4 = V_6 = V_0/2$. Then, the well-known procedure based on the principles of small ripple approximation, inductor-volt-second balance, and capacitor-charge-balance are implemented to (1) and (2) for attaining the steady state quantities. Under the assumption of the properly designed converter ($r_1 = r_3 = r_\alpha$ and $r_2 = r_4 = r_\beta$), the non-ideal voltage gain of the proposed converter can be obtained by

$$G = \frac{V_o}{V_i} = \frac{2}{D'^2} \times \frac{R_L D'^2}{R_L D'^2 + 4r_\alpha/D'^2 + 4r_\beta} = \frac{2}{D'^2} \times \mu(D', R_L, r_\alpha, r_\beta) \tag{3}$$

where $\mu$ denotes the efficiency of the converter, represented by the second term on the right-hand side of (3), and is a function of the duty cycle, load resistance, and inductor resistances. According to (3), the ideal voltage gain is $2/D'^2$ as in the non-interleaved version. Figure 4 provides the performance analysis results. In Figure 4a, the negative effect of the decreasing efficiency on the voltage gain is exhibited considering different $r_\alpha/R_L$ and $r_\beta/R_L$ values. Besides, the inductor average currents can be related as follows:

$$I_{L1} = I_{L3} = I_{L\alpha} = \frac{V_o}{\mu R_L D'^2} = \frac{I_o}{\mu D'^2}, \quad I_{L2} = I_{L4} = I_{L\beta} = I_{L\alpha} D'. \tag{4}$$

From (4), one can see that the interleaved structure cuts the inductor currents in half when compared to the non-interleaved version [19].

### 2.3. Small Signal Analysis

The small signal analysis of the proposed converter can be realized by perturbing the dynamic model expressions as in

$$\frac{d}{dt}\tilde{x} = A\tilde{x} + B\tilde{d} \tag{5}$$

where $\tilde{x}$ and $\tilde{d}$ are the state variables and control variable, respectively. The small signal model of the proposed converter can be obtained as follows:

$$A = \begin{bmatrix} -r_1/L_1 & 0 & 0 & 0 & -D'/L_1 & 0 & 0 \\ 0 & -r_2/L_2 & 0 & 0 & 1/L_2 & 0 & -D'/(2L_2) \\ 0 & 0 & -r_3/L_3 & 0 & 0 & -D'/L_3 & 0 \\ 0 & 0 & 0 & -r_4/L_4 & 0 & 1/L_4 & -D'/(2L_4) \\ D'/C_3 & -1/C_3 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & D'/C_5 & -1/C_5 & 0 & 0 & 0 \\ 0 & D'/C_o & 0 & D'/C_o & 0 & 0 & -2/(R_L C_o) \end{bmatrix}, \tag{6}$$

$$B = [V_3/L_1 \quad V_o/(2L_2) \quad V_5/L_3 \quad V_o/(2L_4) \quad -I_{L\alpha}/C_3 \quad -I_{L\alpha}/C_5 \quad -2I_{L\beta}/C_o]^T,$$

$$\tilde{x} = [\tilde{i_{L1}} \quad \tilde{i_{L2}} \quad \tilde{i_{L3}} \quad \tilde{i_{L4}} \quad \tilde{v_3} \quad \tilde{v_5} \quad \tilde{v_o}]^T.$$

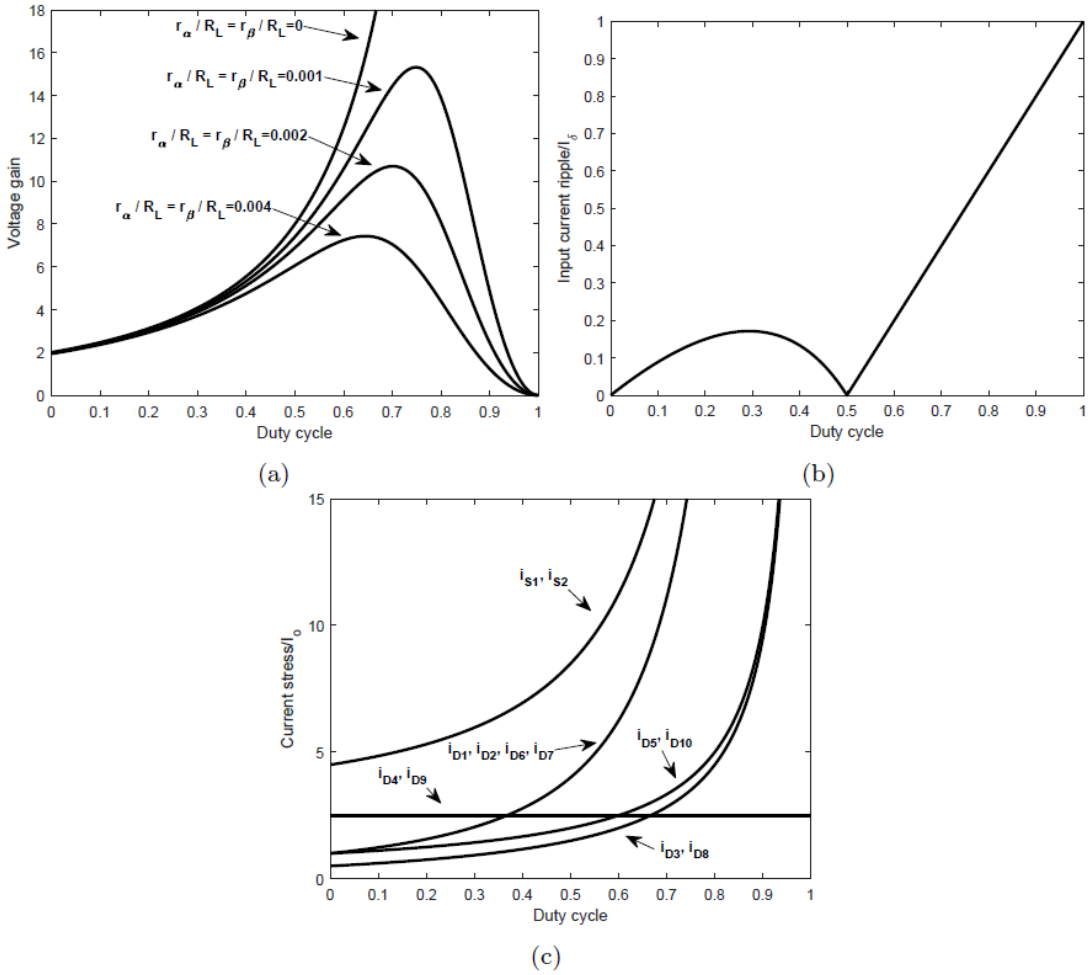



***Figure 4.*** *a) Voltage-gain curves, b) input current ripple, c) current stresses*

## 3. DESIGN PROCEDURE

In (5), it is shown that how average inductor currents are related to the output current. Now, based on Figure 2, the inductor current ripples can be calculated by ignoring inductor resistances and assuming that $L_1$=$L_3$=$L_\alpha$ and $L_2$=$L_4$ =$L_\beta$ as in

$$\Delta i_{L1} = \Delta i_{L3} = \Delta i_{L\alpha} = \frac{V_i D}{L_\alpha f_s}, \quad \Delta i_{L2} = \Delta i_{L4} = \Delta i_{L\beta} = \frac{V_i D}{D' L_\beta f_s} \tag{7}$$

where $f_s$ is the switching frequency. Since the input current is equal to sum of $i_{L1}$ and $i_{L3}$, the input current ripple can be computed by studying on their slopes as in

$$\Delta i_i = \begin{cases} \dfrac{I_\delta (1-2D) D}{D'}, & if\ D < 0.5, \\ I_\delta (2D-1), & if\ D > 0.5. \end{cases} \tag{8}$$

where $I_\delta = V_i/(L_\alpha f_s)$. In Figure 4b, the normalized input current ripple is plotted against the duty cycle. This figure shows that the input current ripple is cancelled out when $D$=0.5. Moreover, in low duty cycle region, it is possible to have low input current ripples in comparison to high duty cycle region. When it comes to designing capacitors, their voltage ripples need to be known. From Figure 2, the voltage ripples of $C_3$ and $C_5$ can be computed as in (9) when assuming $C_3$=$C_5$ =$C_\alpha$.

$$\Delta v_3 = \Delta v_5 = \frac{V_o D}{D' R_L C_\alpha f_s}. \quad (9)$$

After this step, instead of focusing on the individual voltage ripples of SC capacitors, the output voltage ripple is expressed as in (10) under the assumption that all SC capacitors are equal to $C_\beta$. It is known that all SC capacitors are exposed to the half of the output voltage. Besides, it can be shown that the average voltages of $C_3$ and $C_5$ are ideally equal to $V_o D'/2$.

$$\Delta v_o = \frac{2V_o D}{R_L C_\beta f_s}. \quad (10)$$

The voltage and current stresses of the semiconductors are obtained based on the equivalent circuits demonstrated in Figure 3, then are listed in Table 1. According to this table, the switches and SC diodes are exposed to only half of the output voltage thanks to SC operation; besides, the voltage stresses of $D_1$, $D_2$, $D_6$, and $D_7$ are scaled by the duty cycle resulting in even lower voltage ratings. Additionally, the current stress expressions are attained by considering only average inductor currents assuming low current ripples. Unlike other components, special attention is required to obtain the current stresses of $D_4$ (or $D_9$) and $S_1$ (or $S_2$). According to Figure 3a, turning on $S_1$ in Stage-I results in $C_1$ clamps to $C_4$ through $D_4$ and $S_1$, and therefore a current spike occurs on $D_4$ which can be calculated by $I_o/(2C_\beta f_s r_p)$ where $r_p$ is equivalent series resistance of $C_1$, $C_4$, $D_4$, and $S_1$ considering the generated voltage difference between $C_1$ and $C_4$ in the previous state; besides, this current spike also is seen on $S_1$. The normalized current stresses are plotted in Figure 4c; according to this figure, $D_1$, $D_2$, $D_6$, $D_7$, and switches experience higher current stresses since they take upon transferring the currents of input inductors ($L_1$ and $L_3$). Please note that the product of "$C_\beta f_s r_p$" is here set to a typical value, 0.2, for illustration. Finally, based on the voltage and current characteristics of a FC system, Nexa 1200 from Heliocentris, and the above analysis, the power elements of the proposed converter are designed for $200V$ output voltage as summarized in Table 2.

## 4. CONTROL METHODS

In this paper, a SIFLC-based control strategy is developed for the proposed converter and compared with two classical approaches, VMC and CMC. As seen in Figure 5, VMC regulates output voltage by a single closed-loop without direct current feedback, while CMC employs dual closed-loops to regulate both voltage and inductor current. Unlike CMC, this paper proposes to determine the current reference using a SIFLC.

### 4.1. VMC and CMC Strategies

In VMC (Figure 5a), there is a voltage control loop where a PI controller, $PI_{vd}$, sets the duty cycle of both switches to the same value. In CMC (Figure 5b), a PI controller, $PI_{id}$, in a voltage loop, called outer loop, determines the reference value of average inductor currents; then inductor currents are regulated by another PI controllers, $PI_{id}$, thanks to the current feedbacks passed through low-pass filters (LPFs). The transfer functions of the control loops are obtained by substituting the converter parameters into (6) as follows:

$$G = C(sI - A)^{-1}B. \quad (11)$$

***Table 1.*** *Semiconductor stresses*

| Elements | Voltage stress | Current stress |
|---|---|---|
| $D_1$, $D_2$, $D_6$, $D_7$ | $(V_o/2)D'$ | $I_{L\alpha}$ |
| $D_3$, $D_8$ | $V_o/2$ | $I_{L\beta}-I_o/2$ |
| $D_4$, $D_9$ | $V_o/2$ | $I_o/(2C_\beta f_s r_p)$ |
| $D_5$, $D_{10}$ | $V_o/2$ | $I_{L\beta}$ |
| $S_1$, $S_2$ | $V_o/2$ | $I_{L\alpha}+ I_{L\beta}+I_o/(2C_\beta f_s r_p)$ |

***Table 2.*** *Converter specifications*

| | |
|---|---|
| Input voltage | 20-36V |
| Output voltage | 200V |
| Peak output power | 1kW |
| Switching frequency | 50kHz |
| $S_1$, $S_2$ | IXTP48N20T (IXYS), 200V /48A |
| $D_1$, $D_2$, $D_6$, $D_7$ | V30100SG-E3/4W (Vishay), 100V /30A |
| $D_3$, $D_4$, $D_5$, $D_8$, $D_9$, $D_{10}$ | MBRF10200 (SMC Diode Solutions), 200V /10A |
| $L_1$, $L_3$ | CODACA, 35µH/25A |
| $L_2$, $L_4$ | Allied Components, 120µH/14.4A |
| $C_1$, $C_2$, $C_4$, $C_6$ | Nichicon, 56µF/160V |
| $C_3$, $C_5$ | Nichicon, 270µF/80V |

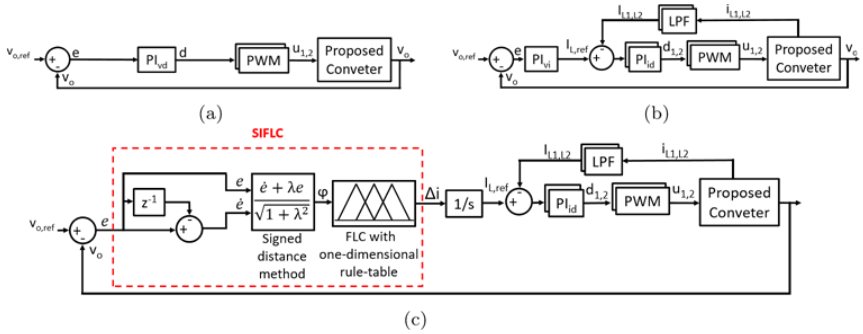



***Figure 5.*** *Control strategies: a) VMC, b) CMC, c) SIFLC*

Now, one can design PI controllers, whose transfer functions are simply $K_p + K_i/s$. Tuning of the proportional gains ($K_p$) and integral gains ($K_i$) of the individual PI controllers is realized through SmartCtrl software as summarized in Table 3. Bode plots before and after compensations of the voltage control loop in VMC, and both outer and inner control loops in CMC are demonstrated in Figure 6. As seen in these plots, compensations yield attaining loop gains having positive phase margins ($\phi$) and decreased cut-off frequencies ($f_c$).

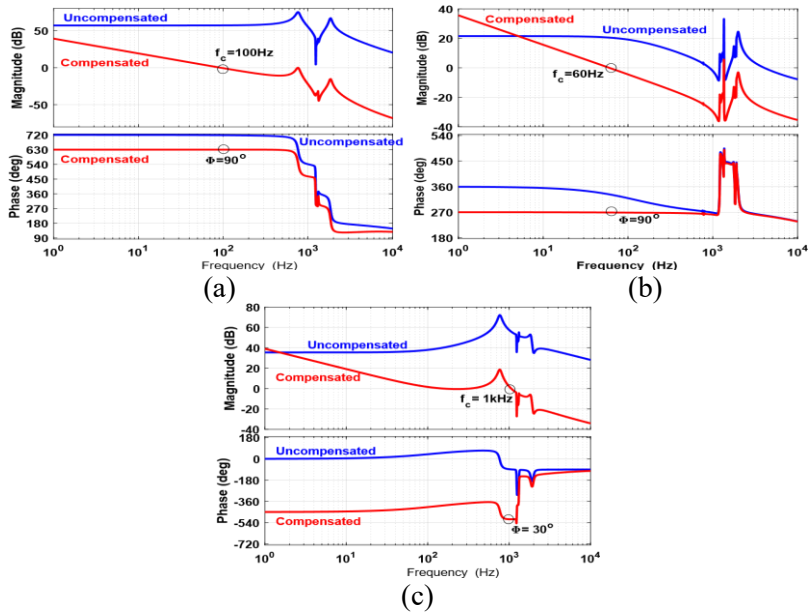



***Figure 6.*** *Bode plots a) voltage loop in VMC, b) outer loop in CMC, c) inner loop in CMC*

***Table 3.*** *Gains of the PI controllers*

| | $K_p$ | $K_i$ |
|---|---|---|
| $PI_{vd}$ | $3.5102 \times 10^{-5}$ | 0.8144 |
| $PI_{vi}$ | 0.0416 | 31.9677 |
| $PI_{id}$ | $5.6123 \times 10^{-4}$ | 9.5314 |

The FLC-based voltage control techniques like in [34-38] have usually two input membership functions (MFs), the error voltage ($e$) and change in error ($\dot{e}$), and an output MF, the change in duty cycle ($\Delta d$). As demonstrated in Figure 5c, the proposed SIFLC technique uses the same input functions; however, the output MF is now the change in the current reference, $\Delta i$. The literature review reveals that mostly symmetrical triangular MFs are preferred in FLCs for minimizing computational complexity, as in this paper. The linguistic variables in the designed MFs are Negative-High (NH), Negative-Medium (NM), Negative-Small (NS), Zero (Z), Positive-Small (PS), Positive-Medium (PM), and Positive-High (PH), as in [35]. First of all, the minimum and maximum values for $e$ are designed as ±200, while as ±0.1 for $\dot{e}$, and as $\pm 5 \times 10^4$ for $\Delta i$. Then, the rule table given in Table 4 is created; similar tables to this table are likely to come across in the literature since DC-DC converters have similar characteristics, e.g., when both $e$ and $\dot{e}$ are large and positive, the duty cycle should increase greatly [43]. As can be seen, the designed rule-table has the same output memberships in a diagonal direction; a FLC with this kind of rule table is said to have a Toeplitz structure [46]. Instead of two input variables requiring a two-dimensional rule-table as in Table 4, it is possible to realize the fuzzy logic (FL) operation by calculating a single input variable ($\varphi$) by the signed-distance method as in

$$\varphi = \frac{\dot{e} + \lambda e}{\sqrt{1 + \lambda^2}} \tag{12}$$

where $\lambda$ is the slope of the main diagonal line. For further details about the signed-distance method, please refer to [46]. In this paper, $\lambda$ can be calculated as 0.1/200 = 0.0005 from the input MFs; then, $\varphi$ can be expressed as $\varphi \approx \dot{e} + 0.0005e$. After obtaining $\varphi$, the one-dimensional rule table is designed as in Table 5; therefore the SIFLC operation is achieved. It is clear that the minimum and maximum values for $\lambda$ can be computed as ±0.2, while they are still $\pm 5 \times 10^4$ for $\Delta i$.

## 5. TEST AND RESULTS

First of all, the model of the chosen FC system is created in MATLAB/Simulink based on the model and parameters presented in [47]; readers are referred to the mentioned paper for further modelling details. Moreover, a non-ideal switching model of the proposed converter is built by PLECS Blockset while control strategies are implemented by Simulink blocks. As an example, SIFLC method is shown in Figure 7. Please note that FL operation in this paper is realized by the Fuzzy Logic Toolbox and the center-of-gravity method is preferred for the defuzzification process.

***Table 4.*** *Two dimensional rule base*

| $e$ \ $\dot{e}$ | PH | PM | PS | Z | NS | NM | NH |
|---|---|---|---|---|---|---|---|
| NH | Z | NS | NM | NH | NH | NH | NH |
| NM | PS | Z | NS | NM | NH | NH | NH |
| NS | PM | PS | Z | NS | NM | NH | NH |
| Z | PH | PM | PS | Z | NS | NM | NH |
| PS | PH | PH | PM | PS | Z | NS | NM |
| PM | PH | PH | PH | PM | PS | Z | NS |
| PH | PH | PH | PH | PH | PM | PS | Z |

***Table 5.*** *One dimensional rule base*

| $\varphi$ | PH | PM | PS | Z | NS | NM | NH |
|---|---|---|---|---|---|---|---|
| $\Delta_i$ | PH | PM | PS | Z | NS | NM | NH |

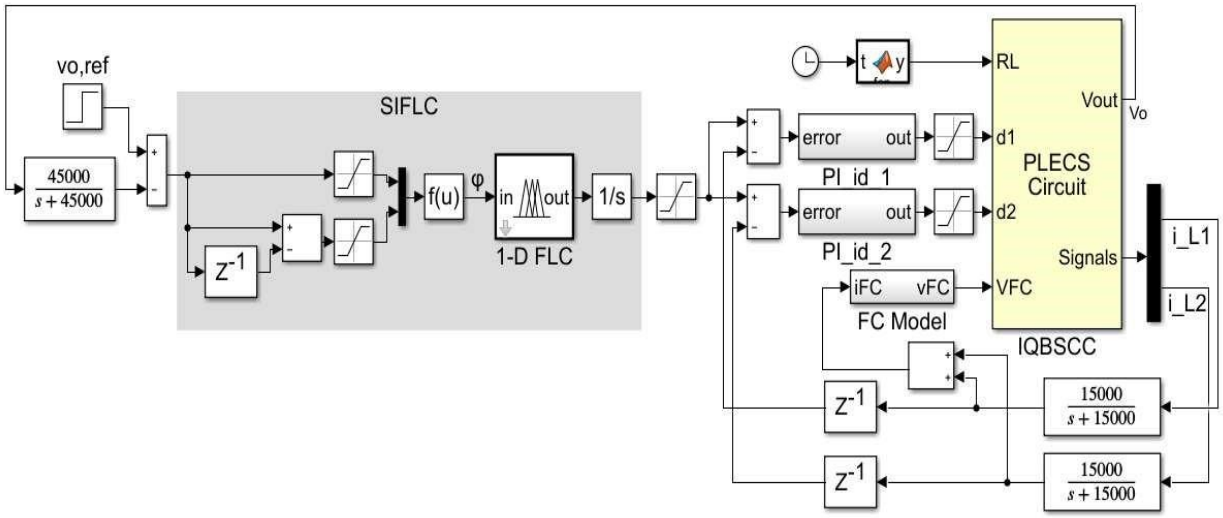



***Figure 7.*** *Simulation model of the SIFLC method*

In the simulation study, three different cases are considered. In these cases, the parameters and parasitics of the converter elements are varied according to the values and tolerances provided in their datasheets as can be seen in Table 6, where $r_{ds-on}$, $V_f$, $L$, $DCR$, and $ESR$ denote the on-state resistance of switches, forward voltage drops of diodes, inductances, dc resistances of capacitors, and equivalent series resistances of inductors, respectively. In this way, it is targeted to make a better evaluation by taking into account the variations that may be faced in real world-applications.

***Table 6.*** *Simulation parameters*

| **Elements** | **Parameters** | **Case-1** | **Case-2** | **Case-3** |
|---|---|---|---|---|
| $S_1$ | $r_{dson}(m\Omega)$ | 50 | 40 | 45 |
| $S_2$ | $r_{dson}(m\Omega)$ | 50 | 50 | 40 |
| $D_1$ and $D_2$ | $V_f(V)$ | 1 | 0.9 | 0.8 |
| $D_3$, $D_4$, and $D_5$ | $V_f(V)$ | 0.95 | 0.85 | 0.8 |
| $D_6$ and $D_7$ | $V_f(V)$ | 1 | 1 | 0.9 |
| $D_8$, $D_9$, and $D_{10}$ | $V_f(V)$ | 0.95 | 0.95 | 0.85 |
| $L_1$ | $L(\mu H)$, $DCR(m\Omega)$ | 35, 4.6 | 39, 4.5 | 37, 4.4 |
| $L_2$ | $L(\mu H)$, $DCR(m\Omega)$ | 120, 28 | 130, 26 | 130, 24 |
| $L_3$ | $L(\mu H)$, $DCR(m\Omega)$ | 35, 4.6 | 35, 4.6 | 33, 4.5 |
| $L_4$ | $L(\mu H)$, $DCR(m\Omega)$ | 120, 28 | 120, 28 | 110, 25 |
| $C_1$ and $C_2$ | $C(\mu F)$, $ESR(m\Omega)$ | 56, 11.3 | 56, 11.3 | 53, 11.8 |
| $C_3$ | $C(\mu F)$, $ESR(m\Omega)$ | 270, 0.95 | 250, 0.92 | 280, 0.98 |
| $C_4$ | $C(\mu F)$, $ESR(m\Omega)$ | 56, 11.3 | 50, 11.2 | 60, 11.4 |
| $C_5$ | $C(\mu F)$, $ESR(m\Omega)$ | 270, 0.95 | 270, 0.95 | 250, 0.92 |
| $C_6$ | $C(\mu F)$, $ESR(m\Omega)$ | 56, 11.3 | 56, 11.3 | 55, 11.1 |

First of all, both voltage and current waveforms of the semiconductors at steady-state are observed. In this study, the output power is set to its maximum, $1kW$, and the parameters in Case-1 are used. In Figure 8, only the waveforms associated with $S_1$, $D_1$, $D_2$, $D_3$, $D_4$, and $D_5$ are shown since the ones in the other phase have same peak values. According to Figure 8, $S_1$, $D_3$, $D_4$, and $D_5$ are exposed to the the half of the output voltage, $100V$, thanks to the SC operation; while $D_1$ and $D_2$ are exposed to about $50V$ since $d_1$ is about 0.5. As a results, the voltage stress analysis provided in Table 1 is verified. Moreover, considering that the output current is $10A$, letting $D'$ as 0.5 and $\mu$ as 0.9, $I_{L\alpha}$ and $I_{L\beta}$ can be computed as about $22A$ and $11A$ from (4); then one can easily validate the current stress analysis in Table 1 by checking the peak currents pointed out in Figure 8.

Furthermore, the performances of VMC, CMC, and SIFLC methods are tested in case of step disturbances considering all cases. As shown in Figure 9, the output resistor is first decreased to 50Ω from 80Ω, then the output voltage is reference is decreased to 180V from 200V. Firstly, all control methods succeed in the output voltage regulation in all cases, therefore the proposed converter reaches the aimed step-up ratio. However, CMC slightly falls SIFLC and VMC behind: the settling times for VMC and SIFLC are about 10ms after both disturbances while they are about 25ms for CMC; in addition, overshoots for VMC and SIFLC are about 7.5% after the first disturbance while it is about 12.5% for CMC. Figure 9 also includes the voltage and current variations of FC; these results show that the control methods can regulate the output voltage while handling the dynamics of the FC.

Besides, the input inductor currents ($i_{L1}$ and $i_{L3}$) are demonstrated in Figure 10 for three control methods and three cases. From these simulation results, it can be first noticed that all methods realize the interleaved operation successfully in Case-1; however VMC cannot regulate the average inductance currents at the same value, thus failing in current sharing in other cases. At this point, a current unbalance factor (Iψ) can be calculated by $|I_{L1}-I_{L3}|/I_{L1}$ for comparison [48]. According to Figure 10, Iψ values for VMC are about 0.33 and 0.0625 in Case-2 and Case-3, respectively, while they are zero for CMC and SIFLC.

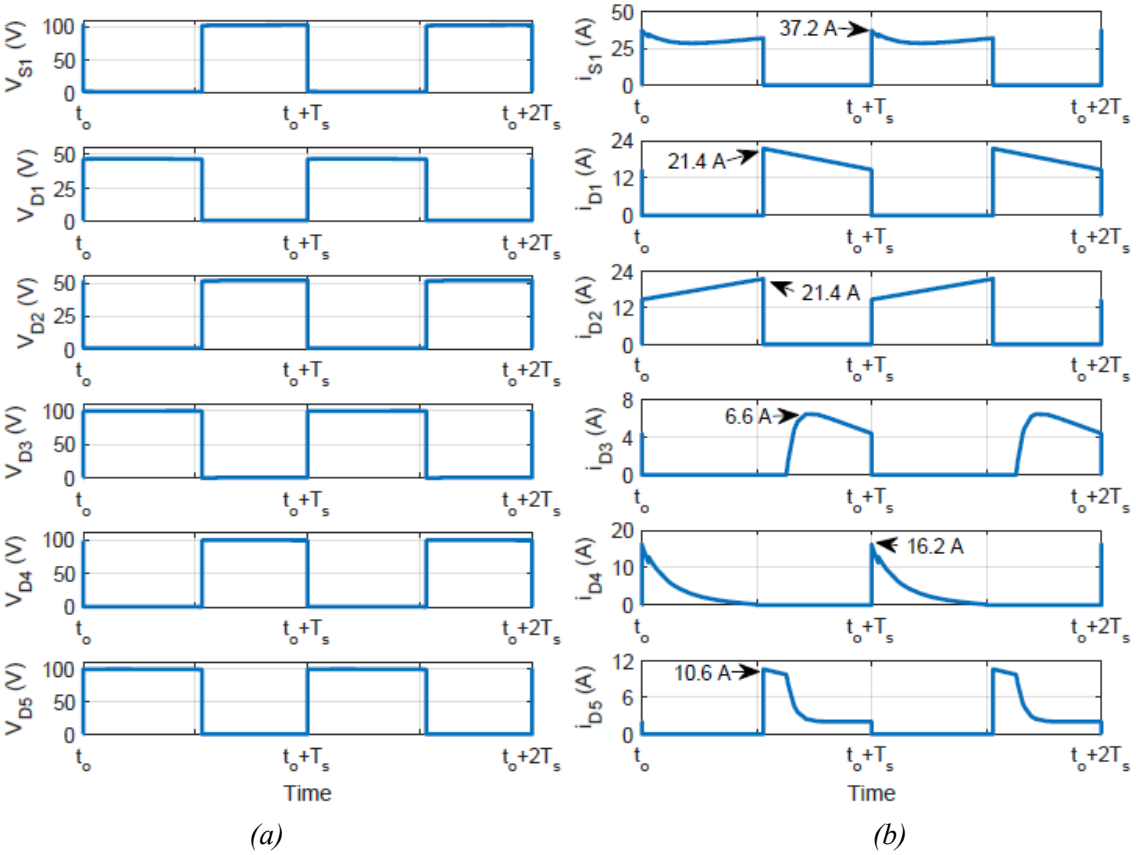



***Figure 8.*** *Semiconductor stresses a) voltage waveforms, b) current waveforms*

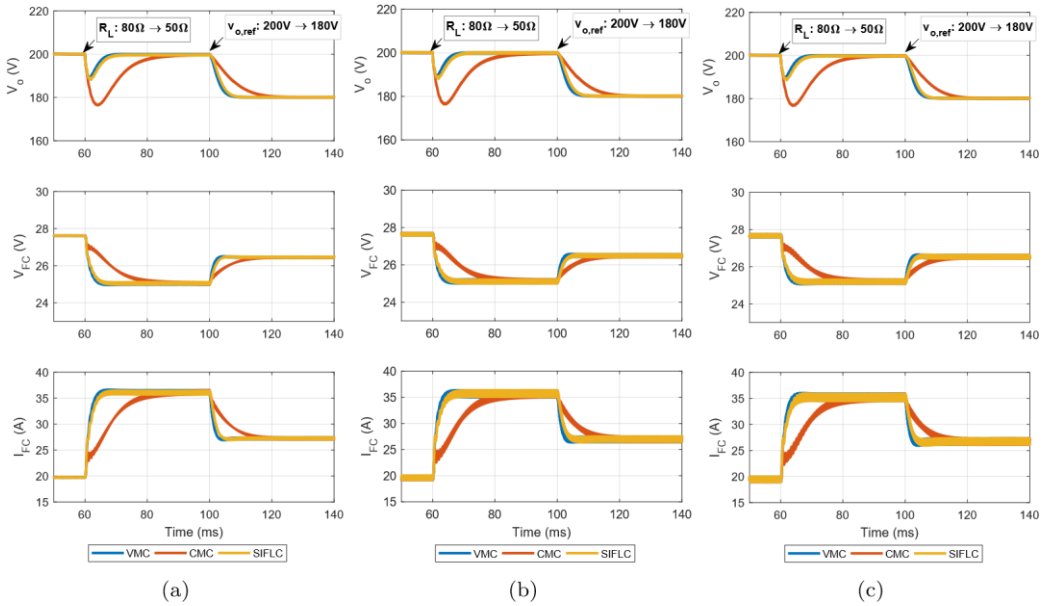



***Figure 9.*** *Output voltage, FC voltage and FC current variations in a) Case-1, b) Case-2, c) Case-3*

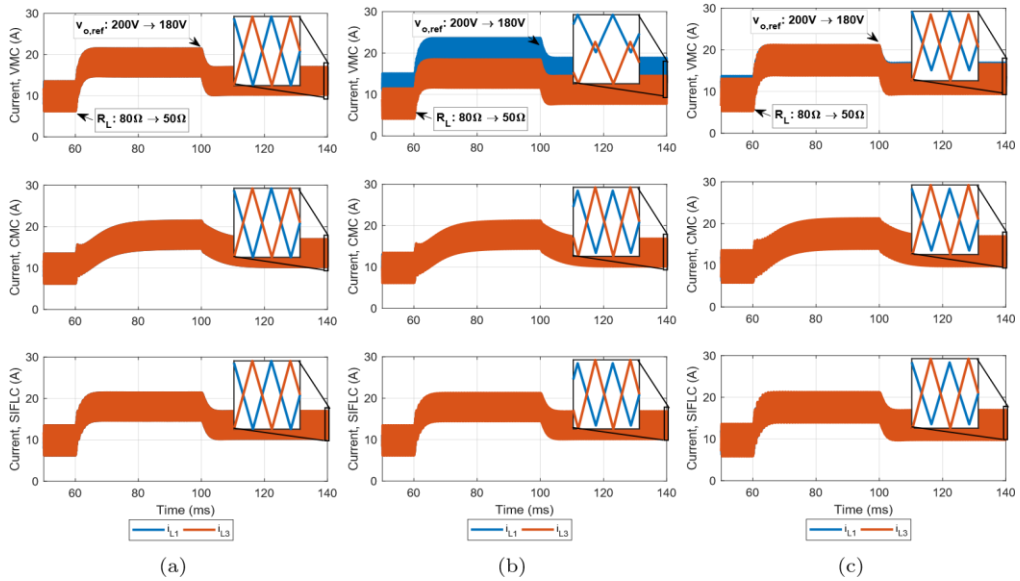



***Figure 10.*** *Inductor current variations in a) Case-1, b) Case-2, c) Case-3*

Therefore; it is clear that the current feedback should be used in the offered interleaved structure to handle the parameter tolerances. In short, it can be asserted that the SIFLC method surpasses the VMC and CMC despite its simple structure; because it simultaneously can adjust the output voltage rapidly despite the step disturbances and split the input current equally into the input inductors.

Finally, in order to test the SIFLC-controlled system under a long-lasting load demand, the average model of the converter can be built based on (4) as demonstrated in Figure 11. This average model is again created in MATLAB by PLECS Blockset. Figure 12 shows the associated simulation results in which a dynamic load demand profile of an office block provided in [49] is implemented. Firstly, it can be seen that the proposed system realizes the output voltage regulation under varying output power, where $d_1$ (similarly $d_2$) is controlled to adjust $I_{L1}$, i.e., the FC current as a result. In addition, $I_{L1}$ is about the half of the FC current owing to the interleaved operation. Moreover, Figure 12 exhibits hydrogen consumption rate ($q_{H2}$) and total hydrogen consumption ($m_{H2}$) of the FC system calculated based on the relationship provided in [50]. From this figure, one can see that $q_{H2}$ is directly proportional to the FC current and about 4L hydrogen is consumed in this simulation study.

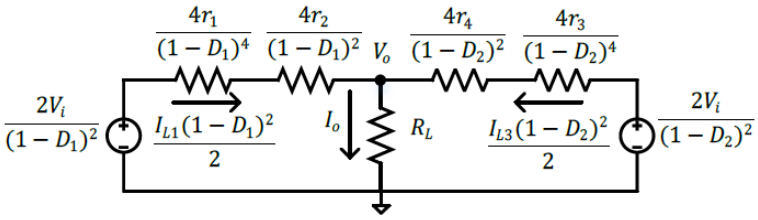



***Figure 11***. *The average model of the proposed converter*

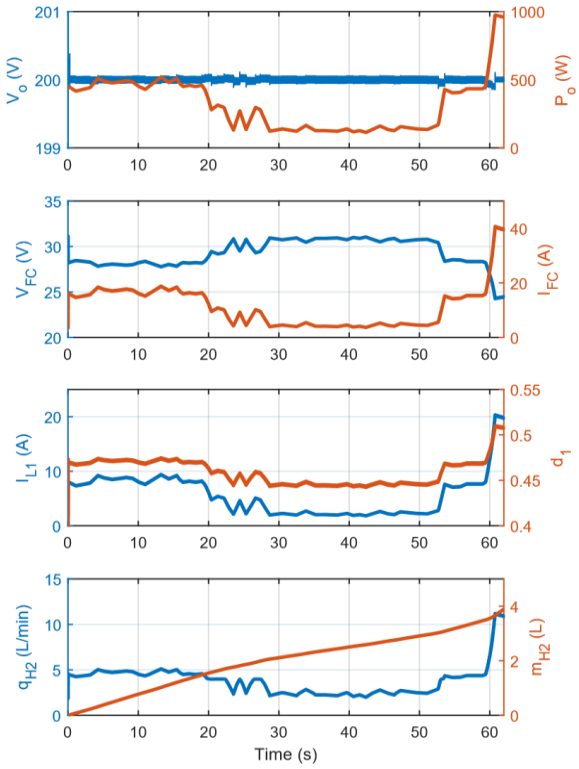



***Figure 12.*** *Dynamic simulation results*

## 6. CONCLUSION

In this article, a new high step-up interleaved DC-DC converter has been offered for FC applications, which are an integral part of the hydrogen economy. This converter can consist of unlimited QB and SC networks; therefore it allows flexibility in terms of phases and voltage gain. After elaborating on the steady-state and small-signal analyses, a design procedure along with a design example has been provided. As another contribution, this paper has proposed a SIFLC-based intelligent control method; and measured it against two classical control approaches, VMC and CMC. For the evaluation of the proposed converter and control method, a detailed simulation study has been performed. First of all, the semiconductor stress analysis has been verified by a non-ideal switching model of the converter; then it has been shown that the proposed control structure has shown good performances in regulating the output voltage and realizing current sharing in input inductors under step disturbances and altered element parameters. Finally, a long-lasting simulation study based on the average model of the proposed converter has been carried out; this study has indicated the satisfactory operation of the SIFLC when the system is subjected to the load demand of an office block.

## CONFLICTS OF INTEREST

No conflict of interest was declared by the author.

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