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DETERMINING CAPTURE CROSS SECTION FROM CAPTURE TRANSIENT SIGNALS

YAKALAMA GEÇİŞ SİNYALLERİNDEN YAKALAMA KESİT ALANINI BELİRLEME

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ABSTRACT

The characterization of defect levels within a semiconductor using capacitive methods is based on manipulating the width of the depletion region through pulsed biasing. During the measurement, the processes of charge emission and subsequent charge capture at the defect energy levels occur sequentially. The aim of this study is to investigate defect energy levels by analyzing both charge capture and emission processes and to determine the capture cross section using the capture capacitance transient signal. In this study, a method is proposed where the capture cross section could be calculated directly from the capture capacitance transient signals. The charge capture process occurs in two distinct regions, known as the fast and slow capture regions, with the slow capture region becoming dominant under specific conditions. In this study, the activation energy of the defect level in the boron-doped Si sample was determined to be in the range of 0.159–0.216 eV using the Deep Level Transient Spectroscopy (DLTS) method. The capture cross section was determined as an average of $\sigma_n = 1.03 \times 10^{-16}\text{cm}^2$ from the capacitance transient signals of the charge emission process. In contrast, when using the capture capacitance transient signals, the average value of the capture cross section was calculated as $5.62 \times 10^{-11}\text{cm}^2$.

Keywords: Capture Cross Section, Defect, DLTS, Trap.

ÖZET

Yarıiletken içerisindeki kusur seviyelerinin kapasitif yöntemlerle karakterizasyonu, arınmış bölge genişliğinin pulslu beslemeler ile manipüle edilmesine dayanır. Ölçüm sırasında, kusur enerji seviyelerinde yük yayınımı ve ardından yük yakalanması ardışık süreçler olarak gerçekleşir. Bu çalışmanın amacı, hem yük yakalama hem de yayınlama süreçlerini analiz ederek kusur enerji seviyelerini araştırmak ve yakalama kapasite geçiş sinyalini kullanarak yakalama tesir kesit alanını belirlemektir. Bu çalışmada, yakalama tesir kesit alanının doğrudan yakalama kapasite geçiş sinyalinden hesaplanabileceği bir yöntem önerildi. Yük yakalama süreci, hızlı ve yavaş olmak üzere iki farklı bölgede gerçekleşmekte olup, belirli koşullar altında yavaş yakalama bölgesi baskın hale gelmektedir. Bu araştırmada kullanılan boron katkılı Si örneğin kusur seviyesinin aktivasyon enerjisi, Derin Seviye Geçiş Spektroskopisi (DLTS) yöntemi kullanılarak 0.159-0.216 eV aralığında belirlenmiştir. Yük yayınlama sürecine ait kapasite geçiş sinyallerinden yakalama tesir kesit alanı ortalama $\sigma_n = 1.03 \times 10^{-16}\text{cm}^2$ olarak hesaplanmıştır. Buna karşılık, yakalama kapasite geçiş sinyalleri kullanıldığında, yakalama tesir kesit alanının ortalama değeri $5.62 \times 10^{-11}\text{cm}^2$ olarak hesaplanmıştır.

Anahtar Kelimeler: DLTS, Kusur, Tuzak, Yakalama Tesir Kesit Alanı.

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1. INTRODUCTION

The identification of trap levels caused by defects in semiconductor materials is crucial in semiconductor manufacturing and characterization. These trap levels, by capturing free carriers, not only alter the free carrier concentrations in the device but also act as recombination centers, reducing the device's efficiency. In particular, in optical devices, recombination centers cause non-radiative transitions, or in devices designed as solar cells or detectors, they trap free carriers generated by photons, leading to a decrease in the device's efficiency. Therefore, the characterization of trap levels is crucial for improving device design. Many common defect characterization methods are based on capacitive techniques, with one such method being deep level transient spectroscopy (DLTS) [1]. Using the DLTS method, the activation energy and concentration of defects in the semiconductor can easily be calculated. However, determining the capture cross-section requires time-consuming and repetitive experiments. DLTS methods are based on the capacitance variation in the depletion region, which changes by the applied external voltage, and the resulting capacitance transients are analyzed as a function of time as the temperature of the sample is scanned. The rate of this change in capacitance is governed prominently by the ionization rate of defect levels. The emission process of charges occurs on the order of approximately 10^{-3} seconds and can be observed with commonly used DLTS equipment. When the applied external voltage is removed or reduced, the trap levels capture charges again. The charge capture and emission processes are described by the Shockley-Read-Hall (SRH) mechanism [2,3]. For thermal equilibrium, the capture and emission rates of a trap level with an activation energy E_a at temperature T are related by the equation:

$$e_n = C_n \exp\left(-\frac{E_a}{kT}\right) \tag{1}$$

In this equation, $e_n$represents the charge emission rate, $C_n$denotes the charge capture rate, E_a is the activation energy, k is the Boltzmann constant, and T is the corresponding temperature. A rough estimate shows that at room temperature, the charge capture rate for a trap level located 0.4 eV below the conduction band is 10^6 times higher than the emission rate. Due to the much faster nature of the capture process compared to the emission process, it is challenging to observe.

When capacitive methods are applied for semiconductor characterization, it is generally assumed that there are no free charge carriers within the depletion region and that all trap levels in the region are ionized. However, Kimerling's study [4] shows that the trap levels located in the region between the depletion boundary (W) and the point where the trap energy level E_a equals the Fermi level E_F denoted as λ in Figure 1a are occupied by charges under thermal equilibrium. The same study also indicates that, when solving the Poisson equation for the depletion region, the free charge carrier concentration (n) changes from the depletion boundary toward the junction point, as given by:

$$n(x) = n_0 \exp\left[-\frac{(W-x)^2}{2L_D^2}\right] \tag{2}$$

Here, n_0 represents the free charge carrier concentration outside the depleted region, and L_D is referred to as the Debye length, expressed by Equation 3. The Debye length depends only on the dopant concentration, the material's dielectric constant, and temperature.

$$L_D = \sqrt{\frac{\varepsilon kT}{q^2 N_D}} \tag{3}$$

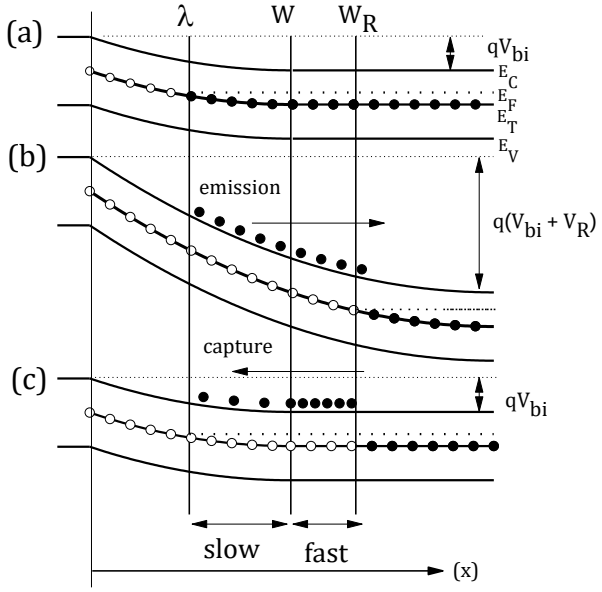

Figure 1. (a) Energy band diagram of a p^+n junction in thermal equilibrium, showing the width of the depletion region. The black circles represent occupied trap levels, while the white circles represent unoccupied trap levels relative to the Fermi level. **(b)** Energy band diagram illustrating charge emission from trap levels above the Fermi level and the change in the depletion region when external bias is applied. **(c)** Energy band diagram depicting the charge capture process of trap levels at the moment the external bias on the junction is removed.

Initially, in the thermal equilibrium state, the filled trap levels near the edge of the depleted region remain above the Fermi level when an external reverse bias is applied, allowing them to emit their charges into the conduction band, and these traps are now found in an unoccupied state (Figure 1b). The emptied trap levels fall below the Fermi level again when the reverse bias is removed, and they capture free charge carriers from the conduction band (Figure 1c). Studies by Borsuk et al. [5] and Zylbersztejn [6] show that the charge capture process occurs in two regions: fast and slow. The charge capture time constant depends on the concentration of free charge carriers and $\vartheta_{th}$the thermal velocities of the free charges, as well as σ_n the capture cross-section of the defect (Equation 4). The thermal velocities of the free carriers depend on the temperature and the effective masses of the free charges. As soon as the reverse bias is removed, the free charge carriers rapidly diffuse into the region outside the depleted area, where the concentration of free charge carriers is constant and equal to the doping concentration, and the fast capture process occurs here. Within the boundary of the depleted region, however, the carrier concentration decreases exponentially toward the junction, where the slow capture process takes place.

$$C_n = \sigma_n \vartheta_{th} n(x) = \sigma_n \sqrt{\frac{3kT}{m_n^*}} n(x) \tag{4}$$

In pulsed capacitance measurements where the capture and emission processes follow one another, both fast and slow capture processes occur. However, the measurement parameters determine the dominance of the fast and slow processes on the capacitance signal. Most of the studies conducted so far have focused on the effects of parameters related to the capture process on the emission process. Based on these effects, the defect's capture cross section has been characterized through changes in the capacitance transition signal during the defect's charge emission process. Studies employing these techniques can be found in references [7-13]. In this study our aim is to determine the capture cross section of defects directly from the capacitance transient signals observed during the capture process.

2. MATERIALS AND METHODS

A boron-doped p-type silicon wafer, purchased from an external supplier, with a resistivity of 20-50 Ohm·cm, thickness of 300 microns, and a (100) orientation, was used for the work. The p-type boron-doped Si wafer was bombarded with electrons having an energy of 40–80 GeV at the SPS North Area H2 beamline, with a particle flux of 20k particles per second. Subsequently, circular aluminum contacts with a diameter of 1 mm were deposited on the wafer using the thermal evaporation method with a mask, forming a Schottky diode. This diode was used to study the charge capture and emission processes at the defect levels. The current-voltage (IV) measurements confirmed the diode behavior, and the ionized dopant concentration was determined to be $3.5 \times 10^{14} \mathrm{cm}^{-3}$ using the capacitance-voltage (CV) method. In order to record the temperature-dependent capacitance transients during the capture and emission processes, a digital version of deep level transient spectroscopy setup was established.

DLTS is a thermal spectroscopy method. When the width of the depletion region of the sample is increased with an applied external bias, charge emission occurs from trap levels above the Fermi level to the conduction band. During the emission process, the time-dependent capacitance change of the sample is recorded for the relevant temperature. To analyze the capacitance transient signals, the difference in capacitance values at two different moments, t_1 and t_2, is plotted as a function of temperature to create a DLTS spectrum. The selected t_1 and t_2 values form a rate window. A peak appears in the DLTS spectrum at the temperature where the emission rate of the trap level matches the selected rate window. By choosing different rate windows, temperature-dependent emission values are obtained, and the activation energy of the trap is calculated using SRH statistics (see reference 1 for details).

The DLTS measurement system included a Boonton 7200 capacitance meter for capacitance transient measurements, an Agilent 81150 function generator for applying pulsed voltages, and an Agilent 3458A multimeter for digitizing capacitance signals. The system operated in vacuum to maintain temperature stability and under dark conditions to prevent light-induced effects. The temperature of the sample was controlled and measured with a Lakeshore 331 controller within the range of 300K to 100K.

3. RESULTS

The time-dependent changes in capacitance during charge emission and capture processes are described by equations 5 and 6, respectively.

$$C_e(t) \cong C_{e_{inf}} \left(1 - \frac{N_T}{2N_D} e^{-t/\tau_e}\right) \tag{5}$$

$$C_c(t) \cong C_{c_{inf}} \left[1 - \frac{N_T}{2N_D} (1 - e^{-t/\tau_c})\right] \tag{6}$$

In the equations, $C_{e_{inf}}$ represents the equilibrium capacitance value reached by the sample capacitance during emission, $C_{c_{inf}}$ represents the equilibrium capacitance value during the capture process, N_T is the trap concentration, N_D is the dopant concentration, τ_e is the emission time constant of the trap, and τ_C is the capture time constant. To observe these processes, the capacitance-voltage (CV) measurement of the sample was first performed, and the depth-dependent dopant concentration was determined. Depth-dependent defect characterization is one of the strongest features of the DLTS method, as the width of the depleted region or, alternatively, the depth to be examined can be determined by the applied voltage. Therefore, the work voltage was set to this range, corresponding to depths between 0.65V and 0.45V, due to the significant change in dopant concentration observed, which indicates the presence of thermally active traps. And the sample was subjected to a 0.45 V bias for 61 ms, during which the charge emission process occurred. This was followed by reducing the bias to 0.5 V for 60 ms, allowing the charge capture process to take place. Capacitance changes were recorded every 30 µs during these processes. Repeating the measurements 300 times helped minimize the standard deviation and enhance the signal-to-noise ratio. Figure 2 illustrates the time-dependent capacitance transients from the Si sample at different temperatures, corresponding to the capture and emission processes. As seen in Figure 2, the capacitance transient signals associated with the capture and emission processes are temperature-

dependent. In both processes, as the temperature increases, the rate of the capacitance transient signal increases. It may be possible to analyze both parts of the capacitance transient signals (capture and emission) using the DLTS method to gain more information about the trap. However, it is essential to first identify the conditions under which this analysis is feasible.

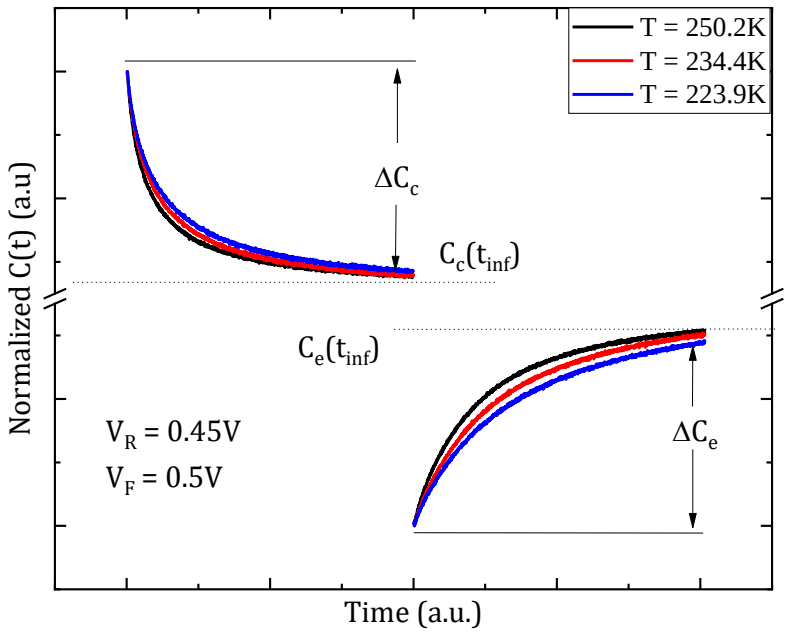

Figure 2. The variation in sample capacitance corresponding to the charge capture and emission processes within the relevant depletion region at different temperatures. The feedback voltage was reduced to 4.75 V to initiate the charge capture process and increased to 5 V for the charge emission process.

As mentioned in the Introduction, the charge capture process occurs in two distinct regions: fast and slow. The capture process manifests as a superposition of these two regions. Therefore, Equation 6 can be expressed by separating the fast and slow capture processes as follows:

$$C_c(t) = C_{c_{inf}}\left[1 - \frac{N_{T_{fast}}}{2N_D}\left(1 - e^{-t/\tau_{c_{fast}}}\right) - \frac{N_{T_{slow}}}{2N_D}\left(1 - e^{-t/\tau_{c_{slow}}}\right)\right] \quad (7)$$

Since the charge capture and emission processes follow each other, this implies that when the applied reverse bias voltage is increased, the defects remain above the Fermi level and emit charges; conversely, when the feedback voltage is reduced, they capture charges. In this case, the amplitudes of the capacitance transient signals corresponding to these two different processes should be similar. However, our measurements indicate that the amplitude of the capacitance signal associated with the capture process is smaller than that of the emission signal. In this study, the changes in the capacitance signal were recorded at a rate of 30 μs^{-1}. Generally, the charge capture time constant for defect levels ranges from picoseconds to milliseconds. The recording speed of the capacitance transition signals in this study was only sufficient to capture the slow capture processes, as the fast capture process occurred before a sufficient number of data points could be collected.

As the difference between the applied voltages during the capture and emission processes increases, the width of the depletion region where the fast capture process occurs will also increase. In this case, the amplitude of the transient signal associated with the charge emission process for the relevant defects

will increase. However, since the major part of the capture process occurs rapidly, it can not be recorded. Therefore, as the difference between the voltages corresponding to the capture and emission processes increases, the ratio of the amplitude of the capture signal to that of the emission signal will decrease.

Figure 3 illustrates the DLTS spectra for capture and emission signals obtained at a rate window of 48.7 s^{-1}, with an emission voltage of 0.45 V and a capture voltage of 0.5 V, in the temperature range of 300 K to 100 K. As shown in Figure 2, the capacitance transient signal consists of two parts: capture and emission. Accordingly, the DLTS spectrum marked as 'capture' in Figure 3 is derived from the capacitance change in the capture part of the capacitance transient signal, while the 'emission' part corresponds to the capacitance change in the emission section of the signal. As indicated in Equations 5 and 6, the processes are reversible, leading to symmetrical spectra. To clearly observe the alignment with the emission process, the capture DLTS spectrum has been inverted (Figure 3b).

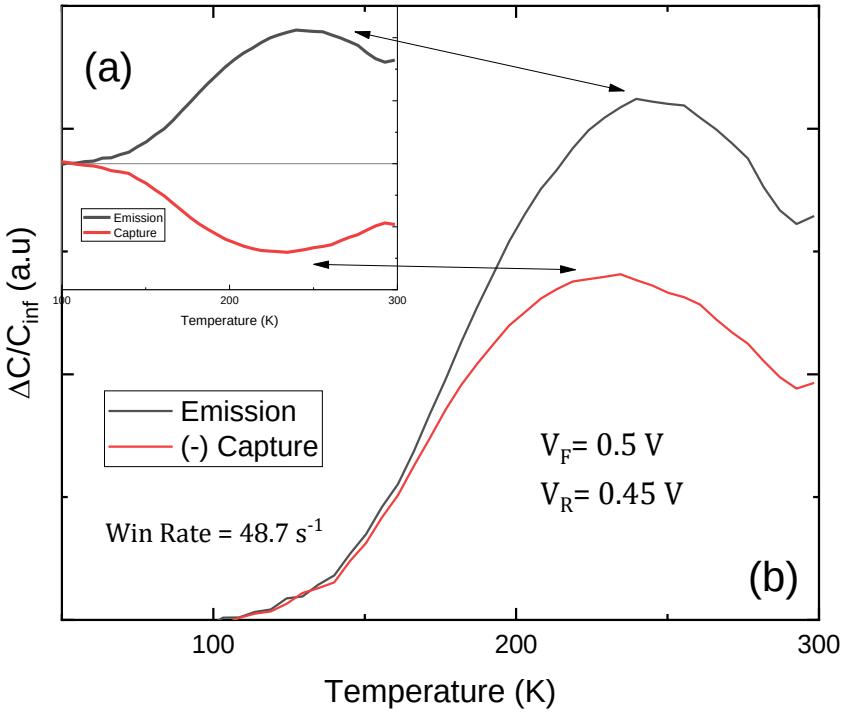

Figure 3. (a) DLTS spectra obtained from the capacity transition signals associated with capture and emission, recorded at a rate of 48.7 s^{-1}. **(b)** The capture spectrum is multiplied by (-1) for better visualization of the spectrum alignment.

In the DLTS spectra of the emission and capture processes, the peak corresponding to the trap indicated by the arrow in Figure 3 shows a lower amplitude for the capture process. This is because the rapid capture transition could not be adequately measured.

Consequently, at a temperature of 250K where the trap is active, the emission voltage was kept constant at 0.45 V, while the capture voltage was set to 0.65V, 0.6V, 0.55V and 0.5V to decrease the width of the depletion region and observe the effect of the fast and slow capture processes more distinctly. Adjusting the differences between these voltages allowed for the differentiation of fast and slow capture processes.

To observe both processes over approximately the same time frame, the capture time was set to 60 ms, and the emission time to 61 ms. Additionally, to reduce the noise in the signal, each measurement was repeated 300 times, and the average was taken. Figure 4 shows the amplitude of the capture capacitance transition signal relative to the emission signal for different capture voltages.

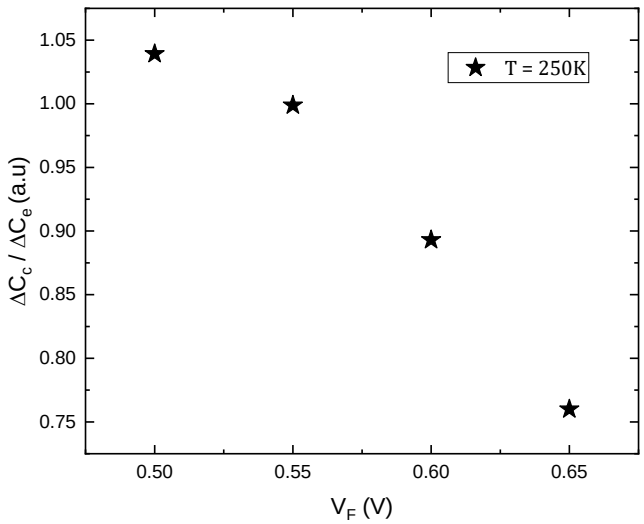

Figure 4. Variation of the ratio of capture and emission capacitance transient signal amplitudes at different capture voltage values at 250K temperature.

As the difference between the capture and emission voltages decreases, the fast capture region's influence wanes, giving way to a more prominent slow capture region. This change allows both the trapping (capture) and release (emission) processes to be detected in the capacitance transient signal amplitude. When the emission and capture amplitudes are equal, it indicates that both processes are being observed effectively. To study the temperature dependence of the slow capture region, measurements were repeated at different temperatures. Figure 5 shows how the ratio of the capture to emission signal amplitudes changes with temperature. For all capture voltage values at the same emission voltage, this ratio decreases as the temperature increases. As will be shown in the following section, the change in free charge carrier concentration causes the fast capture process to become dominant over the slow capture process as the temperature increases.

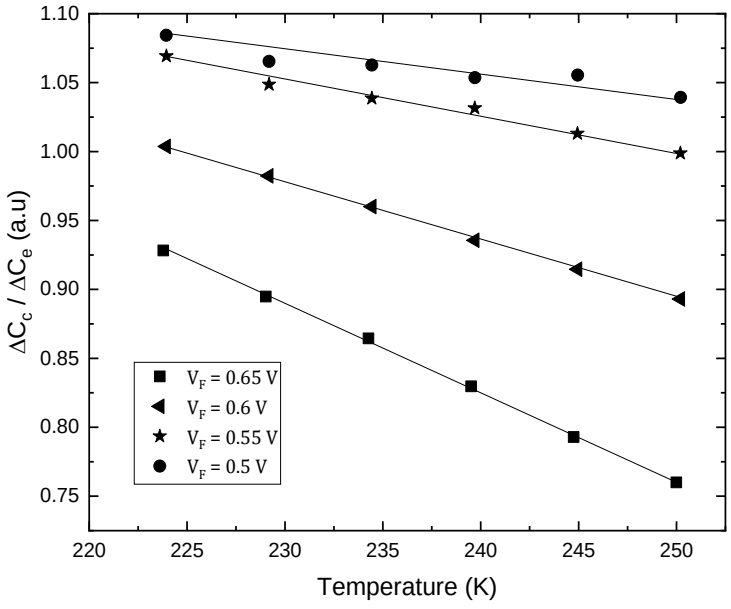

Figure 5. Temperature-dependent variation of the ratio of capture to emission capacitance transient signal amplitudes.

The capture and emission rates exhibit an exponential increase with temperature; this exponential behavior for the emission rate aligns with expectations from the Shockley-Read-Hall (SRH) mechanism. The activation energy of the defect is determined from the temperature-dependent emission rates using Equation 8 [1]. The Arrhenius plots constructed from the emission rates associated with the emission process in the capacitance transient signals are presented in Figure 6. Averaging across all capture voltage values, the activation energy is calculated to be 190 ± 25 meV. The γ value obtained from the graph intercepts allows for the determination of the capture cross-section of the trap, which is between $1.22 \times 10^{-16} - 5.61 \times 10^{-17} \mathrm{cm}^2$.

$$\ln(e_n/T^2) = \ln\gamma + (1000/T)(-E_a/1000k) \tag{8}$$

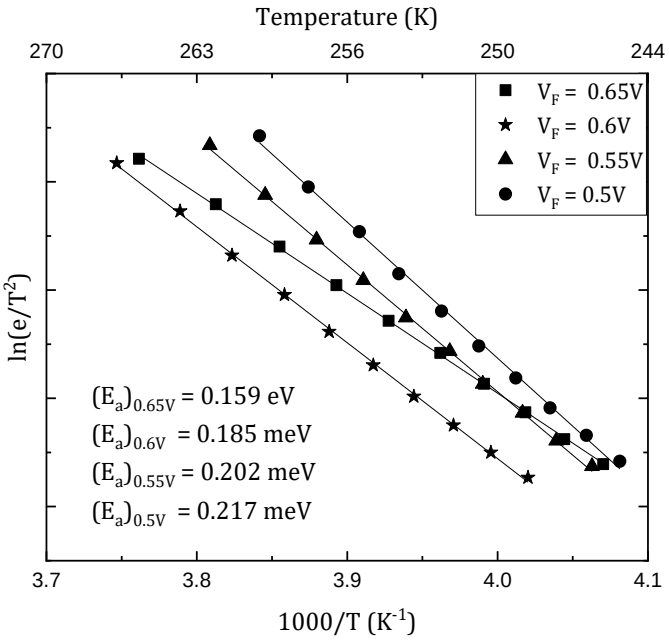

Figure 6. Arrhenius plots obtained from the temperature-dependent emission rates for different capture voltage values. The average trap activation energy is calculated to be 190 ± 25 meV. The intercepts also give rise to similar capture cross section values that averages to $1.12 \times 10^{-16} \mathrm{cm}^2$with a standard deviation of $\pm 1.03 \times 10^{-16} \mathrm{cm}^2$.

The free charge carrier concentration n(x) is equal to the doping concentration N_d in all neutral regions outside the depletion region. As one moves from the depletion region boundary toward the junction, the potential barrier height $\Delta\Psi(x)$ that the carriers will encounter increases. The change in carrier concentration corresponding to the barrier height increase is given by Equation 9. Accordingly, the free carrier concentration decreases exponentially from the depletion region boundary toward the junction region and eventually depletes [5].

$$n(x) = N_d \exp\left[-\frac{q|\Delta\psi(x)|}{kT}\right] \tag{9}$$

Since the trap energy level's charge capture rate depends on the carrier concentration, the charge capture rate in the fast capture region (Figure 1) can be expressed by Equation 10, while in the slow capture region, it is represented by Equation 11.

$$C_n(x) = \sigma_n \vartheta_{th} N_d\,, \qquad W < x < W_R \tag{10}$$

$$C_n(x) = \sigma_n \vartheta_{th} N_d \exp\left[-\frac{q|\Delta\psi(x)|}{kT}\right], \qquad \lambda < x < W \tag{11}$$

Here, W is the depletion region boundary while the capture voltage is applied, and W_R is the depletion region boundary while the emission voltage is applied. The point λ corresponds to where the Fermi level E_F equals the trap energy level E_T. The thermal velocities of free carriers, $\vartheta_{th} = \sqrt{3kT/m_n^*}$, depend on temperature and the effective masses of the carriers. Equation 11 can be rearranged as in Equation 12, and by the help of an Arrhenius plot (Figure 7), the barrier height and capture cross-section can directly be calculated from the graph.

$$\ln\left(\frac{C_n}{\sqrt{T}}\right) = \ln\left(\sigma_n N_d \sqrt{\frac{3k}{m_n^*}}\right) + \left(-\frac{q|\Delta\psi(x)|}{1000k}\right)\left(\frac{1000}{T}\right) \tag{12}$$

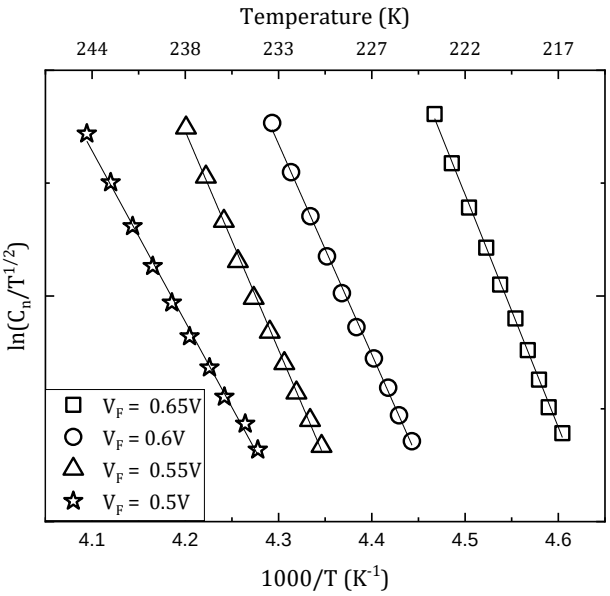

Figure 7. Arrhenius plot illustrating the temperature-dependent capture rates used to determine the capture cross-section and barrier heights. The plot displays four linear lines, each corresponding to different capture voltages indicating the effect of fast capture process becoming more dominant with increasing pulse heights.

Using capacitance-voltage (CV) measurements, the free carrier concentration, attributed to the doping concentration, was determined to be $3.5 \times 10^{14}\text{cm}^{-3}$. The effective mass of the p type Si carriers was taken as $0.5m_0$. The calculated capture cross-section values corresponding to the different applied capture voltages and the heights of the potential barriers are shown in Table 1.

Table 1. Capture Cross-Section Values and The Heights of Potential Barriers Corresponding to The Different Applied Capture Voltages

Emission Voltage (V)	Capture Voltage (V)	q|Δψ(x)| (eV)	Capture Cross Section (cm^{-2})
0.45	0.65	0.44	2.02×10^{-10}
0.45	0.6	0.40	9.64×10^{-12}
0.45	0.55	0.42	1.30×10^{-11}
0.45	0.5	0.33	1.04×10^{-13}

According to the Table 1, as the difference between the capture and emission voltages increases, both the calculated capture cross-section values of the defect and the average potential barrier heights at which the capture process occurs show an increasing trend. This observation suggests an important relationship between voltage differences and the calculated defect parameters, potentially impacting our understanding of defect behavior in the material.

4. DISCUSSION AND CONCLUSION

This study demonstrates that the capture process consists of two parts, and as the difference between the capture and emission voltages decreases, the effectiveness of the slow capture region within the depletion region increases. It was observed that the width of the slow region depends also on temperature, with its influence diminishing as the temperature rises. This is because the slow capture process directly depends on the decrease in carrier concentration toward the junction region, and the carrier concentration itself is an exponential function of both the potential barrier height near the junction and temperature. As temperature increases, the exponential term becomes negligible, causing the slow capture rate to converge toward the rate formulation of the fast capture process. This indicates that the fast and slow charge capture behaviors of defects are related to their positions within the junction region. Since this directly affects the operational efficiency of devices, it is a critical parameter that must be considered in defect characterization and device design. The trap activation energy calculated from the analysis of the capacitance transient signals related to emission was found to be around 0.159–0.216 eV, while the capture cross section was determined to be $1.12 \times 10^{-16} \pm 1.03 \times 10^{-16} \mathrm{cm}^2$. The reason for this variation in the energy range is that, as seen from the width of the DLTS spectrum, the DLTS peak corresponds to multiple defects with closely spaced energy levels rather than a single, well-defined defect. Instead of a sharp peak representing a single defect, the defects behave like a band consisting of closely spaced energy levels. As the voltage range changes, the dominance of one defect over another shifts, and the activation energy obtained from the spectrum corresponds to the most dominant defect. The capture cross section obtained from the capture capacitance transient signal was calculated to be in the range of $10^{-10}\mathrm{cm}^2$ to $10^{-13}\mathrm{cm}^2$. The significant discrepancy and the tendency not to report capture cross section values or to do so with uncertainty in many defect characterization studies arise from the inconsistencies encountered when using emission rates to determine the capture cross section [7, 14-17].

Determining the capture cross sections of traps in a semiconductor device is crucial, as the operation of most devices relies on the capture and emission processes. In this study, the mechanisms of slow and fast charge capture processes of defects located in the junction region were identified. In addition to analyzing the charge emission processes of traps, examining their charge capture processes can also be utilized for trap characterization, particularly in calculating the capture cross section. The method can be better tested and improved in the presence of a well-known defect with a homogeneous distribution throughout the sample. This would allow for more precise and detailed calculations of the capture cross section's dependence on temperature and its position within the sample. As semiconductor device dimensions continue to shrink with advancing technology, even the smallest defects have become critical parameters, making defect characterization increasingly important. The development of the technique proposed in this study could contribute to capacitive defect characterization methods by introducing a new approach.

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