




DESIGN OF ADAPTIVE TRANSVERSAL FILTER UNDER RANDOM DELAY VARIATIONS


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Highlights

- Cascaded small delay elements enhance precision of delay taps.
- Neural network adapts delay errors in transversal filters in real time.
- Adaptive filtering improves reliability in semi-digital transversal filters.
- Proposed method significantly reduces timing errors in high-speed systems.
- Simulation results show enhanced accuracy over conventional filters.

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ABSTRACT: Transversal filters consist of fundamental circuit elements such as adders, multipliers, and unit delay elements. The performance of these filters is affected by inaccuracies in these components, particularly limited precision in delay elements, which becomes significant in high-frequency semi-digital transversal filters. This letter proposes a cascaded delay element structure to mitigate precision errors. The main delay element is complemented by smaller cascaded delay elements, refining overall delay precision. To further enhance accuracy, a neural network (NN)-based adaptation scheme dynamically fine-tunes delay adjustments in real time. The proposed two-layer NN takes inputs from both the primary and cascaded delay elements and generates an optimized output for the next delay stage. The input layer neurons are randomly initialized, while the NN weights are iteratively updated using gradient descent to minimize errors. The neural network weights are determined during an initial factory-calibration stage and remain fixed during all subsequent filter operation. Simulation results demonstrate that the cascaded delay structure, combined with NN adaptation, significantly reduces precision errors, enhancing semi-digital transversal filter performance for high-speed signal processing applications.

Keywords: Neural Networks, Random Delay Errors, Transversal Filters

1. INTRODUCTION

Inter-symbol interference (ISI) remains a critical challenge in high-speed digital communications, where channel dispersion causes symbols to overlap and degrade signal integrity [1]–[3]. A common remedy is to employ an equalizer at the receiver—typically realized as a tapped-delay-line finite-impulse-response (FIR) filter (often called a transversal filter)—to approximate the inverse channel response and restore the transmitted waveform [4], [5]. While digital implementations of such filters leverage high-speed ADCs and shift-register based unit delays [6]–[9], they incur significant complexity, latency, and power consumption at multi-gigahertz rates.

Analog and mixed-signal transversal filters eliminate the need for full-rate digitization by implementing delay cells, multipliers, and adders in continuous-time or semi-digital domains [10]–[13]. The CMOS FIR filter in [12] employs a fixed resistor-ladder weighting and capacitor-integration scheme to achieve low phase distortion and power-independent tap count, but its entirely static architecture cannot correct for run-time delay jitter or process, voltage, temperature (PVT) -induced timing variations.

Coefficients are commonly realized via capacitor or resistor ratios [13], current-source ratios [14], or resistor ladders [15], yielding high energy efficiency. However, analog delay elements are inherently vulnerable to random variations due to PVT shifts and fabrication mismatches which introduce timing jitter and phase errors that distort the filter's frequency response [10], [15]. Early works often assumed that delay errors were negligible under a stable clock, focusing instead on coefficient mismatches [10]–[12]. More recent statistical studies have characterized the impact of random delay deviations on transfer-function amplitude and phase [16], and Akyuz's thesis [17] provided a detailed analysis of how such jitter accumulates in N-tap filters.

To mitigate delay-induced distortions, several calibration and compensation strategies have been explored outside the direct context of transversal filters. Authors in [18] introduced off-line and blind on-line digital calibration for analog ADC errors, demonstrating that one-time or periodic tuning can

substantially reduce circuit non-idealities. Digital equalization techniques in adaptive spatial filtering to cancel noise-like interferences are applied in [19], illustrating how FIR filters can correct analog deviations via iterative algorithms. In RF front-ends, Lim et al. [20] used adaptive FIR filters for digital compensation in IQ modulators, while Shyu and Chang [21] incorporated phase-compensation in FIR structures to improve active noise control. Authors in [22] proposed a reduced-bias delay-lock loop for adaptive filters, achieving hardware-level correction of timing offsets. More recently, [23] addresses process-variation compensation in analog neural-network processors, and various works have employed neural networks for error correction in pipelined ADC stages [24] and in all-analog equalizers for coherent optical receivers [25].

In addition, related adaptive-filter techniques such as transform-domain adaptive filtering for GPS delay spoofing reduction [26] and microcomb-based photonic transversal processors [27] demonstrate the breadth of domains where timing errors must be mitigated. Foundational analyses in [28] and [29] quantified how switching-instant fluctuations in switched-capacitor networks introduce noise, reinforcing that timing uncertainty is a ubiquitous hardware concern.

Despite this extensive body of work on calibration, compensation, and statistical analysis, no prior study has demonstrated a lightweight, real-time compensation mechanism for random delay variations within a transversal filter itself, using a factory-trained neural network that requires no on-line weight updates. Existing methods either rely on continuous adaptation (e.g., LMS pipelines [19]), dedicated analog control loops (e.g., delay-lock loops [22]), or one-time off-line calibration tailored to specific components (e.g., ADCs [18]), but do not address dynamic, in-operation delay jitter in FIR filters.

In this paper, we fill that gap by proposing a cascaded delay-cell architecture augmented with a two-layer neural network whose weights are determined during an initial factory calibration. Once deployed, the NN whose input consists of signals tapped at multiple points along each cascaded delay line immediately compensates for delay errors through a single feed-forward inference, without iterative updates. This approach affords real-time error correction, low hardware overhead compared to continuous-adaptation schemes, and robustness to PVT-induced delay perturbations. The remainder of this paper details the design, calibration procedure, and performance evaluation of the proposed adaptive transversal filter.

2. MATERIAL AND METHODS

The transfer function of an FIR filter in direct form is represented as follows

$$H(w) = \sum_{k=0}^{N-1} h_k e^{-jwkT} \quad (1)$$

where w is the angular frequency, N is the number of taps, h_k are filter coefficients and T is the unit delay duration. Representation of the FIR filter with errors in the delay taps is in Figure 1. δ_i is the error in the i^{th} delay element. Ideal filter coefficients are assumed through the manuscript to simplify the calculations. From the structure of the filter, an error in k^{th} delay element effects the subsequent taps, from $(k + 1)^{th}$ to the last one, therefore, delay errors appear cumulatively. Transfer function with the errors in delay taps becomes [2]

$$\hat{H}(w) = \sum_{k=0}^{N-1} h_k e^{-jw(kT + \sum_{i=1}^k \delta_i)} = \sum_{k=0}^{N-1} (h_k e^{-jw(\sum_{i=1}^k \delta_i)}) e^{-jwkT} \quad (2)$$

As can be seen from (2), inaccuracy effects make the filter coefficients complex and this result non-conjugate complex zeros. Considering the statistical variations, an accurate model for CMOS inverter delay errors is presented in [7]. Referring to this model, it is assumed through the paper that the delay errors are Gaussian distributed with zero mean and standard deviation of 2%. Using this information, a comb filter with and without errors in delay taps is demonstrated in Figure 2. As can be seen from the figure, the filter does not satisfy the required response in some notch points in the presence of errors on

the unit delay elements.

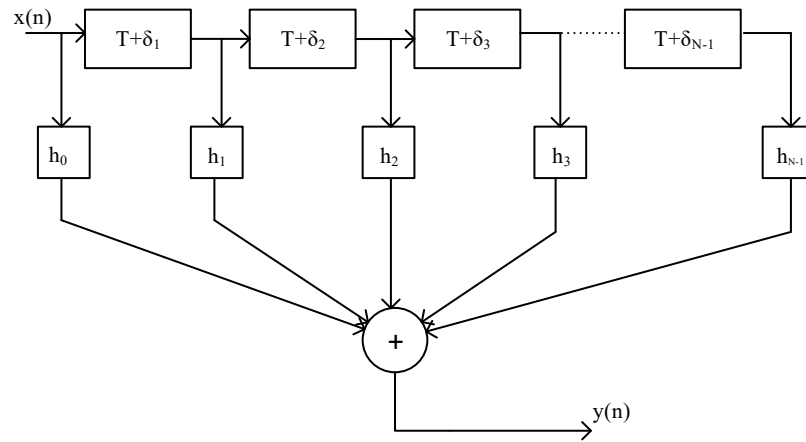


Figure 1. A direct-form FIR filter design incorporating random errors in delay taps.

To simplify the equations, define $\Delta_k = \sum_{i=1}^k \delta_i$ for $1 \leq k \leq n-1$ and to see the error effect in frequency domain, the transfer function of the filter without delay error is subtracted from the transfer function with delay error as [16]

$$|H_{\Delta}(w)| = |\hat{H}(w) - H(w)| = \left| \sum_{k=0}^{N-1} h_k e^{-jwT} (1 - e^{-jw\Delta_k}) \right|. \quad (3)$$

Assuming the accumulated delay error, Δ_k , has a standard deviation much smaller than the unit delay itself, using Taylor series expansion

$$e^{-jw\Delta_k} = 1 - jw\Delta_k + \frac{(jw\Delta_k)^2}{2} - \dots \approx 1 - jw\Delta_k \quad (4)$$

Then the magnitude error is simplified as [16]

$$|H_{\Delta}(w)| \approx \left| \sum_{k=0}^{N-1} h_k e^{-jwT} (1 - (1 - jw\Delta_k)) \right| = \left| \sum_{k=0}^{N-1} h_k e^{-jwT} jw\Delta_k \right| \quad (5)$$

If we rewrite the equation (5) using Euler transform

$$\begin{aligned} |H_{\Delta}(w)| &= \left| \sum_{k=0}^{N-1} h_k ((\cos(wkT)) - j\sin(wkT)) jw\Delta_k \right| \\ &= \left| \sum_{k=0}^{N-1} h_k w\Delta_k (\sin(wkT) + j\cos(wkT)) \right| \end{aligned} \quad (6)$$

Equation (6) can be expressed using its real and imaginary components as follows

$$|H_{\Delta}(w)| = \sqrt{A^2(w) + B^2(w)} \quad (7)$$

where

$$A(w) = \sum_{k=0}^{N-1} h_k w\Delta_k \sin(wkT) \quad \text{and} \quad B(w) = \sum_{k=0}^{N-1} h_k w\Delta_k \cos(wkT) \quad (8)$$

Although errors occur randomly, the statistical analysis of the transfer function's magnitude can still be performed. Since δ_i are typically independent Gaussian random variables, Δ_k become dependent Gaussian random variables. Consequently, $A(w)$ and $B(w)$ are jointly Gaussian random variables. By computing the expected values and variances of $A(w)$ and $B(w)$, and then applying a change of variables to express the transfer function in terms of its magnitude and phase, we can derive statistical properties of the system's response [17].

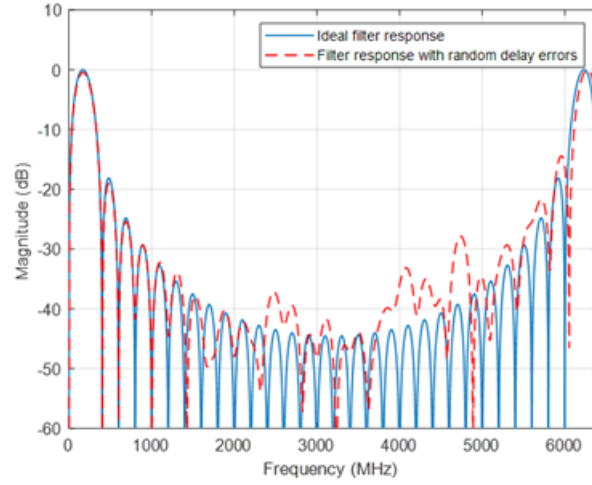


Figure 2. Frequency response of a 32-tap comb filter with imperfect delay elements

$$R(w) = \sqrt{A^2(w) + B^2(w)} \text{ and } \Theta(w) = \arctan \frac{B(w)}{A(w)} \quad (9)$$

The pdf of the error in transfer function magnitude becomes [16],[17]

$$f_R(r) \approx \frac{(\sigma_A(w)^2 + \sigma_B(w)^2)r}{2\sigma_A(w)^2\sigma_B(w)^2(1-\rho(w)^2)} e^S \quad (10)$$

where $S = \frac{-(\sigma_A(w)^2 + \sigma_B(w)^2)r^2}{4\sigma_A(w)^2\sigma_B(w)^2(1-\rho(w)^2)}$, $\sigma_A(w)$ and $\sigma_B(w)$ are standard deviations of $A(w)$ and $B(w)$ respectively and $\rho(w) = \frac{E[A(w)B(w)]}{\sigma_A(w)\sigma_B(w)}$. The probability density function (pdf) derived in (9) follows a Nakagami-Hoyt distribution. Detailed explanations can be found in [17].

Proposed Adaptive Solution

In this section, we propose a compensation mechanism to mitigate inaccuracies in delay taps caused by process variations. Due to fabrication imperfections, the actual delay duration T fluctuates approximately within the range $(T - \sigma_1)$ to $(T + \sigma_1)$, where σ_1 represents the standard deviation of the primary delay tap. To address this issue, we propose a novel approach in which delay taps are intentionally designed with a duration of $(T - \sigma_1)$, ensuring a consistent baseline delay. To compensate for the missing delay component (σ_1) and fine-tune the total delay to precisely T , we introduce L additional small delay taps, each with a standard deviation of $(\sigma_1 + \sigma_2) / 2$, where $\sigma_2 < \sigma_1$. These smaller delay taps are cascaded with the main delay element, providing finer granularity for delay adjustments.

A two-layer neural network (NN) is employed to dynamically adjust the weights of these small delay taps to achieve the target delay of T . The output of each small delay tap, along with the main delay tap, serves as input to the NN, which optimizes their combined effect. The input layer weights are initialized as constant random values, while the hidden layer weights are dynamically updated using the gradient descent algorithm. This adaptive framework enables precise compensation of delay variations, significantly reducing timing errors and enhancing the reliability of semi-digital transversal filters in high-speed applications.

$$Y = \widehat{W}^T [1 \quad \Psi(VX)^T] \quad (11)$$

Where Y is the output of delay block, $\widehat{W} = [\widehat{w}_0 \quad \widehat{w}_1 \quad \dots \quad \widehat{w}_L]^T \in \Re^{L+2}$ is the dynamical output layer neurons' vector, $V \in \Re^{(L+2) \times (L+2)}$ is the randomly assigned constant hidden layer neurons' matrix, Ψ is the activation function and

$X = [X_1 \quad X_2 \quad X_3 \quad X_4]^T \in \Re^L$ is the NN input vector defined as
 $X_1 = X_r(t - (T - \sigma_1 + \xi))$

$$X_2 = X_r(t - (T - \sigma_1 + \xi - (L - 1)\sigma))$$

$$X_L = X_r(t - (T - \sigma_1 + \xi - \sigma)).$$

The difference between output of the NN and the desired output Y_r is defined as (12)

$$e = Y_r - Y \quad (13)$$

As shown in Figure 2, adaptation law of the dynamical NN weights is defined by using standard gradient decent algorithm. First, define a quadratic cost function of the error (13) as

$$C = \frac{1}{2}e^2 \quad (14)$$

Taking derivative of the cost function (14) with respect to the dynamical weights yields

$$\frac{\partial C}{\partial \hat{W}} = e \frac{\partial e}{\partial \hat{W}} = e[1 \quad \Psi(VX)^T] \quad (15)$$

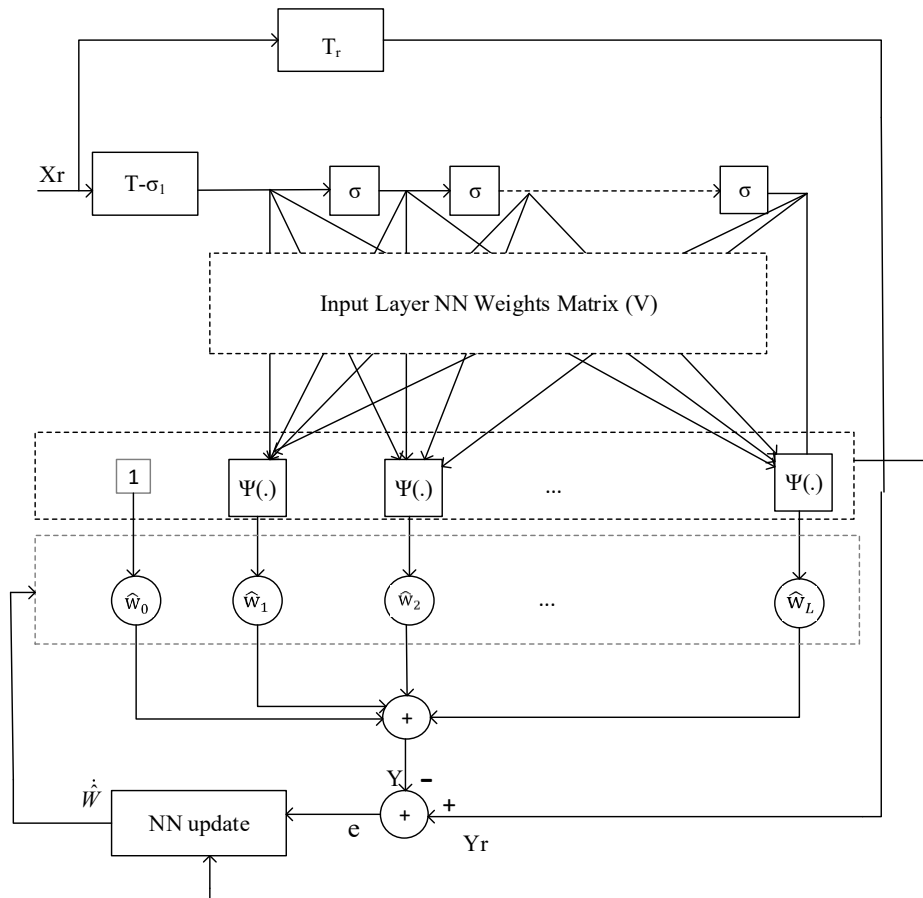


Figure 3. Cascaded block consists of main and small delay elements.

Then, the gradient decent based adaptation law for the dynamical NN weights is given as

$$\dot{\hat{W}} = -k_w \frac{\partial C}{\partial \hat{W}} = -k_w e[1 \quad \Psi(VX)^T] \quad (16)$$

with k_w being a small positive constant design parameter which is called the 'learning rate'.

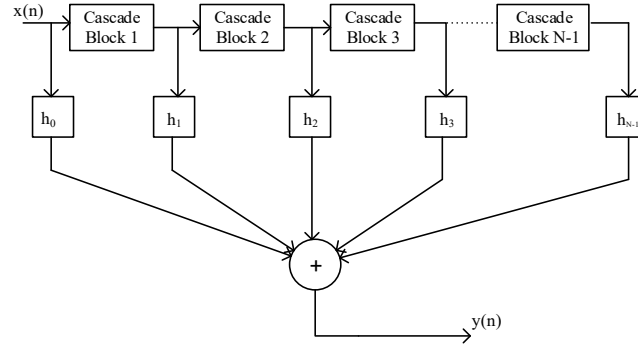


Figure 4. Overall filter design by using cascaded blocks

Figure 3 illustrates the overall neuro-adaptive filter design which consists of the adaptive cascaded delay blocks as given in Figure 4.

3. RESULTS AND DISCUSSION

To verify performance of our neuro-adaptive filter design, MATLAB/Simulink based simulation results are presented. For this purpose, a sinusoidal input signal, $X_r(t)$ is generated and the desired output is defined as $Y_r(t) = X_r(t - T)$. The delay element is assumed to have imperfection rate of σ_1 with the upper bound of $|\sigma_1| \leq \sigma_1^M$ where $\sigma_1^M = 0.02T$. Therefore, a main block with delay rate of $T - \sigma_1^M = 0.98T$ is used whereas eight small delay elements are used each with delay rate of $\sigma = \frac{\sigma_1^M + \sigma_2^M}{8}$ where $\sigma_2^M = 0.02(T - \sigma_1^M)$ is the upper bound of the imperfection rate satisfying $|\sigma_2| \leq \sigma_2^M$. Imperfection on the small delay elements is neglected. The two-layer NN is fed by 10 inputs: Output of the main block, output of eight small blocks, and one bias input. Constant input layer NN weights, $V \in \mathbb{R}^{10 \times 10}$ are chosen randomly around 0~1. Initial values of the estimated hidden layer weights $\hat{W}(0) \in \mathbb{R}^{10}$ are fixed to 0.1. The NN learning rate is defined as $k_w = 0.0002$.

To illustrate effectiveness of our neuro-adaptive filter design, the simulation compares results of two different 32 tap filters. First, results of the neuro-adaptive filter are provided, then the regular filter's results are given. In both cases, the imperfection rates of the delay elements are chosen the same.

Case 1: Neuro-adaptive filter: As illustrated in Figure 5, the error between the desired output and the output of the neuro adaptive block converge to a small value $|Y_r - Y| \leq 0.02$ after the 2000th seconds or 34 minutes

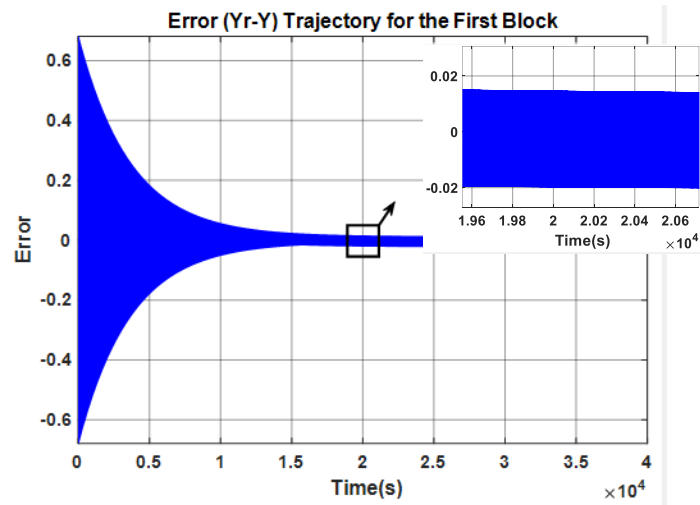


Figure 5. Error between desired output and the output of the neuro-adaptive delay blocks.

As shown on Figure 6, frequency response of the 32-tap filter consists of neuro adaptive delay taps is close to the ideal response. However, there are still small errors due to NN approximation error. Convergence of the dynamical hidden layer NN weights is given on Figure 7. Each trace represents one NN weight's value over time; all converge to their calibrated final values.

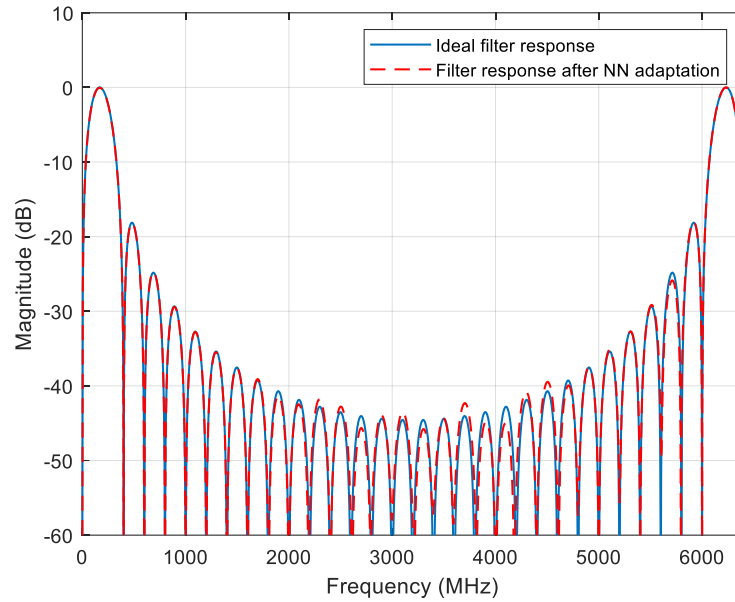


Figure 6. Frequency response of the neuro adaptive 32-tap filter with imperfect delay elements.

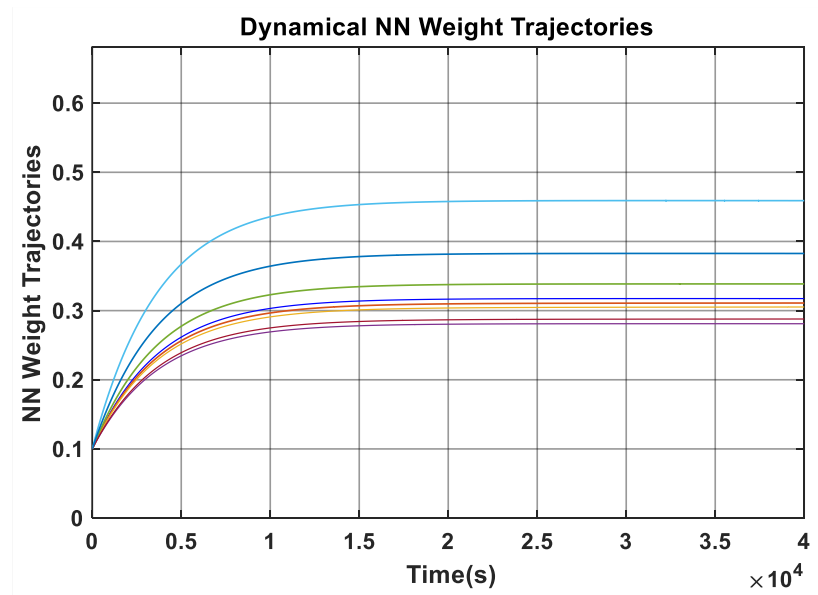


Figure 7. Trajectories of the hidden layer NN weights.

Case2: Regular filter with imperfect delay elements: Figure 8 shows the error between the ideal output and the filter output when each delay cell is perturbed to $T + \sigma_1$. By comparing Figures 5 and 8, it is clear that the error in Figure 8 is roughly an order of magnitude larger than in Figure 5.

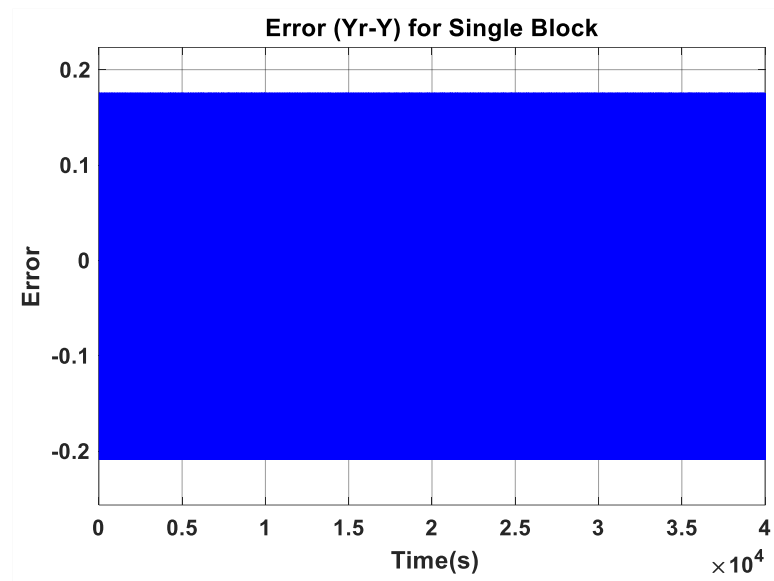


Figure 8. Error between desired output and the output of the regular delay element with imperfection.

4. CONCLUSIONS AND FUTURE WORK

The results presented in this letter demonstrate a resilient filtering approach that effectively mitigates imperfections in delay elements, ensuring improved performance in semi-digital transversal filters. To achieve this, we proposed a neural network (NN)-based adaptive filter design, which dynamically compensates for delay variations.

This approach was implemented by cascading small delay elements alongside the main delay block, allowing for finer adjustments in delay precision. The output of the cascaded delay blocks was then processed by a two-layer NN, where the outputs of both the main and small delay elements served as inputs to the NN. This adaptive mechanism continuously corrects delay mismatches by leveraging the learning capabilities of the NN.

Delay imperfections may arise during the manufacturing process or over time due to environmental factors. To ensure optimal performance, the user is required to calibrate each block by tuning the NN weights based on the error between the filter's output and the desired response. This calibration process can be performed during initial deployment or as the filter adapts to changing conditions over time, ensuring consistent and reliable operation in high-speed signal processing applications.

In future work, we plan to validate and extend our NN-based compensation approach across a variety of technologies and application domains, ranging from advanced CMOS and mixed-signal implementations in commercial analog filter ICs and RF front-ends to purely digital delay lines in FPGAs and even optical signal-processing chains where fiber-length jitter induces random delays. Such cross-technology prototyping will reveal how the cascaded-delay plus NN paradigm scales with process, frequency, and system complexity. Concurrently, we will investigate more sophisticated neural architectures, beyond our two-layer perceptron, capable of jointly correcting multiple error sources (e.g., gain mismatches, nonlinearities, and delay drift) in real time. Although deeper or specialized networks introduce extra hardware and training overhead, they may unlock richer calibration capabilities, enabling fully self-correcting filter and signal-processing modules in increasingly demanding environments.

Declaration of Ethical Standards

The authors declare that all ethical guidelines including authorship, citation, data reporting, and publishing original research.

Credit Authorship Contribution Statement

Finding the problem and deciding the solution proposal, researching, developing software, preparing the draft of the article, writing and reviewing the article.

Declaration of Competing Interest

The author declares that he has no conflict of interest

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Data Availability

All data was not presented in the article. It would be supplied by the author upon request.

REFERENCES

- [1] J. Remple and I. Galton, "The effects of inter-symbol interference in dynamic element matching DACs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 64, no. 1, pp. 14–23, Jan. 2017.
- [2] A. Y. Hassan, "Enhancing signal detection in frequency selective channels by exploiting time diversity in inter-symbol interference signal," *Wireless Pers. Commun.*, vol. 106, pp. 1373–1395, 2019.
- [3] S. Kim and I. Galton, "Adaptive cancellation of inter-symbol interference in high-speed continuous-time DACs," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 70, no. 11, pp. 4309–4322, Nov. 2023, doi: 10.1109/TCSI.2023.3301714.
- [4] M. Hosney, H. A. I. Selmy, A. Srivastava, and K. M. F. Elsayed, "Interference mitigation using angular diversity receiver with efficient channel estimation in MIMO VLC," *IEEE Access*, vol. 8, pp. 54060–54073, 2020.
- [5] J. Liu and X. Lin, "Equalization in high-speed communication systems," *IEEE Circuits Syst. Mag.*, vol. 4, no. 2, pp. 4–17, 2004.
- [6] N. Shwetha and M. Priyatham, "Performance analysis of self-adaptive equalizers using EPLMS algorithm," in *Proc. 2020 4th Int. Conf. I-SMAC (IoT in Social, Mobile, Analytics and Cloud) (I-SMAC)*, Palladam, India, 2020, pp. 872–876.
- [7] F. T. Gebreyohannes, A. Frappé, and A. Kaiser, "Semi-digital FIR DAC for low power single carrier IEEE 802.11ad 60 GHz transmitter," in *Proc. IEEE 13th Int. New Circuits Syst. Conf. (NEWCAS)*, 2015, pp. 1–4.
- [8] M. R. Sadeghifar, H. Bengtsson, J. J. Wikner, and O. Gustafsson, "Direct digital-to-RF converter employing semi-digital FIR voltage-mode RF DAC," *Integration*, vol. 66, pp. 128–134, 2019.
- [9] M. R. Sadeghifar, O. Gustafsson, and J. J. Wikner, "Optimization problem formulation for semi-digital FIR digital-to-analog converter considering coefficients precision and analog metrics," *Analog Integr. Circ. Signal Process.*, 2018.
- [10] E. OhAnnaidh, S. Rouat, S. Verhaeren, S. L. Tual, and C. Garnier, "A 3.2 GHz sample-rate 800 MHz bandwidth highly reconfigurable analog FIR filter in 45 nm CMOS," in *Proc. IEEE ISSCC, Analog Techniques*, San Francisco, CA, USA, Feb. 2010.
- [11] V. Srinivasan, G. Rosen, and P. Hasler, "Low-power realization of FIR filters using current-mode analog design techniques," in *Proc. ACSSC*, 2004, vol. 2, pp. 2223–2227.
- [12] G. Xu and J. Yuan, "A CMOS analog FIR filter with low phase distortion," in *Proc. ESSCIRC*, 2002, pp. 747–750.

- [13] A. Petraglia and S. K. Mitra, "Effects of coefficient inaccuracy in switched-capacitor transversal filters," *IEEE Trans. Circuits Syst.*, vol. 38, no. 9, pp. 977–983, Sep. 1991.
- [14] P. Liu, Y. B. Kim, and Y. J. Lee, "An accurate timing model for nano CMOS circuit considering statistical process variation," in *Proc. IEEE Int. SoC Design Conf.*, Seoul, South Korea, Oct. 2007, pp. 269–327.
- [15] S. Patil, S. G. Rao, Y. Chen, and Y. Tsvividis, "Signal encoding and processing in continuous time using a cascade of digital delays," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 66, no. 3, pp. 1017–1030, Mar. 2019.
- [16] N. Akyuz, "Effects of random delay errors in transversal filters," M.S. thesis, Univ. Texas Dallas, Dallas, TX, USA, 2011.
- [17] M. T. Ozgun and M. Torlak, "Effects of random delay errors in continuous-time semi-digital transversal filters," *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol. 61, no. 1, pp. 183–190, 2014.
- [18] G. Cauwenberghs and G. C. Temes, "Adaptive digital correction of analog errors in MASH ADCs. I. Off-line and blind on-line calibration," *IEEE Trans. Circuits Syst. II, Analog Digit. Signal Process.*, vol. 47, no. 7, pp. 621–628, Jul. 2000, doi: 10.1109/82.850421.
- [19] A. Mandal and R. Mishra, "Digital equalization for cancellation of noise-like interferences in adaptive spatial filtering," *Circuits Syst. Signal Process.*, vol. 36, pp. 675–702, 2017.
- [20] A. G. K. C. Lim, V. Sreeram, and G.-Q. Wang, "Digital compensation in IQ modulators using adaptive FIR filters," *IEEE Trans. Veh. Technol.*, vol. 53, no. 6, pp. 1809–1817, Nov. 2004, doi: 10.1109/TVT.2004.836934.
- [21] K.-K. Shyu and C.-Y. Chang, "Modified FIR filter with phase compensation technique to feedforward active noise controller design," *IEEE Trans. Ind. Electron.*, vol. 47, no. 2, pp. 444–453, Apr. 2000, doi: 10.1109/41.836361.
- [22] G. Fan, Y. Huang, Y. Su, J. Li, and G. Sun, "A reduced bias delay lock loop for adaptive filters," *Adv. Space Res.*, vol. 59, no. 1, pp. 230–235, Jan. 2017.
- [23] S. Moon, K. Shin, and D. Jeon, "Enhancing reliability of analog neural network processors," *IEEE Trans. Very Large Scale Integr. Syst.*, vol. 27, no. 6, pp. 1455–1459, Jun. 2019, doi: 10.1109/TVLSI.2019.2893256.
- [24] R. Rafieisangari and N. Shiri, "A neural network-based error correction in the first-stage residue of pipelined analog to digital converters," *Int. J. Circuit Theory Appl.*, vol. 52, no. 12, pp. 6001–6027, Dec. 2024, doi: 10.1002/cta.4076.
- [25] N. Nambath *et al.*, "All-analog adaptive equalizer for coherent data center interconnects," *J. Lightwave Technol.*, vol. 38, no. 21, pp. 5867–5874, Nov. 2020, doi: 10.1109/JLT.2020.2987140.
- [26] P. Teymouri, M. R. Mosavi, and M. Moazedi, "Delay spoofing reduction in GPS navigation system based on Time and Transform Domain adaptive filtering," *Iranian Journal of Electrical and Electronic Engineering*, vol. 14, no. 3, pp. 222–235, Sep. 2018, doi: 10.22068/IJEEE.14.3.222.
- [27] Y. Sun, J. Wu, Y. Li, and D. J. Moss, "Comparison of microcomb-based radio-frequency photonic transversal signal processors implemented with discrete components versus integrated chips," *Micromachines*, vol. 14, no. 9, p. 1794, Sep. 2023, doi: 10.3390/mi14091794.
- [28] K. Avci and A. Nacaroğlu, "Computation of noise in switched capacitor networks due to the random fluctuation of the switching instants," in *Proc. 1st Int. Conf. Informatics (ICI)*, Çeşme, Turkey, Sep. 2004, pp. 1–4.
- [29] K. Avci and A. Nacaroğlu, "Analysis of the effect of periodic fluctuation of switching instants on the transfer characteristics of switched capacitor networks," *Int. J. Circuit Theory Appl.*, vol. 22, pp. 15–24, 1994.