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Research Article

A New Topology using HFL for Transformer-Based Multilevel Inverters

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Abstract

This paper presents a new hybrid structure for transformer based multilevel inverter (MLI) topologies. The proposed topology integrates an asymmetric multiplexer circuit (push-pull), a high frequency link (HFL) circuit and PUC to produce 11 levels at the output voltage wave. The main structure includes 10 power switches and four rectifier diodes. Simulation results and experimental results confirm that the proposed inverter effectively synthesizes the 11-level AC voltage waveform with low total harmonic distortion (THD). The inverter is tested with 100Ω pure resistive, 30mH and 50mH inductive loads under different load conditions to verify its robustness and operational stability. Loss simulations are performed with PLECS software. The power loss analysis shows that the system operates with an efficiency of 98% in overall performance. The dynamic response of the inverter is analyzed under varying modulation indices and operating frequencies and shows reliable performance over a wide operating range. Due to its high efficiency and reduced component count, the proposed topology is particularly suitable for single-source applications such as renewable energy integration, stand-alone power systems and electric vehicle inverters.

Keywords: Multilevel inverter, DC-AC Converter, High Frequency Link, Low Total Harmonic Distortion, Push-pull Converter

Transformatör Tabanlı Çok Seviyeli İnvertörler için HFL Kullanan Yeni Bir Topoloji

Öz

Bu çalışma transformatör tabanlı çok seviyeli evirici (ÇSE) topolojileri için yeni bir hibrit yapı sunar. Önerilen topoloji bir asimetrik çoklayıcı devre (push-pull), bir yüksek frekans bağlantısı (YFB) ve bir PUC devresini entegre ederek çıkış gerilim dalgasında 11 seviye üretir. Ana yapı 10 güç anahtarı ve dört doğrultucu diyot içerir. Simülasyon ve deneysel sonuçlar, önerilen eviricinin düşük toplam harmonik bozulma (THD) ile 11 seviyeli AC gerilim dalga şeklini etkin bir şekilde sentezlediğini doğrulamaktadır. Evirici, 100Ω tam dirençli, 30mH ve 50mH endüktif bileşenli yüklerle farklı yük koşulları altında test edilerek sağlamlığı ve çalışma kararlılığı doğrulanmıştır. Kayıp simülasyonları PLECS yazılımıyla gerçekleştirilir. Yapılan güç kaybı analizleri sistemin genel performansında %98'lik bir verimle çalıştığını gösterir. Eviricinin dinamik tepkisi, değişen modülasyon indeksleri ve çalışma frekansları altında analiz edilmiş ve geniş bir çalışma aralığında güvenilir performans göstermiştir. Yüksek verimliliği ve azaltılmış bileşen sayısı nedeniyle, önerilen topoloji özellikle yenilenebilir enerji entegrasyonu, bağımsız güç sistemleri ve elektrikli araç invertörleri gibi tek kaynaklı uygulamalar için uygundur.

Anahtar Kelimeler: Çok seviyeli evirici, DA-AA dönüştürücü, Düşük toplam harmonik bozulma, Push-Pull dönüştürücü, Yüksek frekans bağlantısı

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1. Introduction

Multilevel inverters (MLIs) make an important contribution to DC-AC power conversion in advanced power conversion systems. MLIs are structures that provide a sinusoidal voltage at the output as a result of switching DC sources depending on certain angles. Compared to conventional inverters, MLIs have significant advantages in terms of better power quality, high output voltages with low voltage semiconductor devices, low THD, low electromagnetic interference, dv/dt ratio and switching losses [1]. The use of MLIs in a system improves the power quality and efficiency of the system because harmonic distortion and switching losses are reduced. They are frequently used in industrial applications such as renewable energy systems, electric vehicles, power distribution networks and industrial motor drives. Multilevel inverter topologies, control methods and modulation techniques have been investigated detailed in many papers from the literature [2], [3], [4]. The most common and well-known MLI topologies which are neutral point clamped, flying capacitor and cascaded H-bridge inverter (CHB) topologies have been introduced in [5], [6] and [7], respectively.

The number of output levels of multilevel inverters is possible with isolated DC source boosting or switched capacitor boosting circuits. MLI topologies using capacitors require additional circuitry to prevent inrush currents. Isolated source boosting is a major problem for MLI. This makes MLI both complex and costly [8]. Asymmetric configuration of the DC source and switching elements used can significantly increase the capability of level generation. Although asymmetric use of source voltages is a significant advantage, it may not be easy to obtain DC sources with different amplitudes [9]. In applications such as electric vehicles, the use of a single DC source has become almost mandatory due to the difficulty of charging multiple sources. MLI topologies obtained with High Frequency Link (HFL) offer a specific solution to the number of sources and inrush currents.

CHB in [10], [11], [12], [13], FC in [14], active NPC in [15], Switched MLI in [16], Packed U-cell (PUC) in [17], [18], Bypass diode MLI topologies in [19], [20] are proposed for MLI topologies. Some of these works, a primary winding and variable number of secondary windings are used in the transformer to generate a square signal. Secondary voltages are multiplexed by adding more than one primary winding to the transformer. In addition, H-bridge circuit is used to generate square wave signal.

In this study, a push-pull circuit has been used instead of a H-bridge circuit with 4 switches unlike the above studies. In addition, 2 push-pull circuits are used instead of an odd number of primary windings. In the topology, the transformer windings are wound in a ratio of 3,3:2,2:1 and the output voltage of the transformer is leveled as 1x and 2x. In this method, each DC bus is characterized by 2 different voltages at the output of the transformer. As a result, a 7-level voltage is obtained at the output of the PUC circuit with a single DC source from a conventional 4-switch H-bridge, while an 11-level output voltage is obtained with 2 push-pull structures created with 4 switches. Low THD is achieved by using the nearest level control (NLC) and Sinusoidal Pulse Width Modulation (SPWM) methods at low switching frequency. Unlike many existing topologies in the literature, which often rely on multiple isolated DC sources or

complex switching networks, the proposed configuration simplifies the overall structure while preserving high output quality and efficiency.

2. Material and Methods

2.1. Proposed Topology

The operating principle of the proposed topology is illustrated in Figure 1. The system is composed of three main components, each serving a specific function within the overall operation.

1. **Multiplexer Circuit (MC):** Located on the input side, the MC generates asymmetrical high-frequency voltages by switching a single DC source. These voltages are applied to the primary windings of the transformer in a controlled manner to create multiple voltage levels.
2. **Multi-Input Single-Output Transformer:** This transformer plays a central role by transferring the high-frequency asymmetrical voltages from the primary side to the secondary side. The unique structure of the transformer enables efficient power transfer using multiple primary inputs and a single secondary output.
3. **PUC Inverter Circuit:** Positioned at the output stage, the PUC circuit processes the multi-winding high-frequency AC voltage from the transformer's secondary and converts it into a stepped multi-level AC output. This stage includes a rectifier that contributes to generating a smooth AC waveform suitable for grid or load connection.

This modular and hybrid configuration enhances the inverter's efficiency, scalability, and voltage level resolution, while reducing the number of required components compared to conventional topologies.

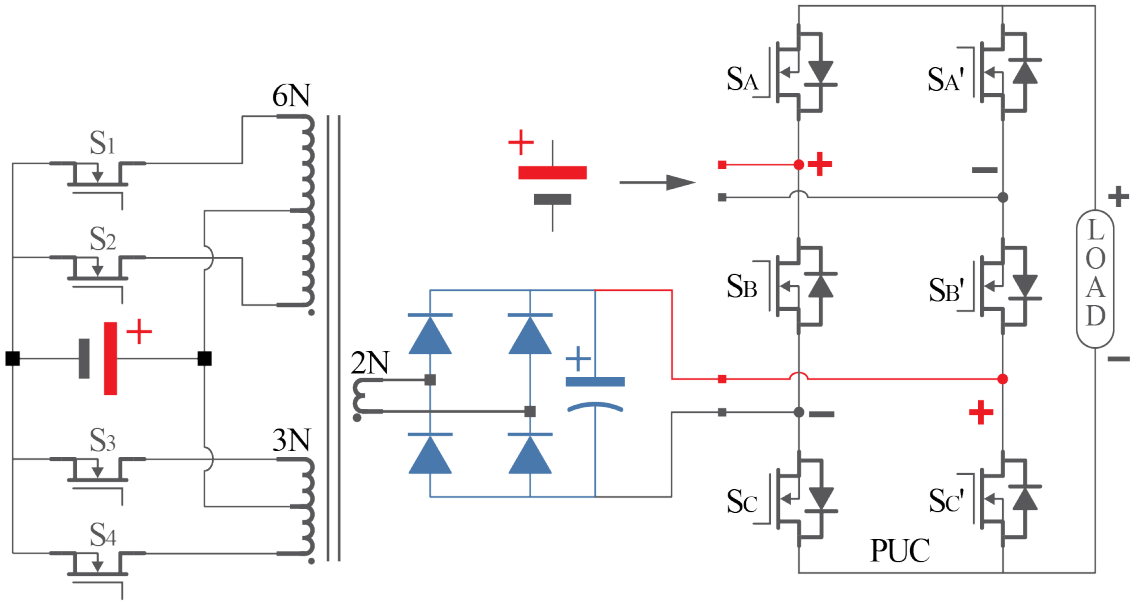


Figure 1 General structure of the proposed transformer-based multilevel inverter topology, including the asymmetric multiplexer, high-frequency transformer, and output stage.

The use of a HFL in the proposed topology provides significant advantages such as galvanic isolation, reduced transformer size, and improved power density. Moreover, operating at high

frequency enables faster dynamic response and better integration in compact power electronic systems.

The most distinguishing feature of the proposed topology is its multi-input, single-output structure, which sets it apart from conventional HFL techniques. In this configuration, the input side of the transformer asymmetrically applies voltage from the DC input source to two primary windings at high frequencies. These windings operate in an inverted manner with winding ratios of 3:1 and 3:2 with respect to the output, respectively. The switching diagram of the proposed circuit is shown in Figure 2. An important advantage of this switching scheme is that the pulses for all four switches are derived from a single Sx signal generated by the microcontroller, simplifying the control mechanism. As a result, high frequency asymmetric pulses are applied to switches S_1-S_4, leading to the generation of asymmetric winding voltages. Figure 2 also provides a table of the voltage levels in the secondary winding of the transformer as a function of the Sx state. As can be seen, when Sx = 0, the output voltage V_0 is $0.33V_{DC}$ and when Sx = 1, V_0 reaches $0.66V_{DC}$. This structured approach improves the efficiency of voltage conversion while maintaining system simplicity and control precision.

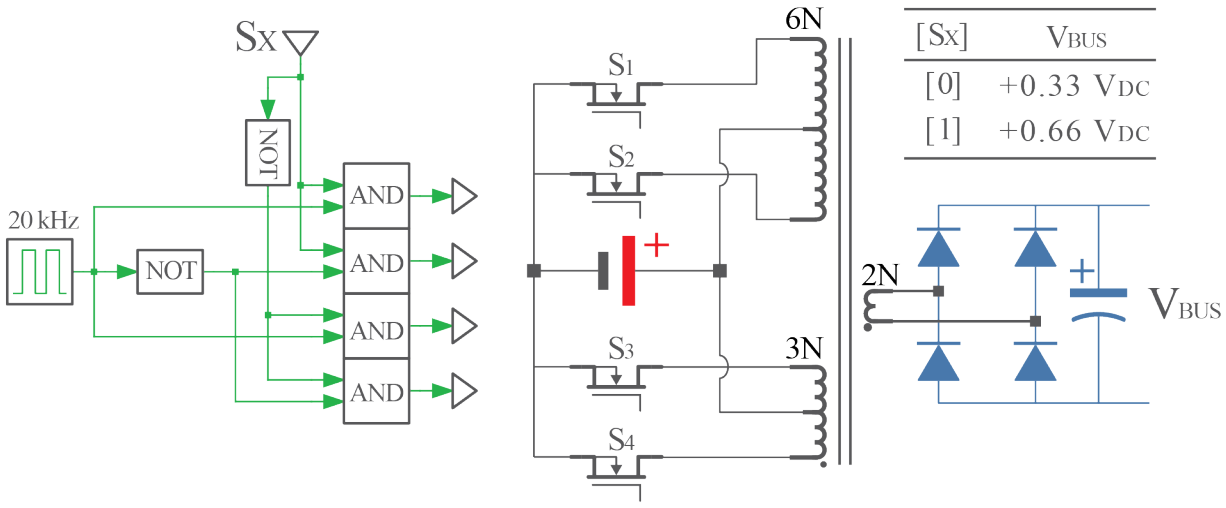


Figure 2 Operating principle of the proposed topology and generated output voltage levels.

In Figure 2, 2 Push-Pull circuits are used in the front circuit of the transformer. The single DC voltage source used in the circuit is operated separately with Push-Pull circuits and two square signals are generated at the output of the transformer, one times and two times the amplitude of the DC source used at the input. These square signals are used in the MLI circuit thanks to the bridge rectifier diode to obtain a DC bus voltage varying as 1VDC and 2VDC independent of the source ground.

When the transformer winding calculation is made, it is made according to the number of windings less than the primary windings. Primary windings have winding numbers in the ratio of 1:2. According to the core used in the transformer, the number of turns is calculated as follows for the primary winding:

$$N_{primary_{Min}} = \frac{V_{RMS}}{4 \cdot f \cdot A \cdot B_{MAX}} = \frac{120}{4 \cdot 20 \cdot 10^{3} \cdot 1.65 \cdot 10^{-4} \cdot 0.2} = 45.4 \quad (1)$$

Here, since the amplitude of the square voltage signal in the winding is 120V, the RMS value is also 120V. The toroidal transformer has a cross-sectional area of 1.65 cm2 (1.5 cm×1.1 cm) and a flux density of 0.2 Tesla and is switched at 20 kHz. The primary winding must be at least 45.4. In this case, 48 and 96 turns of the primary windings and 32 turns of the secondary winding are suitable. A new source configuration is recommended for the PUC topology implemented at the back-end of the circuit. The proposed configuration is shown in the PUC circuit presented in Figure 3. As can be seen, a constant $3V_{DC}$ bus voltage is applied to the upper layer, while the lower layer utilizes the multiple voltage levels ($1V_{DC}$ and $2V_{DC}$) generated in the secondary output winding of the input HFL. The PUC circuit converts these input voltages into a five-level AC voltage waveform. This topology is widely used due to its ability to convert the upper layer voltage Vu and lower layer voltages Va into bipolar voltages ±Vu, ±Va and ±(Vu + Va) at the output. As a result, the proposed topology generates bipolar voltage levels of $1V_{DC}$, $2V_{DC}$, $3V_{DC}$, $4V_{DC}$ and $5V_{DC}$ using bus voltages of $1V_{DC}$, $2V_{DC}$ and $3V_{DC}$, providing a multilevel AC voltage wave that is advantageous for high performance power electronics applications.

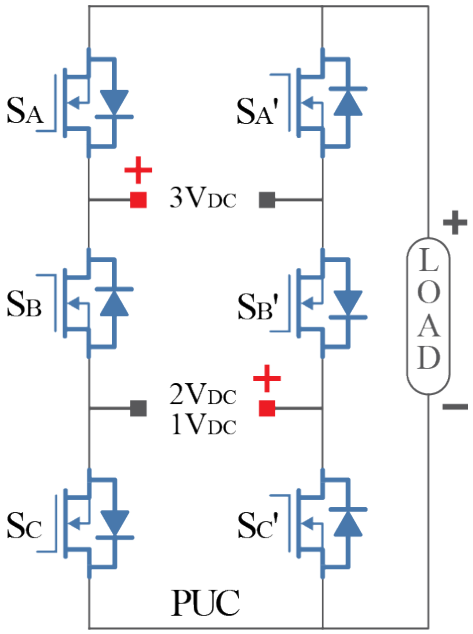


Figure 3 PUC-based power stage configuration used in the proposed topology.

Figure 4 shows the operating modes of the PUC topology based on the proposed source configuration to produce an 11-level AC waveform at the output. Each operating mode corresponds to a specific switching circuit that generates the voltage levels synthesized in the output waveform. By properly controlling the switches, a stepped output voltage is obtained, which improves power quality and reduces harmonic distortion.

This multi-level operation is particularly beneficial in medium and high power applications where improved efficiency and reduced filtering requirements are critical. Furthermore, the switch states corresponding to each switching mode are presented in Table 1, providing a detailed illustration of how the 11-level AC waveform is generated.

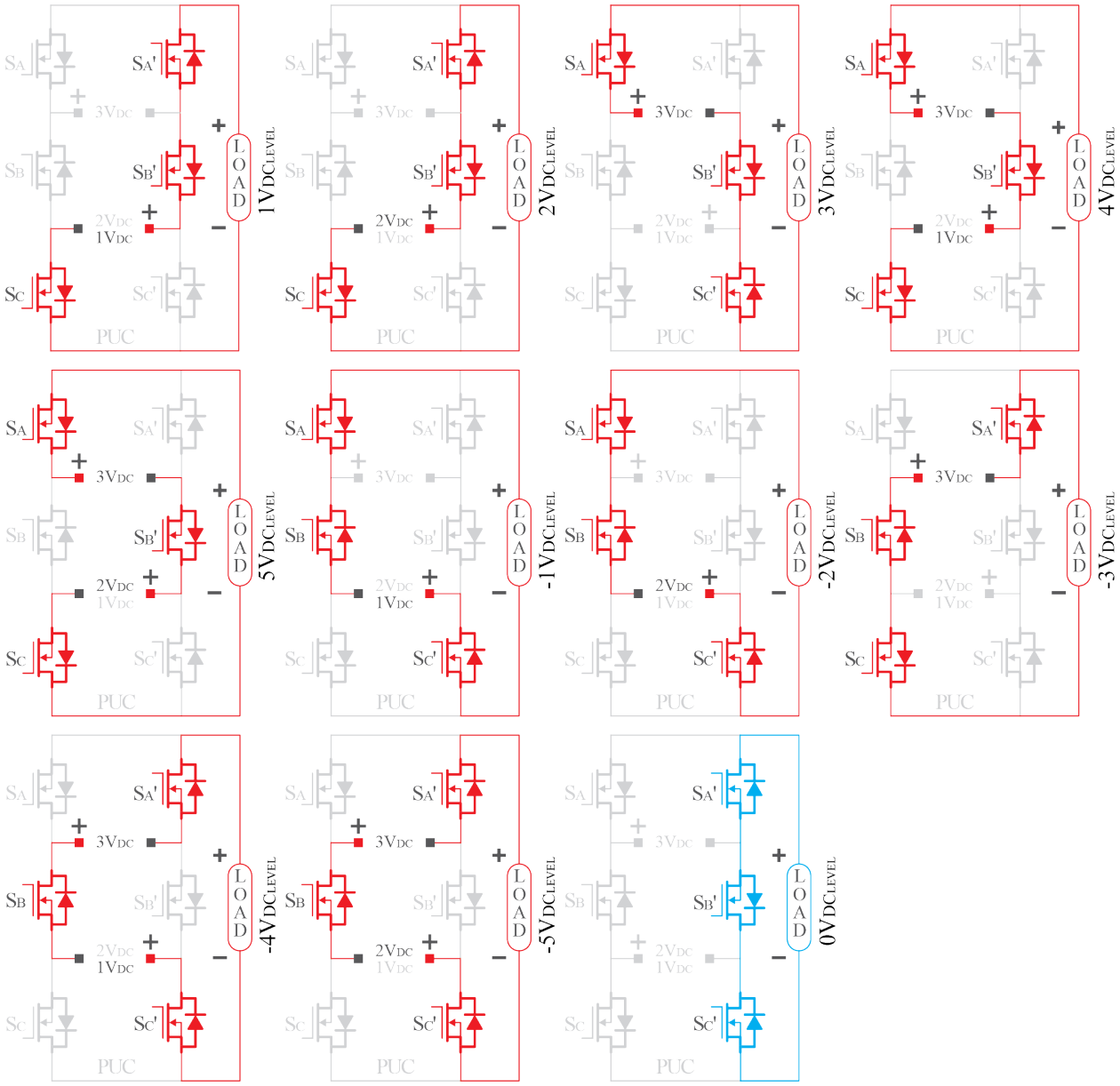


Figure 4 Operation modes of the PUC circuit within the proposed inverter topology.

Table 1 Switching States for Each Mode of Operation in the Proposed PUC Topology

S_X	S_A	S_B	S_C	V_{OUT}
1	1	0	1	+5 V_{DC}
0	1	0	1	+4 V_{DC}
0	1	0	1	+3 V_{DC}
1	0	0	1	+2 V_{DC}
0	0	0	1	+1 V_{DC}
0	0	0	0	+0 V_{DC}
0	1	1	0	-1 V_{DC}
1	1	1	0	-2 V_{DC}
0	0	1	0	-3 V_{DC}
0	0	1	0	-4 V_{DC}
1	0	1	0	-5 V_{DC}

The operation is tested with NLC and SPWM control methods and the output voltage waveform and switching pulses are shown. The output voltage waveform and the corresponding switching pulses according to the NLC control technique are shown in Figure 5. An important difference that distinguishes this topology from many existing works in the literature is that the switching pulses in the DC are generated from the high frequency modulation of the control signal, as observed in the figure. In particular, the relationship between the Sx signal and the switching pulses (S_1, S_2, S_3, S_4) of the switches in the WD is remarkable. The switch pulses S_1 and S_2 are 5kHz high frequency modulated signals derived from the signal Sx. When Sx = 1, switches S_1 and S_2 are reverse-triggered at high frequency, while S_3 and S_4 remain OFF. Conversely, when Sx = 0, S_3 and S_4 switches are reverse-triggered at high frequency, while S_1 and S_2 remain OFF. Similarly, the output voltage waveform and switch pulses obtained with the SPWM control method are shown in Figure 6. In the SPWM control method, the carrier signal frequency is set to 2.5kHz. It should be noted that since the modulation frequency in S1-S4 signals is 5 kHz, they are triggered more tightly than the output voltage.

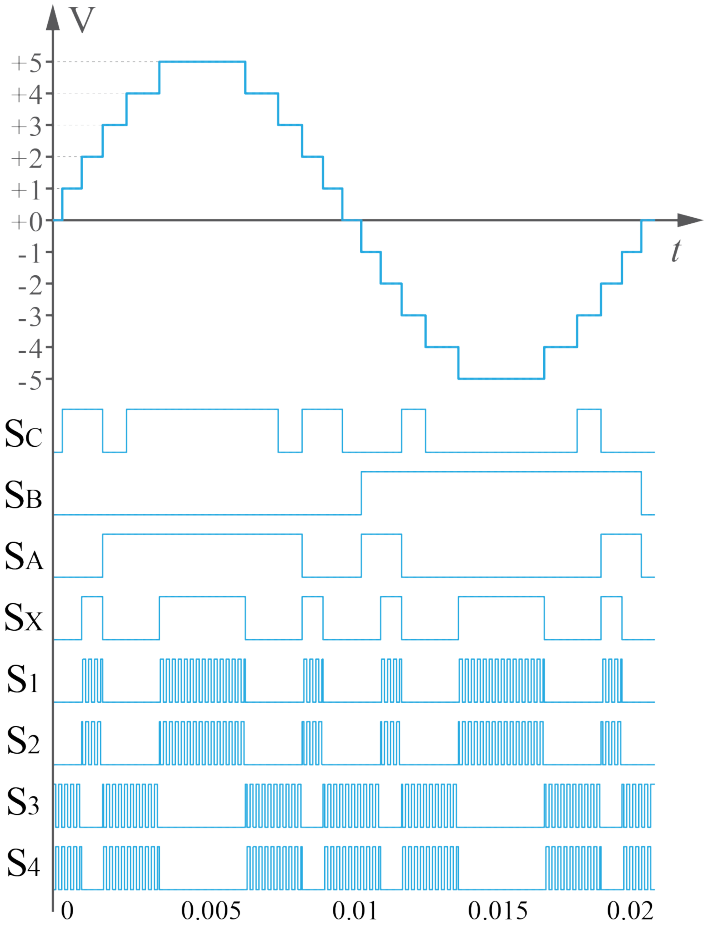


Figure 5 Output voltage waveform and switching pulses with NLC control technique.

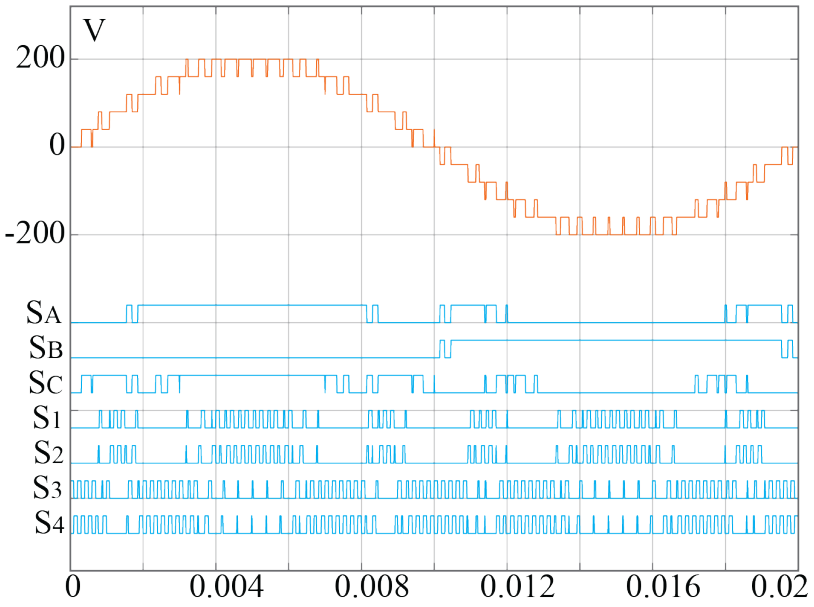


Figure 6 Output voltage waveform and switching pulses with SPWM control technique.

Total standing voltage (TSV) is an important performance metric in MLI topologies. It gives important clues for the expansion of the topology for the switches and high voltage applications used in the topology. Distribution of blocking voltages on the power switches is shown in Figure 7. TSV is defined as the summation of the highest blocking voltages that each switch is exposed to at all levels. To calculate the TSV in the topology, the highest voltages at all levels of the switches used in the circuits on the primary and secondary of the transformer are summed. The 4 switches on the primary of the transformer are expressed in terms of input DC voltage source as follows:

$$TSV_1 = \sum_{j=1}^{4} (V_{S_j}) \tag{2}$$

$$TSV_1 = 2 \times 2V_{DC} + 2 \times 3V_{DC} = 10V_{DC} \tag{3}$$

Switches S_A and S_A' in the PUC circuit on the secondary of the transformer are exposed to 1VDC, switches SC and SC' are exposed to $0.67V_{DC}$, and switches S_B and S_B' in the middle are exposed to $0.67V_{DC}$.

$$TSV_2 = \sum_{j=1}^{6} (V_{S_{PUC}}) \tag{4}$$

$$TSV_2 = 2 \times 1V_{DC} + 2 \times 0.67V_{DC} + 2 \times 1.67V_{DC} \approx 6.67V \tag{5}$$

The general TSV of the circuit is obtained by summing the two TSVs calculated above

$$TSV = TSV_1 + TSV_2 = 16.67V \tag{6}$$

Table 1 shows the N_{LEVEL}, N_{SW}, N_{DR}, N_{DD}, N_{CAP}, N_{CAP}, N_{TR} and TSV values of other studies in the literature. The total TSV value was calculated by taking into account the H-bridge circuits on the primary of the transformer.

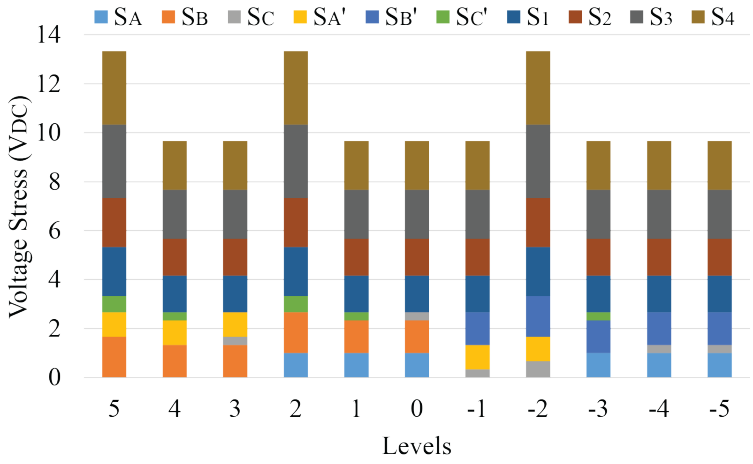


Figure 7 Distribution of blocking voltages on power switches.

2.2. Comparative Study

A comprehensive review of the literature is carried out to evaluate the performance of proposed topology and compare it with the works in the literature. The comparison includes various performance metrics such as cost function (CF), number of switches used in the topology, number of isolated DC sources and overall system efficiency. One of the critical parameters in the evaluation is the cost function (CF), which is widely used to evaluate the efficiency and complexity of MLI topologies by considering the number of semiconductor switches, gate drivers and DC sources required for the application. The main parameters used by many researchers to indicate the advantage of their proposed topology are the number of power elements used, the number of DC sources, the TBV and the number of levels produced by the topology. Although the cost functions assigned to these parameters are formulated slightly differently, they are mostly similar to each other.

In the proposed topology, the CF according to the specified parameters is determined as in (7).

$$CF = \frac{(N_{SW} + N_{GD} + N_D + N_C + \alpha TSV) \cdot N_{DC}}{N_L} \tag{7}$$

The weighting factor α is usually taken as (α=0.5) and (α=1.5). If the weighting coefficient α is given a value greater than 1 (e.g. α=1.5), the TSV is considered to be more important than the number of power components, whereas if α is given a value less than 1 (e.g. α=0.5), it is considered to be less important. The cost factor is then calculated according to the value given to the weighting coefficient. In this study, the CF for 15 levels takes the value 2.94 when the cost function α=0.5 and 4.46 when α=1.5. Table 2 shows the performance comparison between the proposed topology and other studies in the literature on the cost function with weighting factors depending on the voltage levels.

Table 2 Comparative Analysis of the Proposed MLI with Similar Studies.

Topology	Year	N_L	N_{DC}	N_{SW}	N_{GD}	N_D	N_C	TSV	C_F (α)	
									0.5	1.5
[22]	2024	7	1	7	7	2	2	15	3.64	5.79
[23]	2024	7	1	10	10	1	2	17	4.50	6.93
[24]	2024	7	1	8	8	-	4	16	4.00	6.29
[21]	2023	9	1	10	9	2	3	44	5.11	10.00
[25]	2022	9	1	12	11	-	3	44	5.33	10.22
[26]	2022	13	1	12	11	3	3	36	3.62	6.38
[27]	2021	13	2	14	14	2	4	34	7.85	13.08
Prop.	**2025**	**11**	**1**	**10**	**10**	**4**	**-**	**16.67**	**2.94**	**4.46**

It should be noted in Table 3 that there is an inverse relationship between the voltage level and the CF, i.e. as the number of voltages increases, the CF decreases. The CF value of the proposed 11-level topology is relatively low compared to other studies in the literature. The extensive literature comparison highlights the advantages of the proposed topology, especially in terms of reduced switch count, lower CF, improved efficiency and improved voltage level generation. The results show that the proposed design offers a cost-effective and high-performance solution for multilevel inverter applications and is a promising candidate for renewable energy systems, electric drives and other power conversion applications.

2.3. Power Losses and Efficiency Analysis

The determination of power loss is a critical parameter in the performance evaluation of MLI. Transmission losses (P_{cond}), switching losses (P_{SW}) and transformer losses (P_{tr}) are the parameters that affect the total power loss.

$$P_{\text{losses}} = P_{cond} + P_{\text{sw}} + P_{tr} \tag{8}$$

In MLI circuits, conduction losses occur due to the on-state resistance (Rs) of the conducting power switches on the current path, the internal resistance (Rd) of the diodes, the forward voltage drop (Vd) of the diode and the internal resistance (Rc) of the capacitor. MLIs exhibit a large number of power elements and a dynamic operating performance. The variation in load current in each operating mode further complicates conduction and switching losses in power circuits. Therefore, loss and power simulations in power electronic circuits can be easily performed with computer software using thermal models of the elements. The PLECS program is one of the important software that has achieved outstanding success in this field and has been applied in many scientific studies and has proven its successful performance with its results. In this study, the thermal power losses of the proposed MLI are modeled in PLECS software and loss analysis is performed. As a result of the loss analysis, the distribution of the total power loss among the circuit elements is shown in Figure 8. In addition, the MLI was tested for 0.1-1kW output power and the inverter performance according to the output power is shown in Figure 9. As can be seen, the maximum performance of the inverter is around 150 W with 96.54%. As expected, the inverter performance decreases slightly when the output power

increases. At very low voltages, the transformer magnetic losses have a significant effect and the efficiency decreases in a similar manner as the load increases.

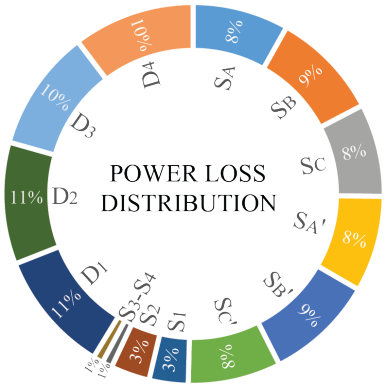


Figure 8 Power loss distribution between power components.

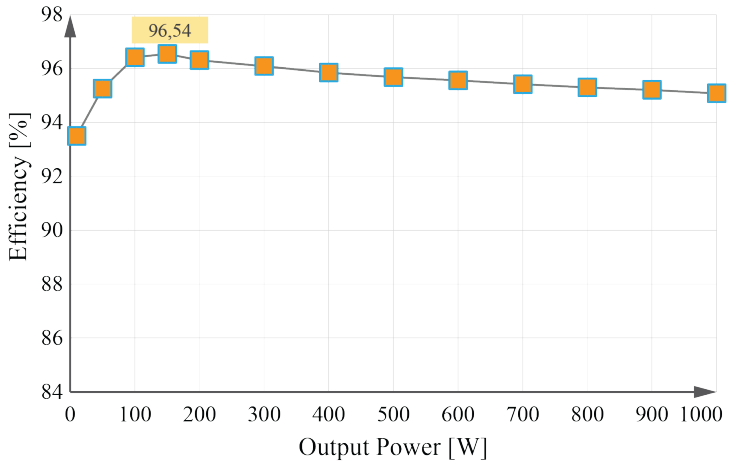


Figure 9 Variation of MLI efficiency according to different output powers.

3. Results and Discussion

3.1. Simulation Studies and Results

Electrical simulations of the proposed 11-level MLI are performed in MATLAB/Simulink to evaluate the performance of this topology. The study is run with both different modulation control techniques and the significant findings are presented in this section. Figure 10 shows the output voltage and current wave signals generated by the MLI under 100Ω+30mH load condition with SPWM control technique. In the model circuit, the amplitude of the input DC voltage source is selected as 120V. Thus, the DC voltage of 120V is applied to the transformer windings with high frequency asymmetric switching technique. In the secondary winding of the transformer, the high frequency AC voltage with 40V and 80V amplitude is transformed into $40V_{DC}$ and $80V_{DC}$ voltages with the help of a rectifier and the PUC circuit generates the AC voltage wave with a peak amplitude of 200V by using the 120VDC input voltage and $40V_{DC}$ and $80V_{DC}$ rectifier voltages.

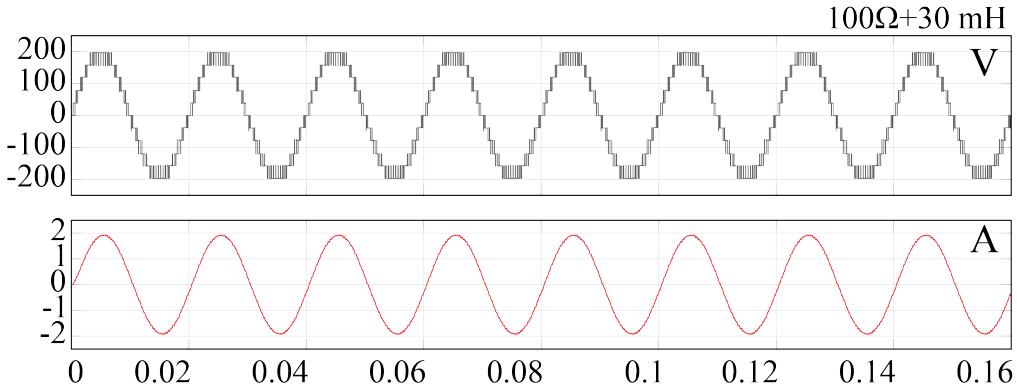


Figure 10 Proposed MLI output voltage and current waveforms.

Figure 11 shows the operating performance of the MLI under different load conditions. The circuit was first operated with 100Ω+50mH and then the output load is changed to 200Ω, 100Ω+30mH and 200Ω+50mH respectively. As can be seen, the inverter responded stably to the changes in the load and no distortion was observed in the output voltage and current signals. This confirms the usability of the proposed inverter in dynamic load variations.

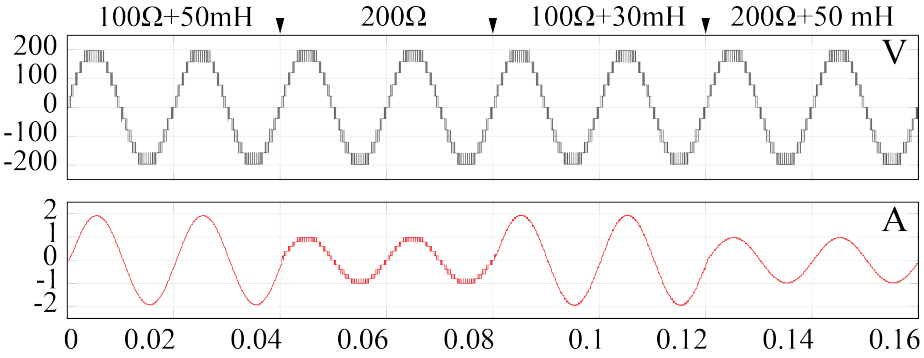


Figure 11. Output voltage of the proposed topology at different frequencies.

One of the critical measures of inverter performance is the response to different frequency and modulation index (MI) variations. In the majority of industrial applications, the system operating frequency can vary. In addition, switching signal error or open circuit (OC) error in power switches can affect the modulation of the output wave. In order to maintain the overall stability of the system, power electronics circuits must be flexible to these dynamic variations. Therefore, the inverter was tested at different frequency and MI variations. Figure 12 shows the response of the inverter to different frequency variations while Figure 13 shows the effect of the change in modulation index on the output waves with the same frequency variations. As can be seen, the inverter operated stably in both cases and no abnormalities were observed in the output signals.

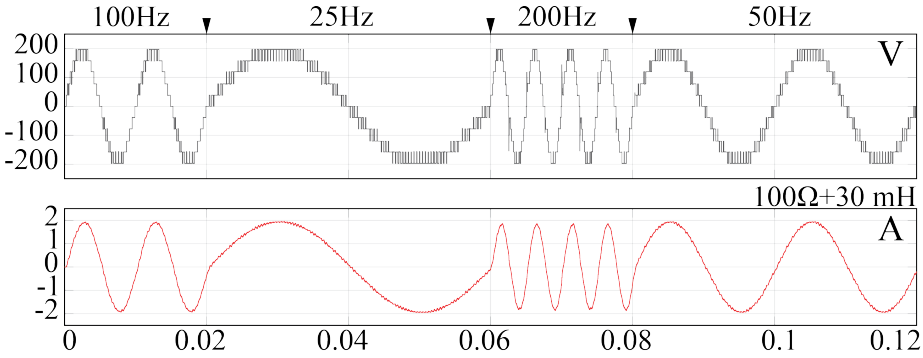


Figure 12 Response of the proposed MLI to different frequency variations.

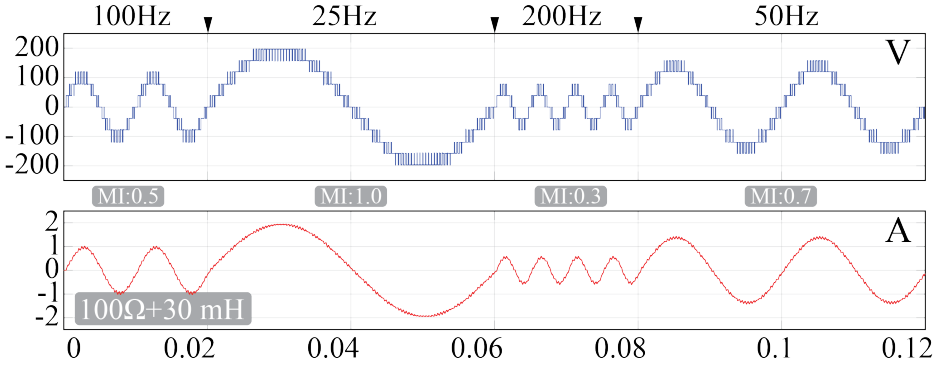


Figure 13 Response of the proposed MLI to different frequency and MI variations.

THD of the inverter output currents at the last different loads is shown in Figure 14. As can be seen, despite the low inductive load component, the inverter achieves the standard with a very low harmonic distortion in the output current. This is due to the high number of levels at the output level.

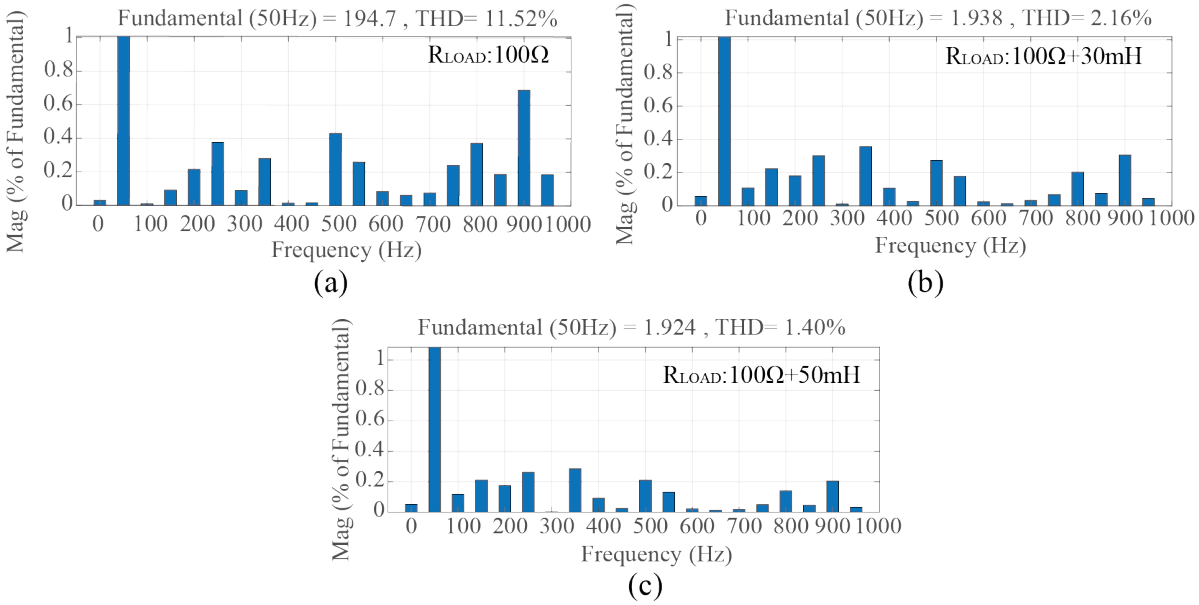


Figure 14 THB analysis of different output currents of the proposed MLI

3.2. Experimental Studies and Results

In order to validate the performance of the proposed topology through experimental studies, various load conditions were applied at the output, including purely resistive loads of 100 Ω and 200 Ω, and inductive loads of 30 mH and 50 mH. The MC circuit and PUC circuit were all implemented as laboratory-scale prototypes. The experimental setup comprises multiple key components: a 120 V DC input power supply, gate driver supply sources, an FPGA-based controller for PWM signal generation, resistive and inductive loads, an LC output filter, and current measurement equipment. A Tektronix oscilloscope and a current probe were used to monitor the output voltage and current waveforms, with the probe scale adjusted to 10 A/V. A visual representation of the test setup is provided in Figure 15, illustrating the arrangement of the hardware components used in the experimental verification.

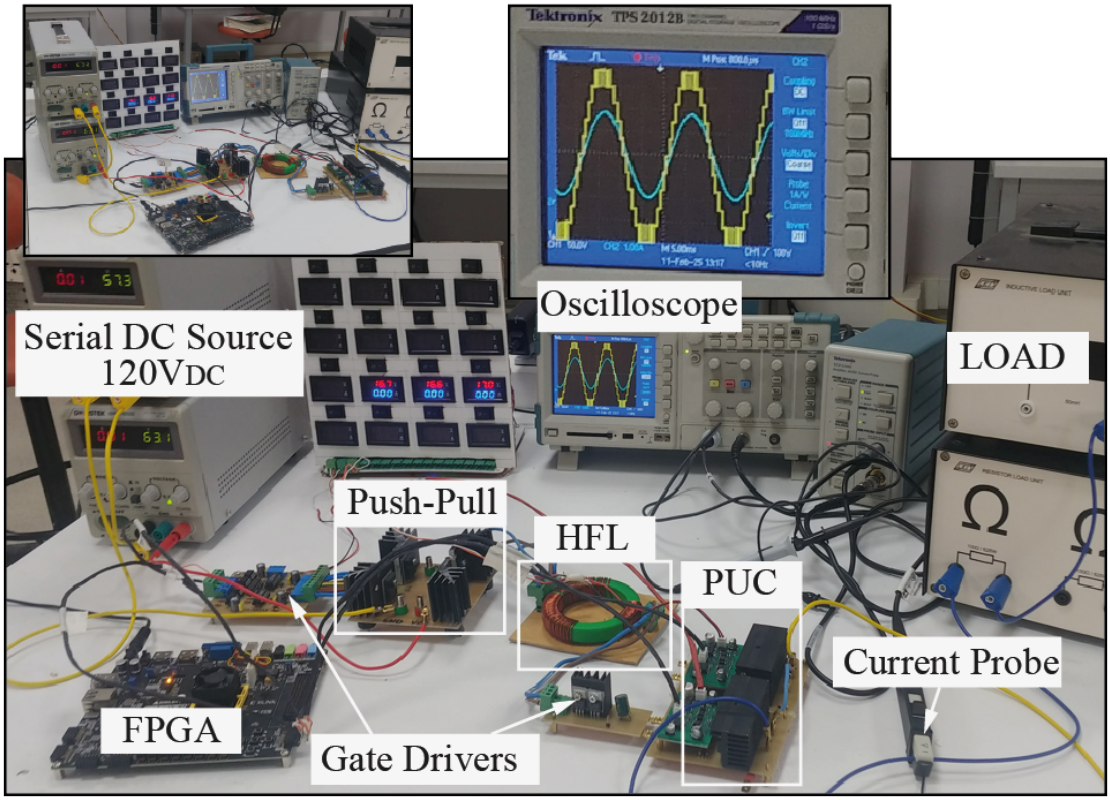


Figure 15 Image of the experimental setup.

MC and HFL convert the input single 120V single DC source voltage into high frequency voltages of 40V and 80V. At the output of the transformer, the high frequency winding voltages are converted to 40V and 80V DC voltages with the help of a rectifier. Figure 16 shows the voltages at the output of the HFL and rectifier. Figure 16 also shows the voltage drops due to forward diode cuts.

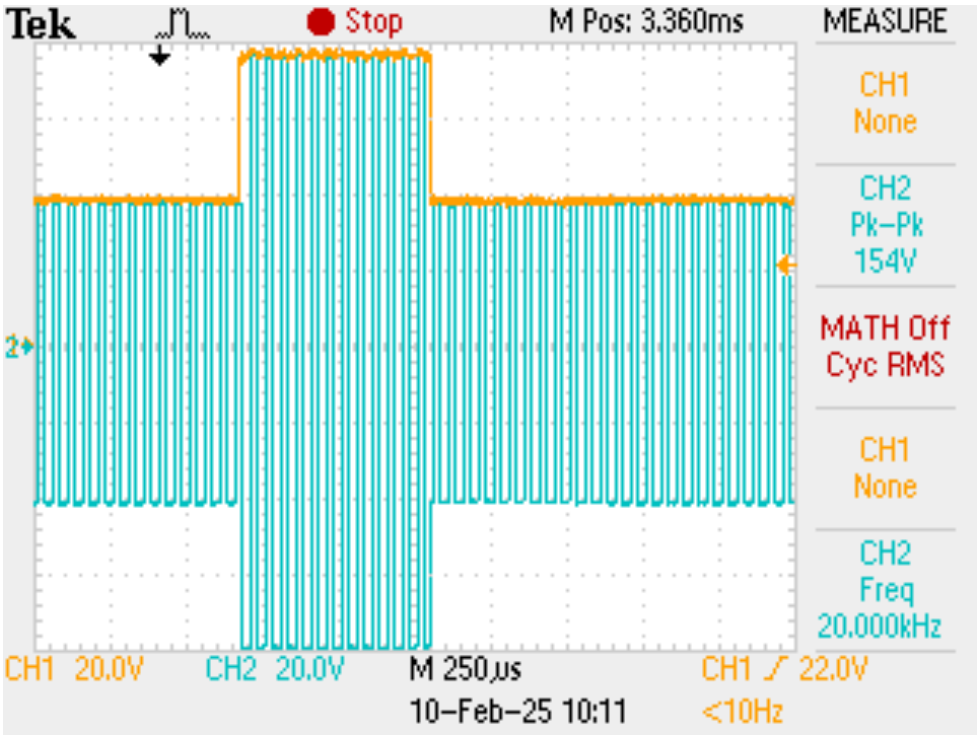


Figure 16 Rectified and non-rectified transformer output voltages.

Figure 17 presents oscilloscope waveforms of the output voltage and current under three different load conditions to demonstrate the performance of the proposed topology. In Figure 17(a), the inverter operates with a 100 Ω purely resistive load. Under this condition, the output current waveform closely follows the stepped nature of the voltage, as there is no phase shift introduced by reactive elements. In Figure 17(b), a 50 mH inductive component is added in series with the resistive load. As a result, the current waveform becomes smoother and more sinusoidal due to the filtering effect of the inductance, which attenuates high-frequency components. This demonstrates that even a modest inductive element significantly improves the current quality, reducing high-frequency leakage and harmonics. To further assess the inverter's performance under varying load scenarios, a third case is shown in Figure 17(c), where a 200 Ω resistive load is applied. Despite the increased resistance, the inverter continues to generate an 11-level output voltage waveform with stable current behavior, indicating its ability to maintain output quality under light-load conditions. These observations confirm that the proposed topology exhibits robust and consistent performance across a variety of load conditions, including resistive, inductive, and low-power operating scenarios.

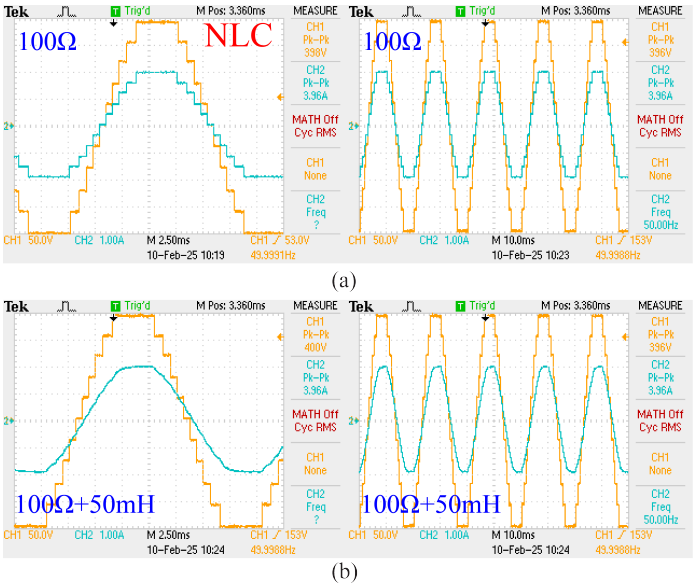


Figure 17 Output current and voltage waveforms of the inverter for NLC method a) 100Ω, b) 100Ω +50mH load conditions.

Figure 18 shows the output voltage and current waveforms obtained using the SPWM technique for the same loads. Compared to Figure 17, it is seen that the SPWM technique provides a smoother structure in the current waveform. This contributes to the reduction of harmonic content and total harmonic distortion, especially for loads with inductive components. As a result, the use of the SPWM technique improves the power quality of the system, resulting in a more stable output waveform. However, the proposed topology provides high output level and high output quality at the fundamental switching frequency without the need for high frequency SPWM control techniques.

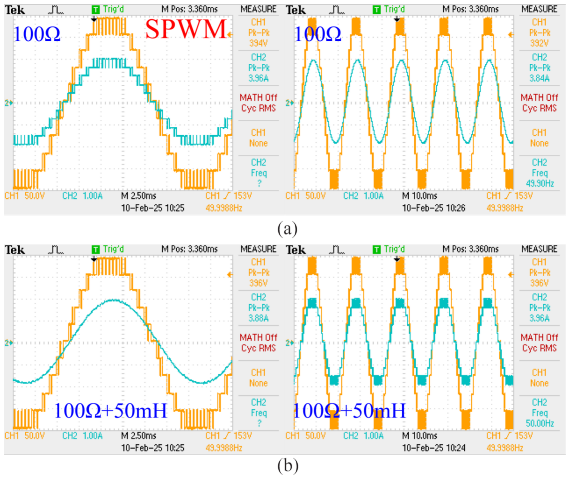
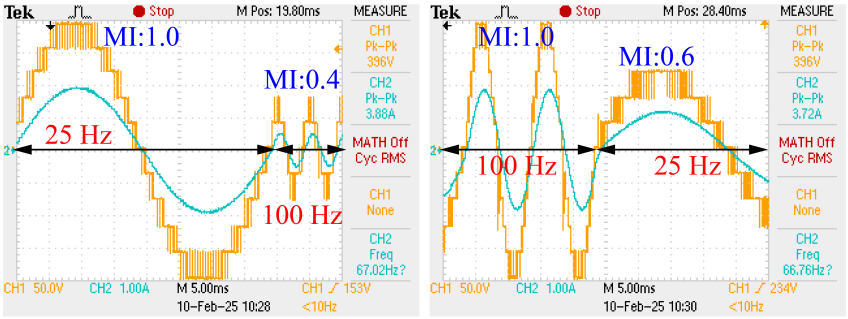


Figure 18 Output current and voltage waveforms of the inverter for SPWM method under a) 100Ω, b) 100Ω +50mH load conditions.

In the literature, various control methods have been proposed to ensure stable operation of multilevel power converters at different voltage levels. Changing the AC output voltage amplitude by adjusting MI and frequency is a widely used technique, especially in variable

frequency systems. Figure 19 shows that the proposed topology can provide variable voltage amplitudes at different frequency variations. The absence of any distortion in the output AC signals proves that the proposed inverter provides flexibility to meet the needs of dynamic systems.



(a) (b)

Figure 19 Output voltage and current waveforms of the inverter at different MI variations

4. Conclusion

In this paper, a low component count multilevel inverter (MLI) topology with high power quality has been introduced. Thanks to its hybrid structure, the proposed topology generates asymmetric multiple voltage levels using a single DC input source. To verify its robustness and performance, the inverter was tested under various load conditions, including a 100 Ω purely resistive load and a combined 50 mH inductive component. Both simulation and experimental results confirm that the topology successfully synthesizes an 11-level AC output waveform with a total harmonic distortion (THD) of less than 2.3%, ensuring high power quality. The switching and transmission losses were precisely simulated using PLECS, and the system achieved an overall efficiency of 98%. Furthermore, the inverter maintained stable operation under varying modulation indices (MI) and switching frequencies, demonstrating strong dynamic response and flexibility across a wide operating range. With its high efficiency, low THD, and reduced number of components, the proposed inverter structure is especially suitable for single-source renewable energy systems, stand-alone power applications with energy storage, and electric vehicle drive systems. These findings provide a solid contribution to the development of advanced MLI systems and offer a promising alternative to conventional topologies in industrial applications. In future work, hardware implementation of the proposed topology and the development of advanced modulation and control strategies will be considered to further validate and enhance system performance.

Ethics in Publishing

There are no ethical issues regarding the publication of this study.

Author Contributions

Hasan Hataş: Conceptualization of the study, topology design, implementation of simulations, analysis of results, and drafting of the manuscript.

Murat Karakılıç: Verification of simulation results, literature review, conduction of loss analysis using PLECS software, and final editing and proofreading of the manuscript.

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