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Research Article / Araştırma Makalesi

A Comparative Study of DQ and CSD Methods for Voltage Regulation in DSTATCOM-Based SEIG Systems

DSTATCOM Tabanlı KUAG Sistemlerinde Gerilim Regülasyonu için DQ ve CSD Yöntemlerinin Karşılaştırmalı Çalışması

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Abstract

Self-Excited Induction Generator (SEIG) plays an important role in independent power generation systems. Since SEIGs have difficulty maintaining the terminal voltage when load conditions change, an adequate compensation and control system is required. Distribution Static Compensators (DSTATCOMs) stand out with their fast dynamic response, reactive power support, and harmonic reduction capabilities. The performance of DSTATCOMs depends on the effectiveness of the control method. In this study, the performance of the widely used dq method and Current Synchronous Detection (CSD) method is compared under nonlinear loads, unbalanced loads, and DC offset conditions. The CSD method stands out with its effectiveness in filtering PCC voltages, peak estimation, and simple structure. The dq method, thanks to its high accuracy and stability in phase synchronization, has provided successful performance in harmonic suppression, current and voltage balancing, and reduction of DC offset effects. In both methods, the total harmonic distortion (THD) of SEIG current and voltage is below 5% in accordance with IEEE-519 standards.

Keywords: *Self-Excited Induction Generator (SEIG), Distribution Static Compensators (DSTATCOM), Wind energy*

Öz

Kendinden Uyarımlı Asenkron Generatör (KUAG), bağımsız güç üretim sistemlerinde, önemli bir rol oynamaktadır. SEIG'ler yük koşulları değiştiğinde terminal gerilimini korumakta zorluk çektiği için etkili bir kompanzasyon ve kontrol sistemine ihtiyaç duyulmaktadır. Dağıtım Statik Kompanzatörleri (DSTATCOM) hızlı dinamik tepkileri, reaktif güç desteği ve harmonik azaltma yetenekleri ile ön plana çıkmaktadır. DSTATCOM'ların performansı kontrol yönteminin etkinliğine bağlıdır. Bu çalışmada, yaygın olarak kullanılan dq yöntemi ile Akım Senkron Algılama (CSD) yönteminin performansı doğrusal olmayan yükler, dengesiz yükler ve DC ofset koşulları altında karşılaştırılmıştır. CSD yöntemi, PCC gerilimlerini filtrelemedeki etkinliği, tepe değerini tahmin etmesi ve basit algoritması ile öne çıkmaktadır. Ayrıca akım ve gerilimlerde meydana gelen DC ofset durumlarında faz gerilimi kestirimi daha üstündür. dq yönteminde ise faz senkronizasyonundaki yüksek doğruluk ve kararlılığı sayesinde harmonik bastırma, akım ve gerilim dengeleme ve DC ofset etkilerini azaltmada başarılı performans sağlamıştır. Her iki yöntemde de IEEE-519 standartlarına uygun şekilde SEIG akım ve geriliminin toplam harmonik distorsiyonu (THD) %5'in altındadır.

Anahtar Kelimeler: *Kendinden Uyartımlı Asenkson Generatör (KUAG), Dağıtım Statik Kompansatörleri (DSTATCOM), Rüzgâr enerjisi*

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1. Introduction

Wind energy systems are one of the fastest growing and widespread systems among renewable energy sources. Wind energy is gaining more and more importance day by day due to its environmentally friendly structure, reducing carbon emissions caused by fossil fuels, and contributing to sustainable energy production[1]. In wind turbines, asynchronous (induction) generators, synchronous generators, and permanent magnet generators are generally preferred according to system performance, efficiency, and cost issues. Induction generators preferred in off-grid systems are called self-excited induction generators (SEIG) [2].

SEIGs are characterized by a robust squirrel cage rotor structure, low maintenance costs, the absence of slip rings and brushes, self-protection against faults, and good dynamic response[3]. However, one of the most significant disadvantages of SEIGs is that their terminal voltages fluctuate if the required reactive power is not provided as the load [4]. Moreover, when the load is high, the terminal voltage can drop significantly, causing the SEIG to become unstable and its voltage to collapse[5]. The reactive power required for the SEIG to generate voltage at the starting moment is provided by capacitor banks connected to the terminals. An efficient voltage regulation system is required to ensure that the SEIG voltage is stable and regular. Power electronic converter-based systems, especially Static Var Compensator (SVC) and Distribution Static Compensator (DSTATCOM) systems, are widely used for this purpose. Although researchers have widely proposed SVC-based methods based on controlled switching of capacitor banks, SVCs do not adapt to dynamic load changes due to their long response times, which reduces their performance under load conditions with load imbalance and harmonic currents[6]. Because the reactive power provided by SVCs depends on the terminal voltage, and the capacity to provide reactive power decreases during sudden voltage drops[7]. This negatively affects system stability, and even SEIG may become unable to produce voltage. Due to these limitations, DSTATCOM stands out as the advanced dynamic performance under changing load conditions.

DSTATCOM emerges as an important alternative in SEIG-based systems, as it provides stable system operation with fast and dynamic reactive power support. It effectively regulates voltage, especially under load imbalances and load conditions containing harmonics, and increases system reliability by responding quickly to sudden voltage drops [8], [9].

The effectiveness of DSTATCOM's performance depends on the control method used. In this context, the Synchronous Reference Frame (SRF or dq) method [10] and the Current Synchronous Detection (CSD) method are prominent control strategies. Researchers have modified the CSD method to filter the phase voltages with the SOGI method [6].

The dq method transforms sinusoidal current and voltage expressions into d-q axes to provide the required active and reactive powers. Due to its precise phase synchronization capabilities, this method provides high accuracy and stability in voltage regulation, harmonic suppression, and load balancing [11]. On the other hand, the CSD method offers a more straightforward and faster control structure by using direct current signals without requiring additional transformations such as dq. This approach provides an advantage in providing a fast response to sudden load changes. In addition, filtering the PCC voltages through the SOGI allows for a more precise determination of the PCC peak voltages.

In this study, the performance of the dq method and the SOGI-based CSD method developed for voltage control in DSTATCOM-based SEIG systems are compared under nonlinear loads, unbalanced loads, and DC offset conditions. Since the phase voltages are filtered separately in the SOGI-CSD method, it showed superior performance in estimating the peak values of PCC voltages under nonlinear load and unbalanced load conditions. Accordingly, SEIG currents and voltages are produced properly despite the unbalanced and harmonic load conditions.

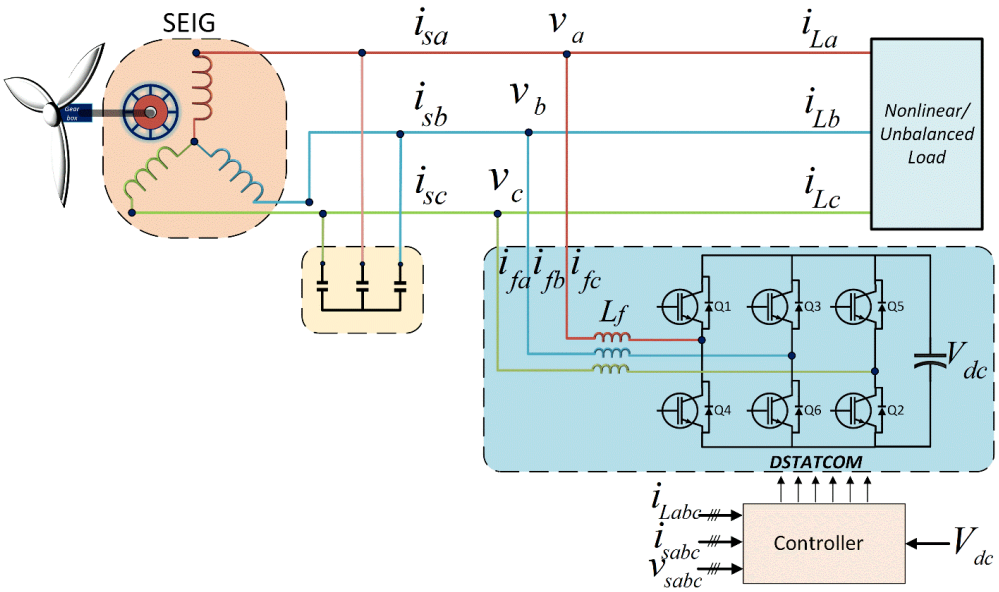

Figure 1. Schematic of DSTATCOM-based SEIG system.

Since the control scheme has no DC offset immunity, the performance of the SOGI-CSD control method is limited in estimating the peak values of PCC. Therefore, the effects of DC offset are reflected in the SEIG currents and voltages and cause limited unbalance. In addition, oscillations occurred in the DC bus voltage. However, these oscillations do not prevent DSTATCOM from providing the desired reactive power.

On the other hand, the dq method effectively meets the reactive power demands. It provides fast responses to dynamic load changes and harmonic distortions thanks to its sensitive phase synchronization. Therefore, even under changing load conditions, SEIG currents and voltages are produced in a balanced and smooth manner. Similarly, in the dq method, oscillations occur in the estimation of the PCC peak value in DC offsets occurring in current and voltage. It is observed that these oscillations were more significant than in the CSD method.

On the other hand, it is observed that SEIG currents and voltages are produced in a balanced and smooth manner with less effect from DC offset in the dq method. It is also determined that the oscillation in the DC bus voltage is lower, unlike the CSD method. When the THD ratios of currents and voltages are examined, although the values are close to each other, the dq method gives better results. However, both methods provide satisfactory performance by keeping the current and voltage THD values below the IEEE-519-2014 standard limits.

2. DSTATCOM-Based SEIG System

Fig. 1 shows the structure of the SEIG-STATCOM system. SEIGs are usually driven by rotating machines such as wind turbines to generate electricity. For the SEIG to initially generate voltage, fixed capacitor banks connected in parallel to the terminals are required. These capacitors are selected to generate the nominal voltage at no load and help the SEIG generate its magnetic field.

DSTATCOM is a power electronic device designed to regulate the SEIG's voltage and improve system stability. As shown in the figures, it mainly consists of IGBT modules and a DC capacitor. STATCOM is connected to the PCC (Point of Common Coupling) via coupling inductors and works integrated with the system.

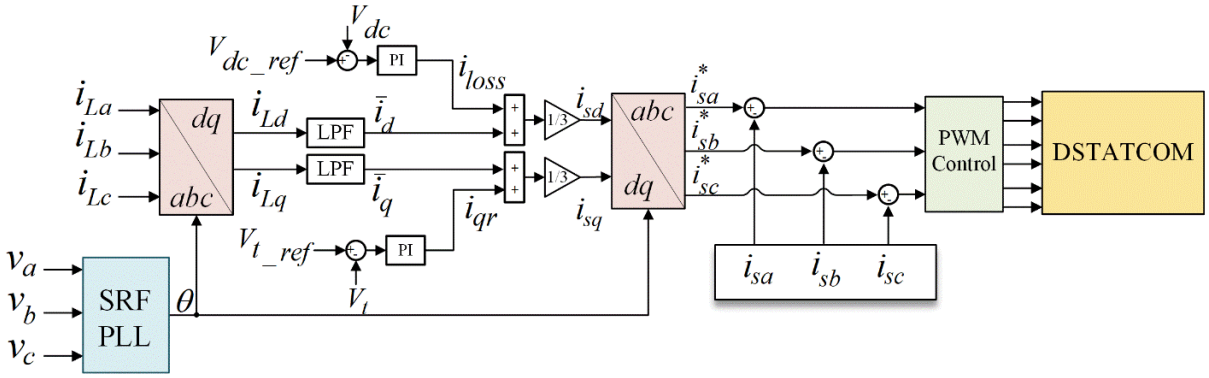

Figure 2. Representation of the dq method

3. DSTATCOM Control Methods

3.1. dq Based Method

The dq method, which is used to meet critical needs such as harmonic suppression, active and reactive power control in three-phase power systems, stands out especially with its ability to respond quickly and stably to dynamic load changes. The block diagram of the dq method is shown in Fig. 2.
In the dq method, load currents (i_{labc}), SEIG terminal voltages (v_{abc}), and DC bus voltage (V_{dc}) must be measured. These measured signals are used in the system as feedback signals. The *abc-dq* conversion process is applied to convert the load current components from the synchronous reference frame to the dq reference frame.

$$\begin{bmatrix} i_{Ld} \\ i_{Lq} \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos\omega t & \cos(\omega t-120) & \cos(\omega t+120) \\ \sin\omega t & \sin(\omega t-120) & \sin(\omega t+120) \end{bmatrix}\begin{bmatrix} i_{La} \\ i_{Lb} \\ i_{Lc} \end{bmatrix} \quad (1)$$

i_{Ld}, i_{Lq} has both fundamental and harmonic components. LPF is used to purify these currents from harmonics. The fundamental components of the LPF output are expressed as $\bar{i}_d$, $\bar{i}_q$ follows.
The Phase Locking Loop (PLL) provides the phase angle (θ) information required for the conversion from abc to dq plane and vice versa. Furthermore, the dq-based method consists of two PI controllers. One of these PI controllers is used to keep the DC bus voltage constant and stable, and the other one is used to keep the terminal voltage of the SEIG stable. In DSTATCOM, a certain level of active current is required to maintain the DC bus voltage; otherwise, the DC bus voltage may drop over time, and the system may lose stability. The active component (i_{sd}) is used to regulate the DC bus voltage. This component is calculated with the help of i_d and i_q components. For the active component current (i_{sd}), the measured DC bus voltage (V_{dc}) is compared with the reference voltage value (V_{dcref}) and the error signal resulting from this voltage difference is transmitted as input to the PI controller. The DC bus voltage error is expressed as follows:

$$V_{dcer(n)} = V_{dcref(n)} - V_{dc(n)} \quad (2)$$

The output of the PI controller gives the i_{loss} value, which is calculated as follows:

$$i_{loss(n)} = i_{loss(n-1)} + K_{pd}\left(V_{dcer} - V_{dcer(n-1)}\right) + K_{id}V_{dcer(n)} \quad (3)$$

The active component i_{sd}, is calculated using the value of i_{loss}, which is generated at the output of the PI controller, as shown in Eq. (4).

$$i_{sd} = \frac{i_{db} + \bar{i_d}}{3} \tag{4}$$

To prevent the voltage drop of the SEIG, the necessary reactive power must be supplied. To control the amplitude of the SEIG's voltage, the reactive component of the source reference currents ($i^*_{sa}, i^*_{sb}, i^*_{sc}$), denoted as i_{sq}, is used. For this purpose, the peak value of the SEIG's voltage must first be calculated. The peak amplitude of the SEIG's voltage is determined as follows:

$$V_t = \sqrt{\frac{2}{3}(v_a^2 + v_b^2 + v_c^2)} \tag{5}$$

This value is compared with the reference value of the voltage amplitude (V_{tref}), and the resulting error is fed into the PI controller. The error for the peak voltage of the SEIG is expressed as follows:

$$V_{ter(n)} = V_{tref(n)} - V_{t(n)} \tag{6}$$

In this context, V_{tref} represents the reference SEIG voltage, and $V_{t(n)}$ corresponds to the measured instantaneous SEIG terminal voltage. The output of the PI controller provides the i_{qr} value, which is calculated as

$$i_{qr(n)} = i_{qr(n-1)} + K_{pq}\left(V_{ter} - V_{ter(n-1)}\right) + K_{iq}V_{ter(n)} \tag{7}$$

As such, K_{pq} and K_{iq} represent the proportional and integral gains of the PI controller, respectively. The reactive component of the current (i_{sq}) is obtained using the value of i_{qr}, which is generated at the output of the PI controller, as expressed in Eq. (8).

$$i_{sq} = \frac{i_{qr} + \bar{i_q}}{3} \tag{8}$$

The obtained i_{sd} and i_{sq} currents are used to calculate the reference source currents ($i^*_{sa}, i^*_{sb}, i^*_{sc}$), through the dq-to-abc transformation.

$$\begin{bmatrix} i^*_{sa} \\ i^*_{sb} \\ i^*_{sc} \end{bmatrix} = \begin{bmatrix} \cos\theta & \sin\theta & 1 \\ \cos(\theta - \frac{2\pi}{3}) & \sin(\theta - \frac{2\pi}{3}) & 1 \\ \cos(\theta + \frac{2\pi}{3}) & \sin(\theta + \frac{2\pi}{3}) & 1 \end{bmatrix} \begin{bmatrix} i_{sd} \\ i_{sq} \\ i^*_0 \end{bmatrix} \tag{9}$$

After generating the reference source currents (i^*_{sabc}), they are compared with the measured currents of the SEIG (i_{sabc}) to produce the required PWM signals. These PWM signals are applied to the IGBTs to supply the necessary active and reactive power.

3.2. CSD Based Method

The Current Synchronous Detection (CSD) method is an effective technique used in SEIG-based DSTATCOM systems for voltage regulation and the extraction of reference currents. Researchers have proposed modified versions of the CSD method to enhance its performance[6]. SOGI-based CSD approaches offer significant advantages in estimating voltage peak values and ensuring precise phase alignment, making them highly suitable for such applications. Fig. 4 shows the block diagram of the SOGI based CSD method. In this theory, load currents (i_{La}, i_{Lb}, i_{Lc}), SEIG currents (i_{sa}, i_{sb}, i_{sc}), SEIG voltages (v_a, v_b, v_c), and DC bus voltage (V_{dc}) are used as inputs.

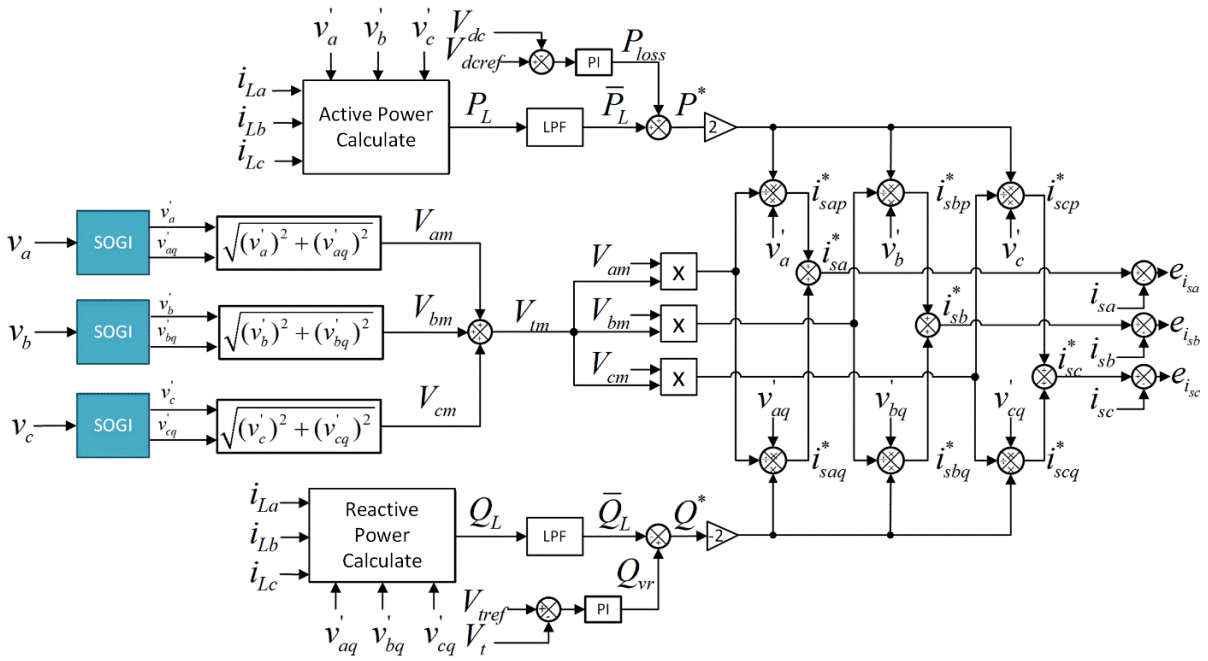

Figure 3. Block Diagram of the SOGI-Based CSD Method

The CSD theory is fundamentally based on estimating the peak values of each phase voltage. In this approach, a SOGI filter is used to filter each phase individually. To calculate the peak values of the phase voltages, the phase signal itself and its 90-degree lagged version are required. In Fig. 4, the output v_a' of the SOGI represents the phase signal itself, while the output v'_{aq} provides its 90-degree lagged version. Using these outputs, the peak values of the phase voltages are calculated as follows:

$$V_{am} = \sqrt{(v'_a)^2 + (v'_{aq})^2}\,;\; V_{bm} = \sqrt{(v'_b)^2 + (v'_{bq})^2}\,;\; V_{cm} = \sqrt{(v'_c)^2 + (v'_{cq})^2} \tag{10}$$

In three-phase systems, the instantaneous power of the load is calculated as follows by taking the product of phase voltages and phase currents:

$$P_L = v'_a i'_{La} + v'_b i'_{Lb} + v'_c i'_{Lc} \tag{11}$$

Here, i_{La}, i_{Lb} and i_{Lc}, represent the load currents. Since the load's active power is calculated without filtering the load currents, it contains both DC ($\overline{P_L}$) and AC ($\widetilde{P_L}$) components. To ensure high-quality output power from the SEIG, oscillations in the load's active power must be eliminated. A commonly used simple method for this purpose is to apply a low-pass filter (LPF). The output of the LPF is expressed as follows:

$$\overline{P_L} = P_L - \widetilde{P_L} \tag{12}$$

To prevent the drop in the DC bus voltage, the reference active power (P^*) is calculated by comparing the reference DC voltage (V_{dcref}) with the instantaneous DC voltage (Vdc). The resulting error is fed into the PI controller. The output of the PI controller provides the value of the power loss (P_{loss}). At the nth sampling instant, the DC bus voltage error, V_{dcer}, is given by.

$$V_{dcer(n)}(n) = V_{dcref}(n) - V_{dc}(n) \tag{13}$$

Here, $V_{dc(n)}$ represents the DC bus reference voltage, while $V_{dc(n)}$ denotes the measured instantaneous DC bus voltage. To maintain the DC bus voltage at the reference value, the output of the PI controller is defined as:

$$P_{loss}(n) = P_{loss}(n-1) + K_{pd}\left(V_{dcer}(n) - V_{dcer}(n-1)\right) + K_{id}V_{dcer}(n) \quad (14)$$

In this context, $P_{loss}(n)$ represents the active power required to compensate for the losses in the STATCOM. K_{pd} and K_{id} are the proportional and integral gain constants of the PI controller for the DC bus voltage, respectively. To obtain the reference active power (P^*), the P_{loss} value is added to the filtered active power of the load.

$$P^* = P_{Loss} + \overline{P_L} \quad (15)$$

To control the switching signals required for the IGBTs in the DSTATCOM structure, the calculation of reference currents is necessary. These reference currents consist of two components: active and reactive. The active components, used for regulating the DC bus voltage, are determined using the following expression:

$$i^*_{sap} = \frac{2P^* v'_a}{\bar{V}_{tm} V_{am}}; \quad i^*_{sbp} = \frac{2P^* v'_b}{\bar{V}_{tm} V_{bm}}; \quad i^*_{scp} = \frac{2P^* v'_c}{\bar{V}_{tm} V_{cm}} \quad (16)$$

To ensure that the terminal voltage remains at the desired reference value, it is necessary to calculate the reactive components. This begins with determining the instantaneous reactive power consumed by the load, which can be derived as shown below:

$$Q_L = v'_{aq} i'_{La} + v'_{bq} i'_{Lb} + v'_{cq} i'_{Lc} \quad (17)$$

The instantaneous reactive power of the load (Q_L) may exhibit oscillations due to nonlinear loads, similar to the active power. To prevent the reference currents from being affected by these oscillations, the reactive power must be filtered to eliminate such variations. A low-pass filter (LPF) is used for this purpose, and its output is represented as:

$$\overline{Q_L} = Q_L - \widetilde{Q_L} \quad (18)$$

To determine the reactive power required by both the SEIG and the load, the reference reactive power (Q^*) is necessary. The calculation of the reference reactive power requires the peak value of the SEIG's terminal voltage (V_t), which is determined as follows:

$$V_t = \frac{V_{am} + V_{bm} + V_{cm}}{3} = \frac{V_{Tm}}{3} \quad (19)$$

The calculated peak voltage of the SEIG (V_t) is compared with the reference peak voltage (V_t^*), and the resulting voltage error is fed into the PI controller. The voltage error of the SEIG, denoted as V_{ter}, at the nth sampling instant is expressed as:

$$V_{ter}(n) = V_{tref}(n) - V_t(n) \quad (20)$$

The output of the PI controller provides the reactive power required by the SEIG.

$$Q_{VR}(n) = Q_{VR}(n-1) + K_{pa}(V_{ter}(n) - V_{ter}(n-1)) + K_{ia}V_{ter}(n) \quad (21)$$

Here, K_{pa} and K_{ia} represent the proportional and integral gain constants of the PI controller, respectively, while V_{ter}(n) and V_{ter}(n−1) denote the voltage errors at the nth and (n−1)th sampling instants, respectively. To obtain the reference reactive power (Q^*), the load's reactive power (Q_L) is subtracted from the reactive power required by the SEIG.

$$Q^* = Q_{VR} - \overline{Q_L} \tag{22}$$

After completing all these steps, the reactive power components of the reference currents required for switching the IGBT are determined as:

$$i^*_{saq} = \frac{2Q^* v'_{aq}}{\bar{V}_{tm} V_{am}}; \quad i^*_{sbq} = \frac{2Q^* v'_{bq}}{\bar{V}_{tm} V_{bm}}; \quad i^*_{scq} = \frac{2Q^* v'_{cq}}{\bar{V}_{tm} V_{cm}} \tag{23}$$

As a result, the calculated active and reactive power components are summed to derive reference currents.

$$i^*_{sa} = i^*_{sap} + i^*_{saq}; \quad i^*_{sb} = i^*_{sbp} + i^*_{sbq}; \quad i^*_{sc} = i^*_{scp} + i^*_{scq} \tag{24}$$

The reference currents (i_{sa}*, i_{sb}*, i_{sc}*) are compared with the measured currents of the SEIG (i_{sa}, i_{sb}, i_{sc}), and the resulting error signals (e_{isa}, e_{isb}, e_{isc}) are defined accordingly. These error signals are then compared with a triangular waveform to generate the switching signals required for the DSTATCOM.

$$e_{isa} = i^*_{sa} - i_{sa}; \quad e_{isb} = i^*_{sb} - i_{sb}; \quad e_{isc} = i^*_{sc} - i_{sc} \tag{25}$$

4. Results and Discussion

In this study, the performance of a DSTATCOM-based SEIG is compared using the dq method and SOGI-based CSD. Tests are conducted under challenging scenarios commonly encountered in practical applications, including nonlinear loads, unbalanced loads, and DC offset conditions in currents and voltages. Nonlinear loads threaten the stability of electrical systems by generating harmonics, while unbalanced loads cause voltage and current imbalances between phases, significantly impacting system performance.

Table 1. SEIG and DSTATCOM Parameters

SEIG Parameters	
Power	15 kW
Voltage (L-L)	400 V
Stator resistance	0.2147 Ω
Stator inductance	0.000991H
Rotor resistance	0.2205 Ω
Rotor inductance	0.000991 H
Mutual inductance	0.06419 H
Frequency	50 Hz
Pole pairs	2
Excitation capacitor bank	C = 290µF (Y-connected)
DSTATCOM Parameters	
Interfacing inductor *(Lf)*	15 mH
DC bus capacitor (C_{dc})	2500 µF
Switching frequency	10 kHz
Reactive Power Capacity	~33.96 kVAr

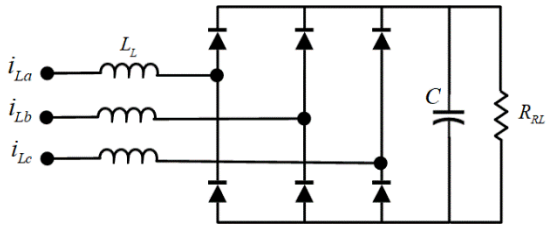

Figure 4. Three-phase diode rectifier with capacitive filter and resistive load.

Additionally, DC offset conditions lead to saturation in measurement and control circuits, resulting in errors in voltage regulation. These test scenarios are critical for evaluating the effectiveness of control methods not only under ideal conditions but also in real-world situations where such challenges are likely to occur. The results provide a detailed assessment of the voltage regulation performance of both methods under various load and operating conditions.

4.1. Performance of DSTATCOM-based SEIG under Nonlinear Load

In the first test, a three-phase diode rectifier with a resistive load and capacitive filter is connected to the SEIG terminals as a nonlinear load (as shown in Fig. 4). Fig. 5 shows the performance of the dq method under nonlinear load conditions while Fig. 6 demonstrates the performance of the SOGI-based CSD control method under the same conditions. In these figures, the load currents (i_{Labc}), the currents injected by DSTATCOM (i_{fabc}), SEIG currents (i_{sabc}), SEIG terminal voltages (v_a, v_b, v_c), amplitude of the SEIG voltages (V_t), and the DC bus voltage (V_{dc}) are given, respectively.

As observed in Fig. 5a and 6a, nonlinear loads draw currents containing harmonics. These harmonic currents can adversely affect the SEIG currents. DSTATCOM provides the necessary compensation to prevent these harmonic contents of the load currents from impacting the SEIG currents. Consequently, the performance of the control algorithms determining these currents is of critical importance.

An effective control algorithm ensures that the SEIG currents and voltages remain balanced and sinusoidal even if the load currents contain harmonics. The currents injected by DSTATCOM are shown in Fig. 5b and 6b. Fig. 5c and 6c clearly show that the SEIG currents are balanced under both algorithms thanks to the currents injected by DSTATCOM. Similarly, Figs 5d and 6d indicate that the SEIG voltages are also balanced under these conditions.

In the dq method, the V_t value is calculated using Equation 5. Since this method uses unfiltered PCC voltages, the V_t value exhibits slight oscillations, as shown in Fig. 5e. In contrast, in the SOGI-based CSD method, the V_t value is calculated using Equation 19. Because the V_{am}, V_{bm}, and V_{cm} values used in this equation are filtered through the SOGI, the oscillations in V_t are significantly reduced, as seen in Fig. 6e.
The DC bus voltage required by DSTATCOM to produce high quality voltage and current shows similar results for both methods (Fig. 5f and 6f). Approximately 2.5 V oscillation occurs in both methods. However, the DC bus value is closer to the reference in the dq method.

Fig. 7 presents the active and reactive power profiles of the load, SEIG, and DSTATCOM under nonlinear load conditions using the dq method. As observed, DSTATCOM effectively compensates for the reactive power demand and maintains power balance in the system.
Fig. 8 shows similar results for the SOGI-based CSD method, confirming its ability to support the SEIG in maintaining stable power flow under nonlinear load conditions.

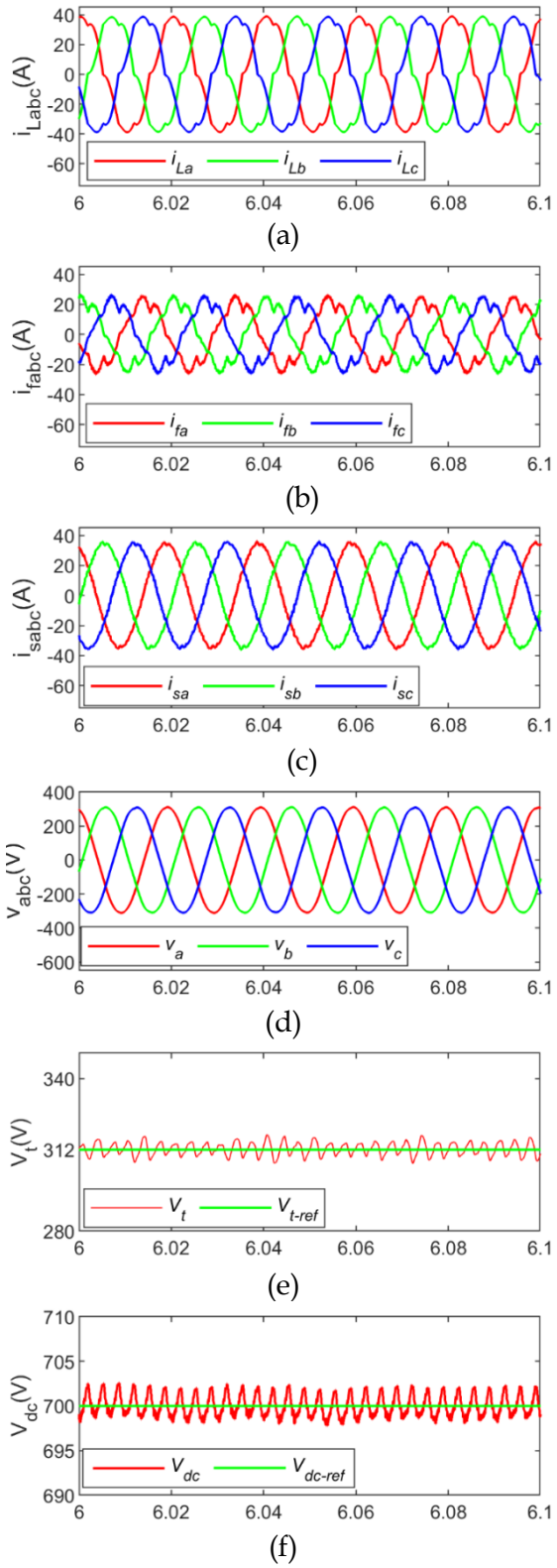

Figure 5. Performance of proposed dq nethod under nonlinear load (a) Load currents, (b) DSTATCOM currents, (c) SEIG currents, (d) SEIG terminal voltages, (e) Amplitude of SEIG voltages, and (f) DC bus voltage.

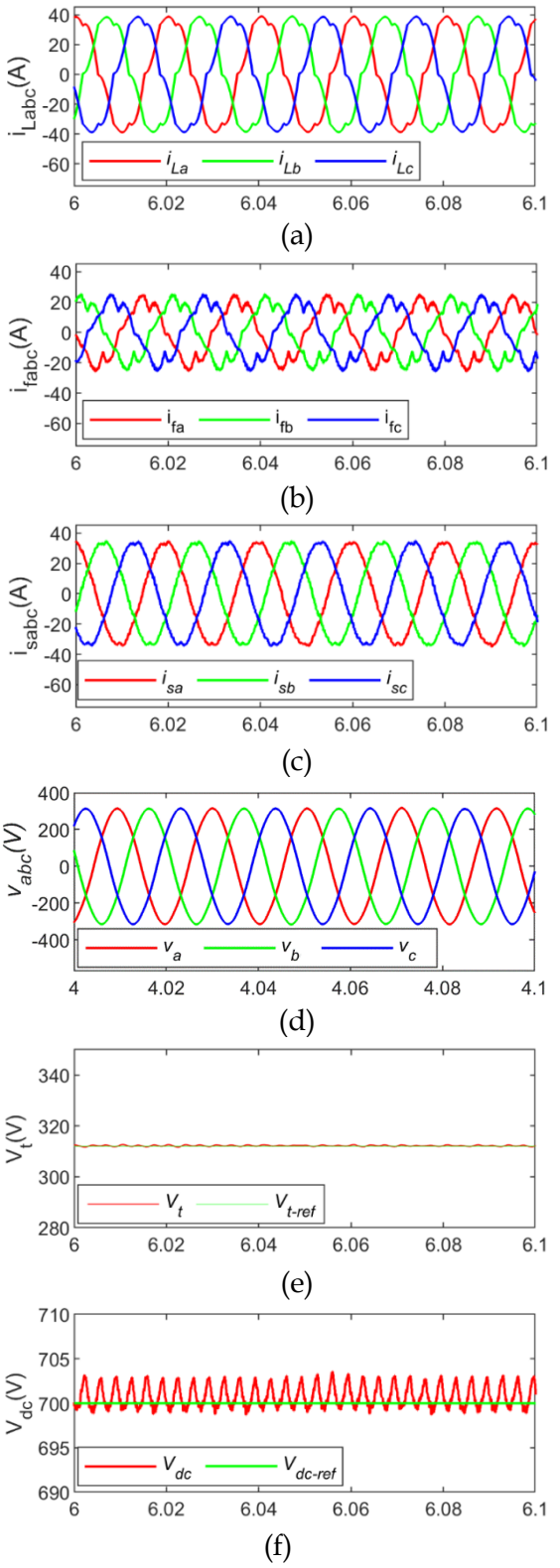

Figure 6. Performance of proposed SOGI-based CSD method under nonlinear loads (a) Load currents, (b) DSTATCOM currents, (c) SEIG currents, (d) SEIG terminal voltages, (e) Amplitude of SEIG voltages, and (f) DC bus voltage.

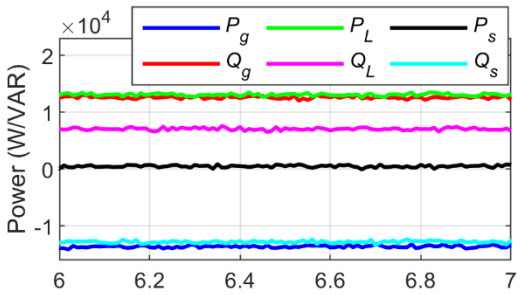

Figure 7. Active-reactive power performance of the SEIG-DSTATCOM system under nonlinear load using dq method.

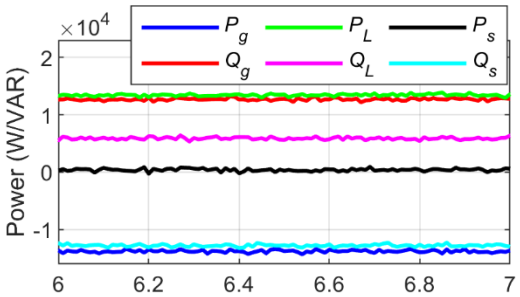

Figure 8. Active-reactive power performance of the SEIG-DSTATCOM system under nonlinear load using SOGI-CSD method.

Fig. 9 presents the THD results for the dq method, while Fig. 10 shows the THD results for the SOGI-based CSD method for nonlinear loads. In Fig. 9a, the THD of the load current is measured as 8.92%, while in Fig. 10a, it is 9.12%. Although the load remains the same, the difference in THD values of the load currents arises from the performances of the control algorithms. The control method providing better compensation for harmonic contents in voltages, indirectly affects the THD of load currents positively. The THD of SEIG currents is obtained as 3.27% in the dq method and 3.99% in the SOGI-CSD method. The THD of SEIG voltages is 1.33% for the dq method and 1.57% for the SOGI-CSD method. These results indicate that the dq method demonstrates better performance under nonlinear load conditions.

Since the dq method uses the PCC voltages directly in the control process, reference signals are produced faster. In this way, faster responses are provided to dynamic load changes. In the SOGI-CSD method, the delays that occur during the filtering of the PCC voltages and the simple structure of the method have reduced its performance compared to the dq method. When the SEIG current, voltage and their THD ratios are examined, it highlighted the performance of the dq method, especially under nonlinear load conditions.

4.2. Performance of DSTATCOM-based SEIG under Unbalanced Loads

Fig. 11 and 12 illustrate the performance of the proposed control algorithms for the SEIG system under unbalanced load conditions. Fig. 11 shows the results obtained using the dq method, while Fig. 12 presents the results for the SOGI-based CSD method. In this test, unbalanced loads consisting of 12Ω, 10Ω, and 8Ω resistances are connected across the phases, creating an imbalance in the system. These unbalanced loads draw currents of varying magnitudes from the phases, leading to system instability. DSTATCOM compensates for these imbalances and provides stability in the SEIG currents and voltages.

As shown in Fig. 11a and 12a, due to unbalanced loads, the load currents exhibit significant imbalances. As depicted in Fig. 11b and 12b, the DSTATCOM effectively mitigates these phase imbalances by injecting compensatory currents. Consequently, as seen in Figures 11d and 12d, the imbalances in SEIG currents and voltages are eliminated thanks to the currents injected by DSTATCOM. When examining the terminal peak values (V_t), a slight oscillation is observed in the dq method (Fig. 11e). However, the SOGI-based CSD method filters the voltages prior to computation, resulting in significantly reduced oscillations, as demonstrated in Fig. 12e.

In both algorithms, as shown in Fig. 11f and 12f, the DC bus voltage exhibits an oscillation of approximately 2 V. Despite the observed oscillations, the DC bus voltage maintains stability throughout the tests.

In 3P3W systems that lack a neutral line, zero-sequence currents cannot be present due to the absence of a return path. Therefore, the control strategies mainly focus on compensating negative-sequence components in order to balance the system.

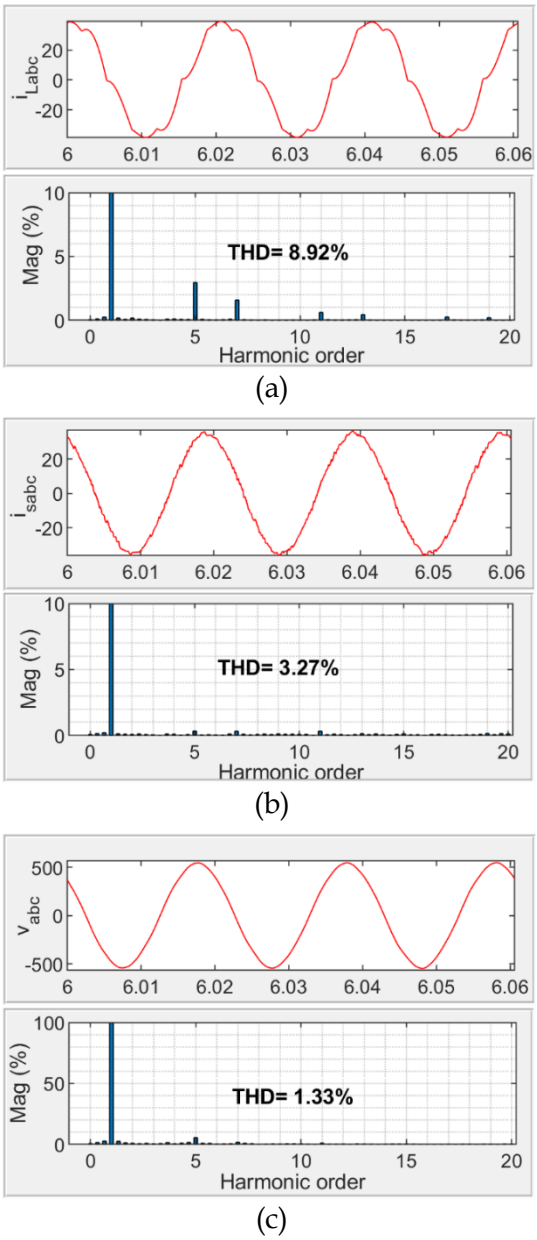

Figure 9. Performance of proposed dq method under nonlinear load (a) Load current and its THD, (b) SEIG current and its THD, and (c) SEIG terminal voltage and its THD.

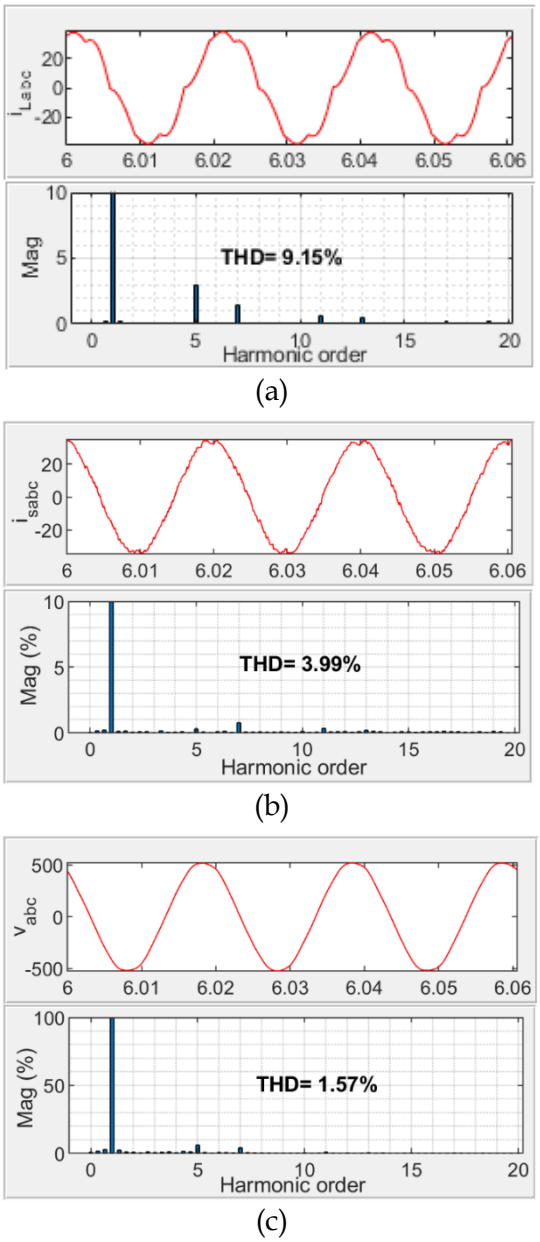

Figure 10. Performance of proposed SOGI-based CSD method under nonlinear load (a) Load current and its THD, (b) SEIG current and its THD, and (c) SEIG terminal voltage and its THD.

As demonstrated in the simulation results, both the dq and SOGI-based CSD methods contribute to the mitigation of current and voltage imbalances under unbalanced load conditions. By injecting appropriate compensating currents, DSTATCOM ensures that the SEIG continues to operate with balanced and stable output voltages and currents.

The active and reactive power responses under unbalanced load conditions are shown in Figs. 13 and 14 for both dq and SOGI-based CSD methods, respectively. These figures demonstrate the capability of both control strategies to regulate power flow and mitigate the impact of load imbalance.

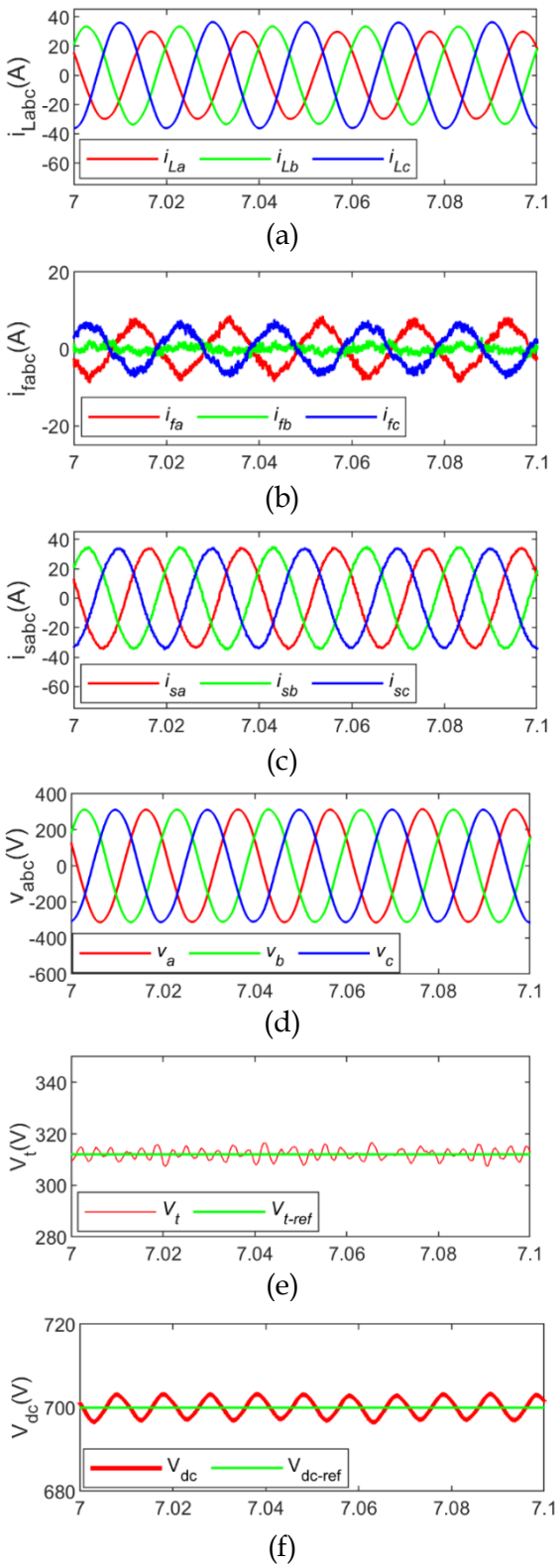

Figure 11. Performance of proposed dq method CSD method under unbalanced loads (a) Load currents, (b) DSTATCOM currents, (c) SEIG currents, (d) SEIG terminal voltages, (e) Amplitude of SEIG voltages, and (f) DC bus voltage.

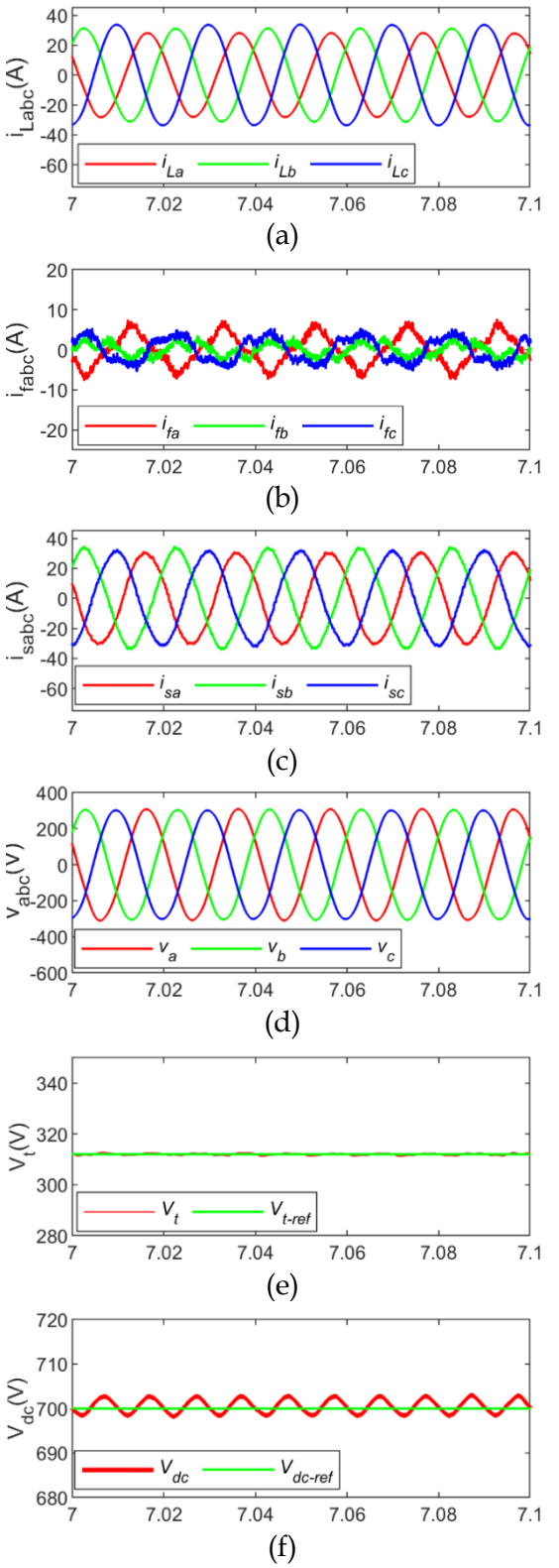

Figure 12. Performance of proposed SOGI-based CSD method under unbalanced loads (a) Load currents, (b) DSTATCOM currents, (c) SEIG currents, (d) SEIG terminal voltages, (e) Amplitude of SEIG voltages, and (f) DC bus voltage.

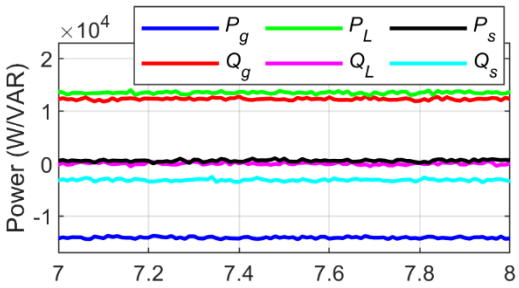

Figure 13. Active-reactive power performance of the SEIG-DSTATCOM system under unbalanced load using dq method.

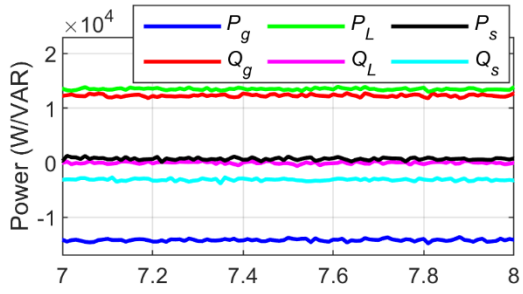

Figure 14. Active -reactive power performance of the SEIG-DSTATCOM system under unbalanced load using SOGI-CSD method.

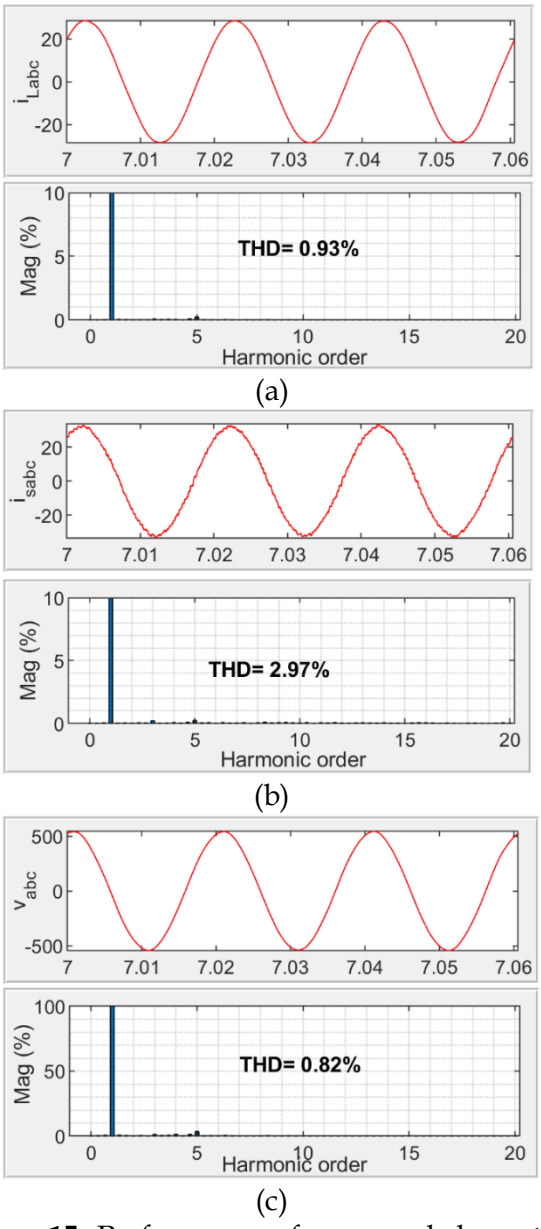

Figure 15. Performance of proposed dq method under unbalanced load (a) Load current and its THD, (b) SEIG current and its THD, and (c) SEIG terminal voltage and its THD.

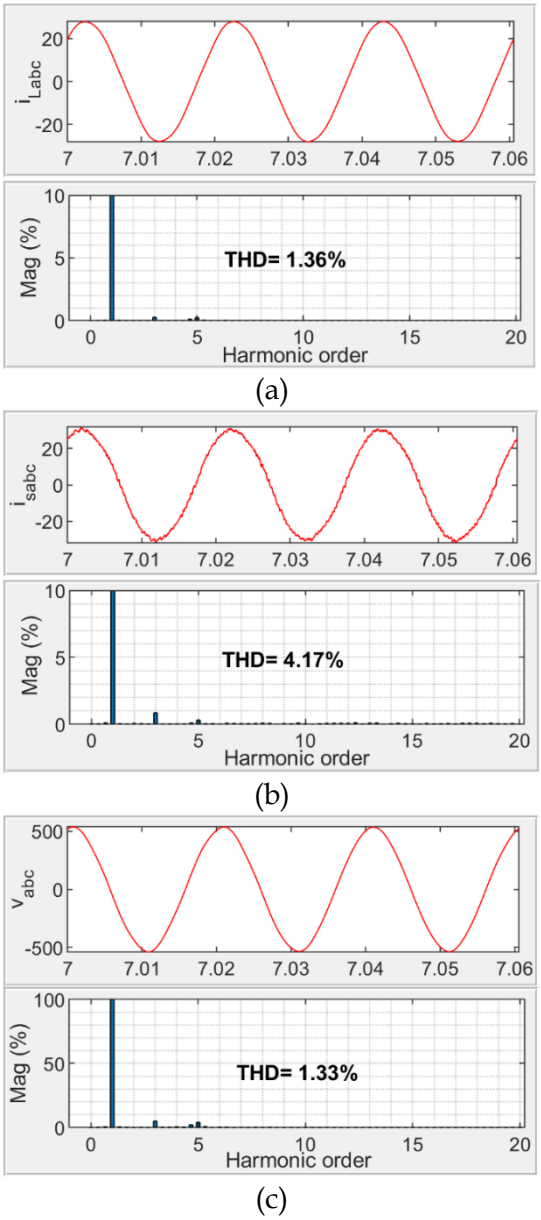

Figure 16. Performance of proposed SOGI-based CSD method under unbalanced load (a) Load current and its THD, (b) SEIG current and its THD, and (d) SEIG terminal voltage and its THD.

The THD analysis more clearly highlights the performance differences between the two methods. Figures 15 and 16 detail the THD results for the dq and SOGI-based CSD methods, respectively. In Figure 15a, the dq method presents a load current THD of 0.93%, while the SOGI-based method in Figure 16a presents a slightly higher THD of 1.36%. The THD of the SEIG currents is 2.97% with the dq method (Figure 15b) and 4.17% with the SOGI-based method (Figure 16b). Similarly, the THD of the SEIG voltages is lower for the dq method at 0.82% (Figure 15c) and 1.33% for the SOGI-based method (Figure 16c).

Overall, the results show that the dq method outperforms the SOGI-based CSD method under unbalanced load conditions.

4.3. Performance of DSTATCOM-based SEIG under in the DC-Offset

In this test, to evaluate the performance of the two control algorithms, DC offset components were added to the measured load currents at 7.1 seconds. At 7.2 seconds, DC offsets were added to the SEIG voltages in addition to the DC offsets in the currents. DC offsets applied to the SEIG voltages were 20 V, -20 V and 30 V, while DC offsets of 5 A, -2 A and 3 A were applied to the load currents, respectively.

Fig.17a and 18a illustrate the load currents with the applied DC offsets, and Fig.17b and 18b show that the DSTATCOM currents undergo waveform changes starting at 7.2 seconds due to the DC offsets.

In the dq method, despite the DC offset in the measured currents and voltages, the SEIG currents (Fig. 17c) and voltages (Fig. 17d) are correctly generated and remain balanced. In contrast, in the SOGI-CSD method, the SEIG currents show slight imbalances (Fig. 18c), but the SEIG voltages remain balanced (Fig. 18d).

The SEIG voltage amplitude (V_t), calculated using the dq method and presented in Fig. 17e, begins to oscillate at 7.2 seconds due to the influence of the DC offsets, as it is derived directly from the measured voltages (according to Eq. 5). Conversely, the SOGI-CSD method, through its filtering mechanism, shows reduced oscillations in the SEIG voltage amplitude (Fig. 18e).

Examination of the DC bus voltages (V_{dc}) reveals that the dq method maintains values closer to the reference and exhibits more stable performance (Fig. 17f), whereas the DC offsets introduced to the SEIG voltages in the SOGI-CSD method result in more pronounced oscillations (Fig. 18f).

In DC offset conditions, offset components injected into the load current and voltage may negatively affect the system performance if not handled properly. The control strategies used in this study are designed to suppress the propagation of DC components to the source side. According to the results, both methods maintain system stability under DC offset, with the dq method achieving slightly better performance in maintaining the DC bus voltage and minimizing oscillations. This shows that the control algorithms are effective in preserving system reliability under abnormal load conditions.

Figures 19 and 20 illustrate the power performance of the dq and SOGI-based CSD methods, respectively, under DC offset conditions. Both methods manage to stabilize active and reactive power despite the presence of offset components in the load.

According to the Total Harmonic Distortion (THD) values presented in Fig. 21 and 22, the dq method yields a THD of 3.41% for the SEIG currents, compared to 4.69% for the SOGI-CSD method. For the SEIG voltages, both methods present similar THD values of approximately 2.65%. In conclusion, although neither method is completely immune to the effects of DC offsets, the dq method overall produces smoother current waveforms and lower harmonic distortion, thereby demonstrating better performance. Moreover, the THD values for both SEIG currents and voltages remain below the 5% threshold specified by the IEEE-519-2014 standard.

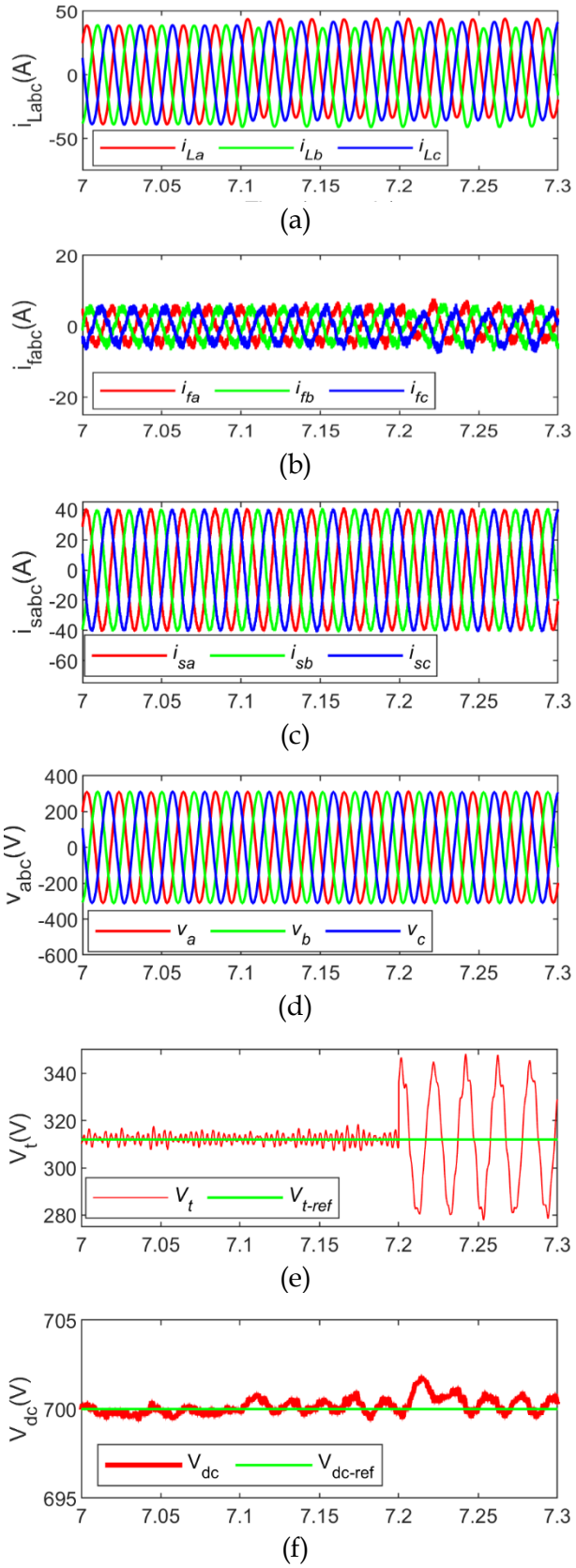

Figure 17. Performance of proposed dq method under DC offset (a) Load currents, (b) DSTATCOM currents, (c) SEIG currents, (d) SEIG terminal voltages, (e) Amplitude of SEIG voltages, and (f) DC bus voltage.

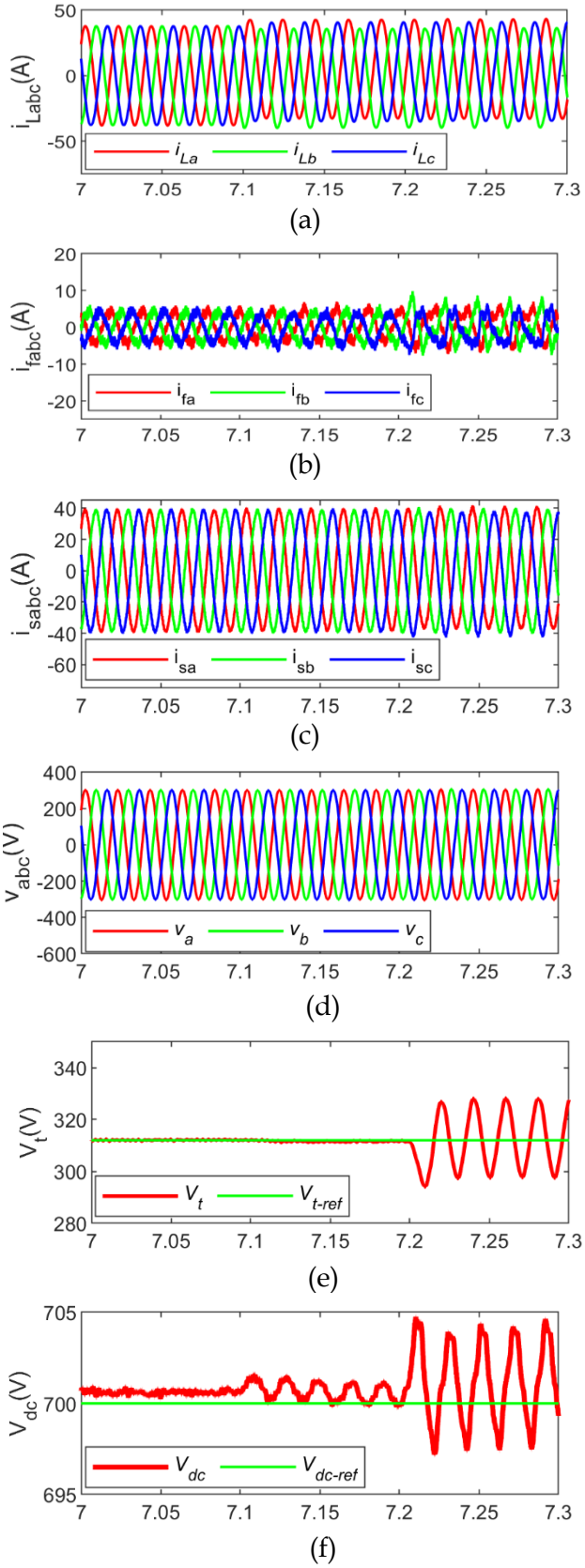

Figure 18. Performance of proposed SOGI-based CSD method under DC offset (a) Load currents, (b) DSTATCOM currents, (c) SEIG currents, (d) SEIG terminal voltages, (e) Amplitude of SEIG voltages, and (f) DC bus voltage.

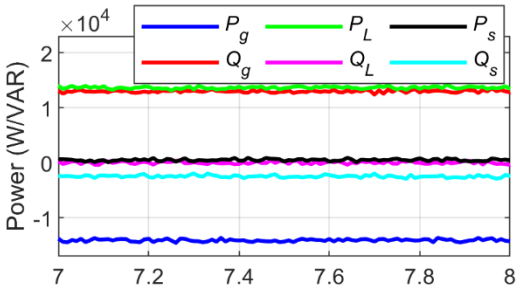

Figure 19. Active-reactive power performance of the SEIG-DSTATCOM system under DC offset condition using dq method.

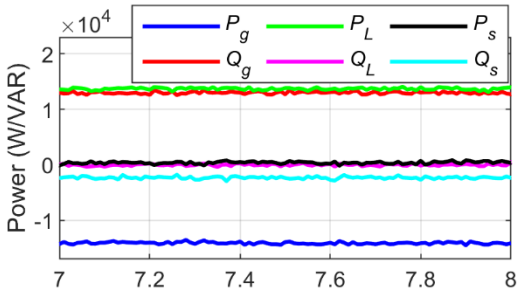

Figure 20. Active -reactive power performance of the SEIG-DSTATCOM system under DC offset condition using SOGI-CSD method.

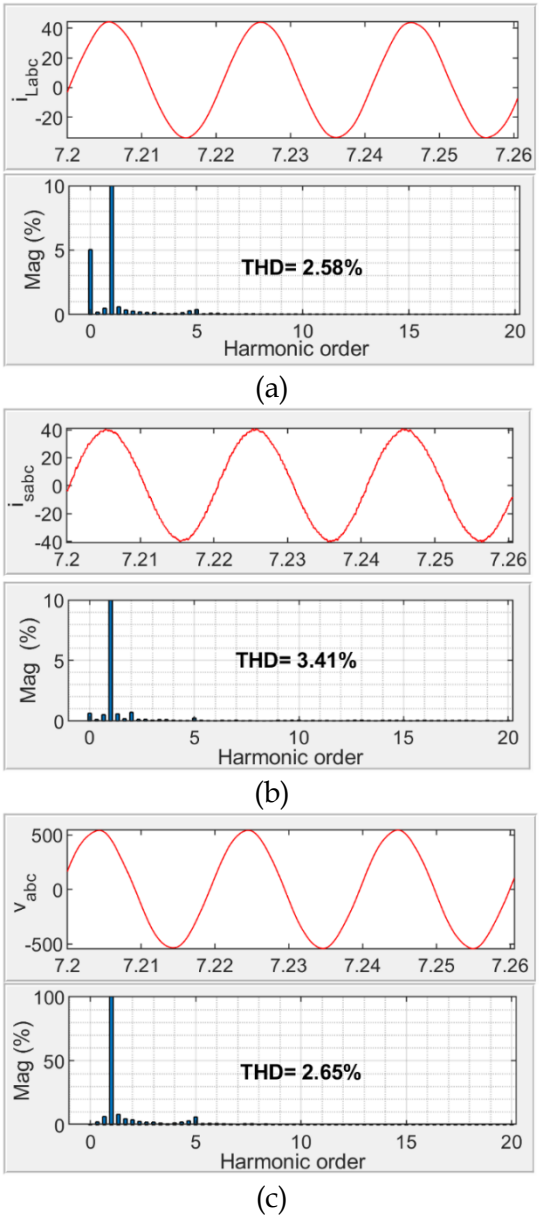

Figure 21. Performance of proposed dq method under DC offset condition (a) Load current and its THD, (b) SEIG current and its THD, and (c) SEIG terminal voltage and its THD.

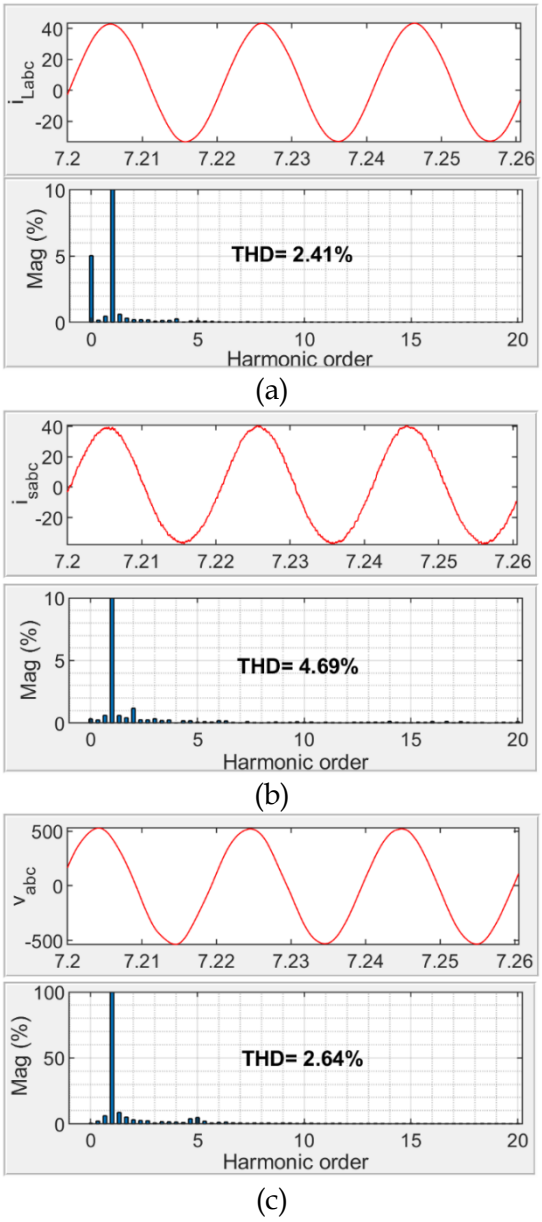

Figure 22. Performance of proposed SOGI-based CSD method under DC offset condition (a) Load current and its THD, (b) SEIG current and its THD, and (c) SEIG terminal voltage and its THD

Table 2 presents a comparative summary of the total harmonic distortion (THD) values for both dq and SOGI-based CSD methods under different operating conditions. It is observed that the dq method generally achieves lower THD levels in SEIG currents and voltages across all test cases. Especially under unbalanced load and DC offset conditions, the dq method demonstrates superior harmonic suppression performance. Although the SOGI-CSD method also keeps THD values within acceptable limits, the results confirm that the dq method provides more consistent power quality improvement.

Table 2. Comparison of THDs for DSTATCOM Control Theories

	SRF-PLL based dq-theory			SOGI-CSD theory		
Test Conditions	Load current	SEIG current	SEIG voltage	Load current	SEIG current	SEIG voltage
Nonlinear load	8.92%	3.27%	1.33%	9.15%	3.99%	1.57%
Unbalanced load	0.93%	2.97%	0.82%	1.36%	4.17%	1.33%
dc-offset	2.58%	3.41%	2.65%	2.41%	4.69%	2.64%

5. Conclusions

The performances of the dq method and csd method are compared under nonlinear loads, unbalanced loads and DC offset condition. dq method provides superior performance by providing direct control of active and reactive power in the SEIG system. Under nonlinear load conditions, it effectively reduces the effect of harmonics and ensures the generation of balanced and smooth current and voltage waveforms. In unbalanced load scenarios, it successfully compensates for phase imbalances in both current and voltage, maintaining system stability. Moreover, under DC offset conditions, the dq method not only ensures the accuracy of both current and voltage generation, but also maintains stable system performance by keeping the DC bus voltage close to the reference value. Under these conditions, the SOGI-CSD method also produces comparable results, especially excellent in estimating phase voltages and PCC peak voltage. It stands out with its simple structure as it does not include transformations in the control scheme. However, when the THD levels of current and voltage are compared, the dq method shows superior performance. In addition, the THD values for both current and voltage in each method remain within the acceptable limits specified by the relevant IEEE-519 standard. As a result, although both algorithms operate within acceptable performance limits, the dq method stands out due to its superior control mechanism and harmonic suppression capabilities.

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Conflict of Interests

The authors of the article declare that they have no personal or financial conflict of interest with any institution, organization or person.

References

[1] Sibrahim M, Aissou S, Rouas R, Haddad S, Benamourche N. Experimental determination of minimum capacitor for self-excitation of induction generators. International Journal of Power Electronics and Drive Systems (IJPEDS) 2024; 15: 109–116.

[2] Singh G, Singh V. SEIG-based transient and steady-state analysis using dragon fly approach. Soft Computing 2022; 1–13.

[3] Giri AK, Arya SR, Maurya R, Chittibabu B. Control of VSC for enhancement of power quality in off-grid distributed power generation. IET Renewable Power Generation 2020; 14: 771–778.
[4] Dwari B, Arya SR, Chilipi R. Enhancing power quality with optimized PI controller in three-phase four-wire wind energy system. Electrical Engineering 2024; 1–19.
[5] Chilipi R, Sumnait AA, Singh B. Control of self-excited induction generator-based micro-hydro power generation system feeding single-phase and three-phase loads. In: 2020 IEEE Industry Applications Society Annual Meeting. IEEE; 2020; 1–8.
[6] Singh B, Murthy S, Reddy R, Arora P. Implementation of modified current synchronous detection method for voltage control of self-excited induction generator. IET Power Electronics 2015; 8: 1146–1155.
[7] Lolamo M, Kumar R, Sharma V. Enhancing power quality of PV-DSTATCOM integrated grid with modified adaptive LMS control. Electrical Engineering 2024; 1–14.
[8] Özer AS, Sevilmis F, Karaca H, Arabaci H. Enhanced control method for voltage regulation of DSTATCOM based SEIG. Energy Reports 2022; 8: 839–847.
[9] Özer, AS., Karaca, H., & Sevilmiş, F. APF Based Control Algorithm for Voltage Regulation of Self Excited Induction Generator Using DSTATCOM. International Conferences on Science and Technology (ICONST) 2023; 327-332
[10] Katole DN, Daigavane MB, Gawande SP, Daigavane PM. Modified single phase SRF dq theory based controller for DVR mitigating voltage sag in case of nonlinear load. Journal of Electromagnetic Analysis and Applications 2017; 9: 22–33.
[11] Sevilmis F, Karaca H. Performance analysis of SRF-PLL and DDSRF-PLL algorithms for grid interactive inverters. International Advanced Researches and Engineering Journal 2019; 3: 116–122.