


## DESIGN of a PULSE GENERATOR CIRCUIT for UWB COMMUNICATIONS

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Received: 09.01.2018, Accepted: 25.05.2018

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Research Article

DOI:10.22531/muglajsci.422644

### Abstract

Generation of very short pulses with a pulse width in the order of a few nanoseconds or less is a requirement for an UWB communications system. A pulse generator circuit based on the step-recovery effect of an RF transistor has been designed for the 0-960-MHz UWB system, and is presented in this paper. The pulse generator includes a linear RF amplifier with common-emitter topology and a high-pass filter following the amplifier. Input of the RF amplifier is driven by a clock signal provided by a function generator. Amplifier output includes positive amplitude and negative amplitude pulses due to rising and falling edges of the collector-emitter voltage of the transistor, respectively. Amplifier output is then fed to a high-pass filter. Low-frequency transitions are further filtered out, and the output of the high-pass filter is a pulse train consisting of very short pulses. The pulse width has been measured as about 2.5 ns using a 300-MHz digital oscilloscope.

**Keywords:** Pulse generator, UWB communications, step-recovery effect of transistors

## UWB HABERLEŞME İÇİN BİR DARBE ÜRETEEN DEVRENİN TASARIMI

### Öz

Bir UWB haberleşme sistemi için, darbe süresi birkaç nanosaniye seviyesinde veya daha az olan darbelerin üretilmesi bir gerekliliktir. Bir RF tranzistörün aşamalı-toparlanma etkisine dayalı bir darbe üreten devre 0-960-MHz UWB sistemi için tasarlanmıştır ve bu makalede sunulmaktadır. Darbe üreten devre ortak-emetör konfigürasyonlu doğrusal bir RF kuvvetlendirici ve kuvvetlendiriciyi izleyen bir yüksek-geçiren filtreden meydana gelmektedir. RF kuvvetlendiricinin girişi bir fonksiyon üretici tarafından sağlanan bir saat işareti ile sürülmektedir. Kuvvetlendirici çıkışında, tranzistörün kollektör-emetör uçları arasındaki gerilimin yükselen ve inen kenarlarından kaynaklanan sırasıyla pozitif genlikli ve negatif genlikli darbeler vardır. Kuvvetlendirici çıkışı daha sonra bir yüksek-geçiren filtreye beslenir. Düşük frekanslı işaretler yüksek-geçiren filtre tarafından yeniden süzülür. Filtrenin çıkışı çok kısa süreli darbelerden meydana gelen bir darbe dizisidir. Darbe genişliği, 300-MHz'lik bir sayısal osiloskop kullanılarak 2.5 ns civarında ölçülmüştür.

**Anahtar Kelimeler:** Darbe üretici, UWB haberleşme, tranzistörün aşamalı-toparlanma etkisi

### Cite

Yıldırım, B. S., (2018). "Design of a pulse generator circuit for UWB communications", *Mugla Journal of Science and Technology*, 4(1), 85-88.

### 1. Introduction

The core of a typical ultra-wideband (UWB) radio transmitter is a pulse generator circuit because short baseband pulses are used to transmit information. Other system blocks of an UWB transmitter are baseband processor, Gaussian filter, radio-frequency (RF) amplifier, and antenna. Federal Communications Commission (FCC) of the United States has defined the following bands for UWB communications. These are 0-960 MHz, 3.1-10.6 GHz, and 22-29 GHz bands. A pulse generator circuit using the step recovery effect (SRE) of an RF transistor is presented in this paper for the 0-960-MHz UWB. This band is suitable to design low-cost, low-power, and long-distance radios. An UWB radio generates small interference on other narrow band channels, is immune to interference, and can not be detected easily.

There are several techniques to generate very short pulses in the order of a few nanoseconds or even less. These techniques are based on the propagation delay characteristics of digital logic gates [1-3], step-recovery diodes [4-7], step-recovery effect of transistors [8], and avalanche effect of transistors [9-10]. Pulse generation using digital logic gates has not been considered since the generated pulse width is about 5 ns when HC series CMOS logic gates are used [11]. Avalanche effect is not considered since it requires high supply voltages and yields high amplitude pulses. Pulse generation using the SRE of a transistor has been described in [8] for the 3.1-10.6-GHz UWB with moderate pulse amplitudes. In this paper, the 0-960-MHz UWB has been addressed using the SRE of an RF transistor.

A pulse generator circuit based on the SRE of an RF transistor has been designed, simulated, built, and tested.

The design includes a linear RF amplifier and a high-pass filter (HPF). The RF amplifier has common-emitter topology and is driven by a clock signal provided by a function generator. When the clock signal is HIGH, the transistor is driven into saturation. Base-collector (B-C) and base-emitter (B-E) junctions are forward biased during saturation. When the clock signal is LOW, the transistor is driven to cut-off, and the B-C junction is reverse biased. If a saturated or forward biased transistor is suddenly reverse biased, the B-C junction exhibits a low impedance until the accumulated charge in the junction is removed, and the impedance then increases to a high value. This phenomenon is the key for very short pulse generation.

## 2. Design of a Pulse Generator Circuit

For the amplifier design, a BFR93A npn transistor is selected. Typical value of the transition frequency  $f_T$  of this transistor is 6 GHz [12]. However,  $f_T$  depends on the collector current  $I_C$  and the collector-emitter voltage  $V_{CE}$ . When  $I_C$  and  $V_{CE}$  are 25mA and 3V, respectively,  $f_T$  is about 5.5 GHz, as indicated in the datasheet. This makes the amplifier design feasible up to about 1.4 GHz. For the design, supply voltage  $V_{CC}$ ,  $V_{CE}$ , and  $I_C$  are selected as 6 Vdc, 3.2 Vdc, and 23.3 mA, respectively. Amplifier is designed and simulated using Ansoft Designer.

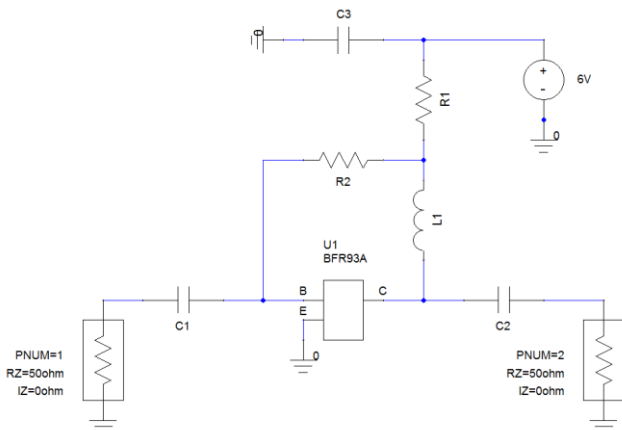


Figure 1. The linear RF amplifier using BFR93A RF transistor.

Transistor Spice parameters and equivalent circuit have been obtained from [12]. Amplifier schematic is shown in Fig. 1. R1 (120  $\Omega$ ) and R2 (10 K $\Omega$ ) are dc bias resistors. C1 (22 nF) is a coupling capacitor used for coupling of the clock signal with minimal loss to the transistor. C2 (100 pF) is also a coupling capacitor. However, by carefully selecting its value, low frequencies are filtered out at the output port. C3 (470 nF) filters out supply line voltage fluctuations. The amplifier has common-emitter topology and linear in design. L1 (120 nH) and R1 are not only a part of the dc bias circuit, but they also serve the stability of the amplifier.

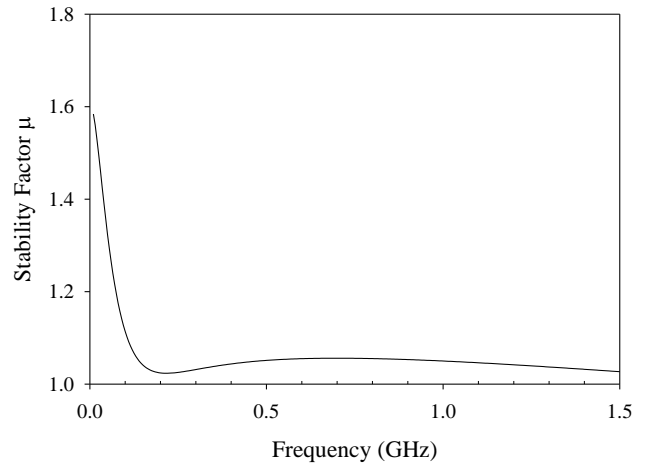


Figure 2. Stability factor  $\mu$  of the amplifier.

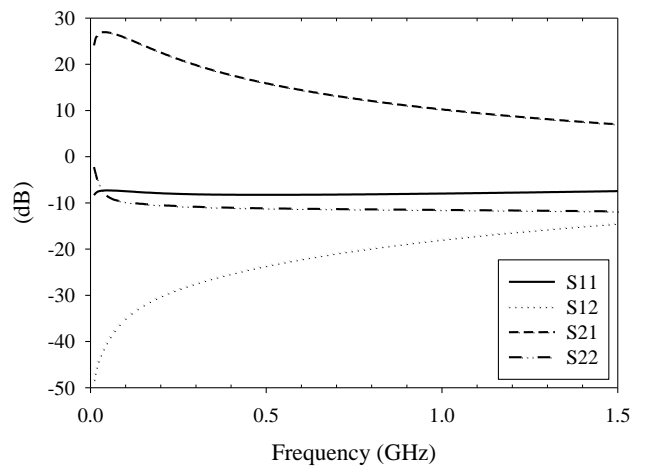


Figure 3. Simulated S-parameters of the amplifier.

Stability parameter  $\mu$  and the S-parameters of the amplifier are simulated using Ansoft Designer, and the results are shown in Fig. 2 and Fig. 3, respectively. It can be seen from Fig. 2 that the amplifier is unconditionally stable from 10 MHz to 1.5 GHz since  $\mu > 1$  within this band. From the simulated S parameters shown in Fig. 3, magnitude of S21 in decibels decreases with increasing frequency. This quantity is related to the gain of the amplifier. The simulated power gain is higher than 10 dB from 10 MHz to 1 GHz. S11 and S22 are indicators of the input and output matching performance of the amplifier, respectively. Industry accepted performance specification for S11 and S22 is about -9.6 dB or below. S22 is less than -10 dB across the band of interest, so no matching circuit is necessary for the output port. And for the input port, S11 is about -8 dB. A broadband matching circuit may be implemented to improve S11. However, it may be too complex, increase the parts count of the circuit, and may lower the gain due to insertion loss of the matching circuit. For these reasons, no matching circuit is implemented at the input port. S12 is referred as reverse gain or isolation, and it's below -20 dB up to about 1 GHz.

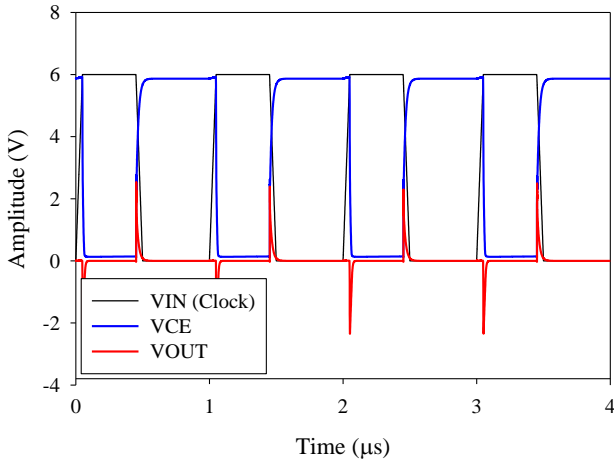


Figure 4. Transient analysis: VIN (clock input), VCE, and VOUT. Results are shown for only four clock cycles.

For the transient analysis, port 1 in the schematic is replaced by a pulsed source whose waveform resembles to a clock signal. Rise and fall times of the pulsed waveform are selected as 50 ns to be compatible with the actual clock signal from the function generator. Measured rise and fall times of the actual clock signal (CLK) from 0 to 6V and from 6 to 0 V are about 50 ns. Pulse duration is selected as 400 ns, so the overall pulse duration including rise and fall times is 500 ns. Clock duty-cycle is 50% which makes the pulse OFF time 500 ns as well. For the transient analysis, output port of the amplifier is terminated by a 50-Ω load resistor. Fig. 4 shows VIN (the clock signal), VCE, and the output voltage VOUT across the 50-Ω load resistor. VCE waveform is out-of-phase with VIN since a common-emitter amplifier produces a 180° phase shift between its input and output. VOUT exhibits positive and negative pulses which occur at the rising and falling edges of the VCE signal, respectively. The reason for these pulses is the differentiation of the VCE signal by C2.

Further filtering of the output signal VOUT is required. This is achieved by a HPF, and its schematic is shown in Fig. 5. The HPF has two short microstrip transmission line sections of about 10-mm long each and a shunt inductor. The width of the microstrip is about 2.84 mm to achieve a 50-Ω characteristic impedance on 1.5-mm thick FR4 substrate. The inductor is positioned at the center of two microstrip lines. Schematic in Fig. 5 indicates the electrical length (E) of the microstrip as 20 degrees which corresponds to about 10 mm physical length at 1 GHz. Since the total electrical length is 40 degrees, the overall microstrip line length is about 20 mm. HPF has been designed using Ansoft Designer. Fig. 6 shows the insertion loss of the HPF for different values of the shunt inductor L. Insertion loss and knee-frequency are lower for higher values of the inductor L. For the simulations, an inductance value of 10 nH has been used. The 3-dB cut-off frequency of the HPF is about 400 MHz for this value of inductance.

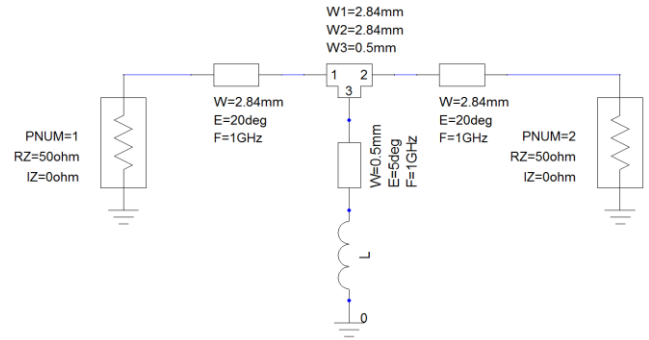


Figure 5. HPF circuit.

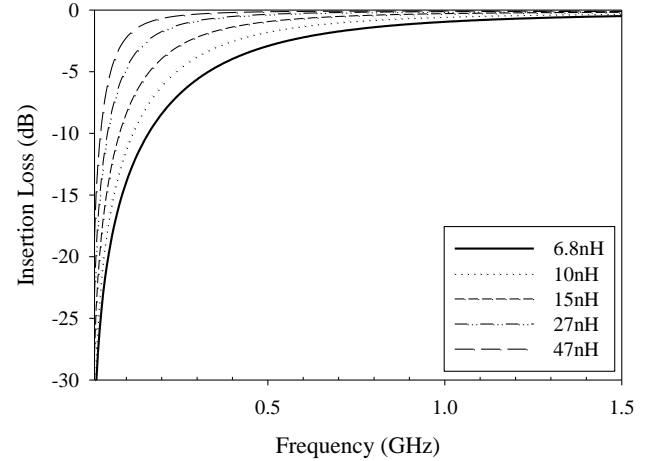


Figure 6. Simulated insertion loss of the HPF for different values of the shunt inductor L.

Amplifier output VOUT shown in Fig. 4 is applied to the input of the HPF, and the steady-state output of the HPF in time-domain is shown in Fig. 7. This waveform also is a pulse train but since the low-frequency transitions are further filtered out, the result is very short duration impulse-like pulses. These are the desired pulses for the 0-960-MHz UWB communications due to their very short pulse widths.

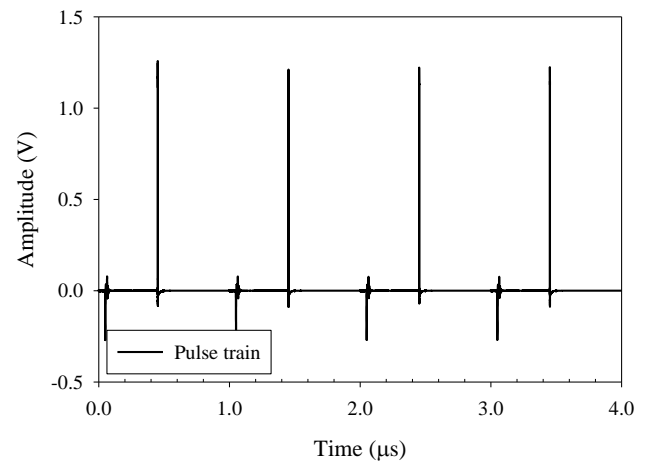


Figure 7. Simulated output of the amplifier+HPF is a pulse train. Pulse output is shown for only four clock cycles.

The amplifier and the HPF were built on 1.5-mm thick FR4 circuit boards. VCE, VBE, and IC of the amplifier were measured as about 3.0 V, 0.77 V, and 24 mA, respectively.

The measured dc operating point of the amplifier is very close to that of the simulated amplifier. A 300-MHz four-channel digital oscilloscope was used for the time-domain measurements. A 1-MHz CLK supplied from a function generator is applied at the input of the amplifier. CLK amplitude varies between 0 and 6 V. Amplifier and HPF boards use 50- $\Omega$  SMA edge-mount connectors at their input and output ports. The two boards were then connected in cascade using an SMA adapter. When the cascaded board is driven by the 1-MHz CLK supplied by the function generator, a pulse train has been obtained at the output of the HPF.

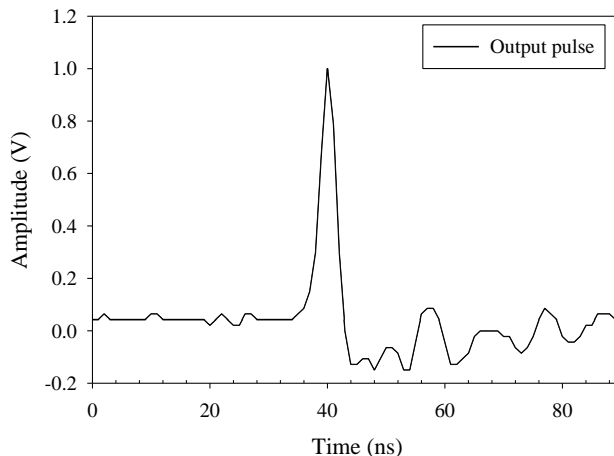


Figure 8. Measured output pulse.

For the time-domain measurements, amplifier input  $V_{IN}$ , VCE, amplifier output, and HPF output are monitored by the oscilloscope. Output of the HPF is a pulse train with impulse like pulses which are separated by 1  $\mu$ s. A single pulse from this pulse train is shown in Fig. 8. Pulse amplitude is normalized to its maximum. Measured pulse width is about 2.5 ns. Measurement accuracy is limited by the 300-MHz bandwidth of the digital oscilloscope. At least a 2-GHz oscilloscope is required to accurately measure the pulse width.

### 3. Conclusion

A low-cost pulse generating circuit for the 0-960-MHz UWB communications has been designed. The circuit includes a linear RF amplifier and a HPF. Very short pulses in the order of a few nanoseconds or less are generated due to the step-recovery effect of the RF transistor BFR93A. Measured pulse width at the output of the HPF is about 2.5 ns. Measurement accuracy is limited by the 300-MHz bandwidth of the oscilloscope. At least a 2-GHz oscilloscope is required to accurately measure the pulse width. It's demonstrated in this paper that SRE can be used to generate very short pulses in the order of a few nanoseconds. These pulses are not only used by UWB communications systems, but they can also be used in microwave imaging and radar systems.

### 4. Acknowledgment

This project has been supported by Muğla Sıtkı Koçman University under Scientific Research Project no. 17/060.

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