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Selection of optimal numerical method for implementation of Lorenz Chaotic system on FPGA

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ABSTRACT

In this study, implementation of Lorenz chaotic system on Spartan 3e XC3S1600e FPGA development board by using Xilinx System Generator technology is presented. Differential equations of any nonlinear system have to be discretized before coding and design process on FPGA editor. The Lorenz chaotic system is discretized by using Taylor series expansion, Runge-Kutta and Euler discretization methods which are mostly preferred to discretize the continuous formed signals. The optimal numerical method based on application area is proposed by proving accuracy and complexity of methods and comparing designs in terms of resource utilizations on FPGA board.

1. Introduction

Chaos can be found in many engineering systems [1]. The main characteristic of chaotic system is that it is extremely sensitive to initial conditions and small difference in initial state can cause to extraordinary differences in the system behavior. Chaotic behaviors are complex, irregular and generally undesirable in mechanical systems. In many mechanical system applications require a control unit that minimizes complexity and eliminates undesired behaviors in order to improve performance of the system. However, chaotic behavior can be useful some areas where the complexity is required such as secure communication and cryptographic systems [2].

The dynamics of chaotic systems have attracted increasing attention of researchers in recent years. The Lorenz model [3] describes the motion of a fluid under the conditions of Rayleigh-Benard flow [4] and it has become a paradigm [5]. The system consists of many features of the chaotic dynamics but it is the simplest model for the dynamics of convective layers and close convection loops [6]. In literature, there are many publications related to Lorenz system and comparisons of it between other chaotic systems [7-10].

In the analysis of chaotic system, two representation types confront to us which are continuous time and discrete time modelling. In digital applications, discrete time modelling must be used in order to process the system behavior onto digital processors. For this purpose, there are many discretization methods in literature. When using a discretization method for a digital processing, it is definitely considered by user whether the design has desired accuracy and resource utilization or not. In this study, Taylor series expansion, Euler and Runge-Kutta discretization methods are used to represent differential equations of Lorenz chaotic system in discrete time domain. Selection of the optimal discretization method is important to have desired performance. In [11], Forward Euler (FE) and Runge-Kutta (RK) numerical integration methods are used for simulating the chaotic behavior of multi-scroll chaotic oscillator and results are compared.

In circuit realization studies, Field Programmable Gate Array (FPGA) technology is frequently preferred by designers based upon its high speed parallel processing and low cost area abilities. When FPGA is used for realization of mathematical equations, a fractional

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number representation format must be arranged to design mathematical model. There are two types of fractional number representation format which are fixed-point and floating-point, respectively.

In this study, differential equations of Lorenz system are discretized by using Taylor series expansion, Euler and Runge-Kutta numerical discretization methods in order to compare designs by the meaning of accuracy, complexity and resource utilizations on FPGA. After discretization process, discrete time models are designed on Spartan 3e XC3S1600e FPGA development board by using Xilinx System Generator (XSG) technology. In the design stage, fixed-point number representation format is used.

Herewith this introduction, the Lorenz chaotic system and three different discretization methods are expressed in Section 2. For each discretization methods, discrete mathematical models are defined. In Section 3, brief information about fixed-point number representation format and FPGA design by using XSG technology is given. Also, implementation results of three designs and comparison of discretization methods are illustrated in this section. At the end, final section concludes the paper.

2. The Lorenz System and Discretization Methods

2.1 The Lorenz System

The Lorenz system [3], named for Edward N. Lorenz is a famous example of nonlinear chaotic system. The system has 3-dimensional dynamical model that exhibits chaotic behaviors. The state equations of system are represented as follow;

$$\begin{aligned} \dot{x} &= \sigma \cdot (y - x) \\ \dot{y} &= r \cdot x - y - x \cdot z \\ \dot{z} &= x \cdot y - \beta \cdot z \end{aligned} \tag{1}$$

where σ, r and β are called control parameters and x, y, z are state variables of system. All σ, r, β>0, but usually σ=10, β=8/3 and r is varied. The system exhibits chaotic behavior for r=28 [12].

The system has many features of nonlinearity. MATLAB Simulink block diagram of the system is illustrated in Fig. 1 and simulation result for *x-y* phase plane portrait is given in Fig. 2.

The chaotic behavior can be quantitatively determined by obtaining maximum Lyapunov exponent (MLE) value [13, 14]. Regarding to simulation time series of the model, MLE values of state variables of the Lorenz system are λ_{1max} = 0.1359, λ_{2max} = 0.0828 and λ_{3max} = 0.0164. Since there are at least two positive MLE value, strong hyper chaotic behavior in the system is quantitatively demonstrated.

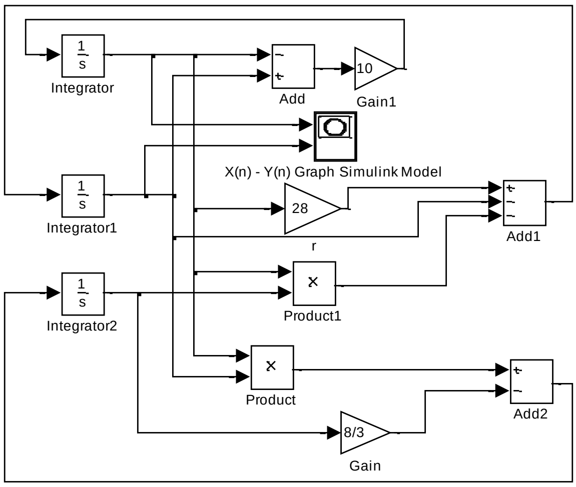

Figure 1. MATLAB Simulink block diagram of Lorenz system.

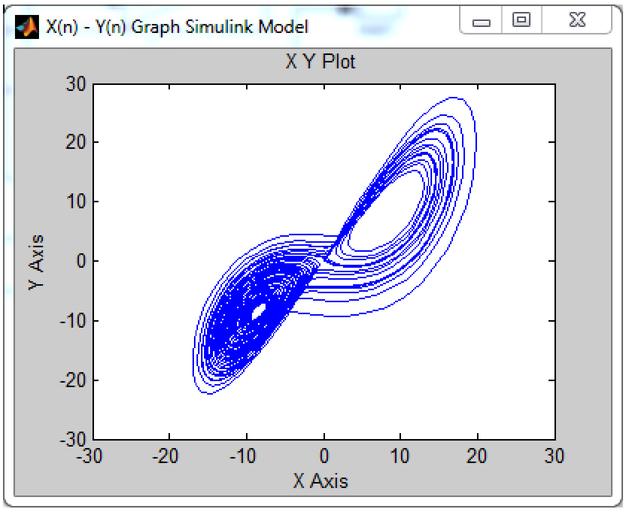

Figure 2. *x-y* chaotic phase plane portrait of the system.

2.2 Taylor Series Expansion Method

In order to program any system on a microprocessor, system model must be discretized. In Taylor series expansion numerical method, state variables of the Lorenz system are expanded for any m^{th} order as follow.

$$\begin{aligned} x(t+h) &= x(t) + \sum_{m=1}^{\infty} \frac{1}{m!} \cdot h^m \cdot x^{(m)} \\ y(t+h) &= y(t) + \sum_{m=1}^{\infty} \frac{1}{m!} \cdot h^m \cdot y^{(m)} \\ z(t+h) &= z(t) + \sum_{m=1}^{\infty} \frac{1}{m!} \cdot h^m \cdot z^{(m)} \end{aligned} \tag{2}$$

Bearing in mind that this study aims the comparison of numerical methods, Taylor series expansion method is executed for m=2 and h=0.001. In this situation, discrete time state equations of the Lorenz system with Taylor series expansion method is obtained as follow.

$$x[n+1]=x[n]+0,001\cdot\dot{x}[n]+\frac{1}{2}\cdot 0,001^2\cdot\ddot{x}[n]$$
$$y[n+1]=y[n]+0,001\cdot\dot{y}[n]+\frac{1}{2}\cdot 0,001^2\cdot\ddot{y}[n] \quad (3)$$
$$z[n+1]=z[n]+0,001\cdot\dot{z}[n]+\frac{1}{2}\cdot 0,001^2\cdot\ddot{z}[n]$$

$$\begin{aligned}
&\dot{x}[n]=\sigma\cdot(y[n]-x[n])\\
&\ddot{x}[n]=\sigma\cdot(r\cdot x[n]-y[n]-x[n]\cdot z[n])-10\cdot\sigma\cdot(y[n]-x[n])\\
&\dot{y}[n]=r\cdot x[n]-y[n]-x[n]\cdot z[n]\\
&\ddot{y}[n]=r\cdot\sigma\cdot(y[n]-x[n])-(r\cdot x[n]-y[n]-x[n]\cdot z[n])\\
&-\sigma\cdot(y[n]-x[n])\cdot(x[n]\cdot y[n]-\beta\cdot z[n])\\
&\dot{z}[n]=x[n]\cdot y[n]-\beta\cdot z[n]\\
&\ddot{z}[n]=\sigma\cdot(y[n]-x[n])\cdot(r\cdot x[n]-y[n]-x[n]\cdot z[n])\\
&-\beta\cdot(x[n]\cdot y[n]-\beta\cdot z[n])
\end{aligned} \quad (4)$$

2.3 Runge-Kutta Discretization Method

In literature, the most preferred Runge-Kutta method is 4[th] order method. Since this study aims to compare discretization methods, 2[nd] order Runge-Kutta method is preferred. 2[nd] order Runge-Kutta method is extended for an example in Eq. 5. State variables of the Lorenz system are executed with 2[nd] order Runge-Kutta method for *h*=0.001 and discrete time model of the system is represented as in Eq. 6.

$$\begin{aligned}
&\dot{x}(t)=\frac{dx(t)}{dt}=f\left(x(t),t\right)\\
&k_1=h\cdot f\left(x(t_0),t_0\right)\\
&x_1(t_0+\frac{h}{2})=x(t_0)+k_1\cdot\frac{h}{2}\\
&k_2=f\left(x_1(t_0+\frac{h}{2}),t_0+\frac{h}{2}\right)\\
&x(t_0+h)=x(t_0)+k_2\cdot h
\end{aligned} \quad (5)$$

$$\begin{aligned}
&k_{1x}=h\cdot\left(\sigma\cdot(y[n]-x[n])\right)\\
&k_{2x}=h\cdot\left(\sigma\cdot(y[n]-(x[n]+\frac{k_{1x}}{2}))\right)\\
&x[n+1]=x[n]+\frac{(k_{1x}+k_{2x})}{2}\\
&k_{1y}=h\cdot\left(r\cdot x[n]-y[n]-x[n]\cdot z[n]\right)\\
&k_{2y}=h\cdot\left(r\cdot x[n]-(y[n]+\frac{k_{1y}}{2})-x[n]\cdot z[n]\right)\\
&y[n+1]=y[n]+\frac{(k_{1y}+k_{2y})}{2}\\
&k_{1z}=h\cdot\left(x[n]\cdot y[n]-\beta\cdot z[n]\right)\\
&k_{2z}=h\cdot\left(x[n]\cdot y[n]-\beta\cdot(z[n]+\frac{k_{1z}}{2})\right)\\
&z[n+1]=z[n]+\frac{(k_{1z}+k_{2z})}{2}
\end{aligned} \quad (6)$$

2.4 Euler Discretization Method

Euler method can be arranged in two ways which are Forward and Backward Euler. In this study, Forward Euler (FE) method is preferred. The expression of FE method is given in Eq. 7 and discretized model is expressed in Eq. 8 for *h*=0.001.

$$\begin{aligned}
&\dot{x}(t)=\frac{x(t+h)-x(t)}{h}\\
&\dot{y}(t)=\frac{y(t+h)-y(t)}{h}\\
&\dot{z}(t)=\frac{z(t+h)-z(t)}{h}
\end{aligned} \quad (7)$$

$$\begin{aligned}
&x[n+1]=x[n]+h\cdot\sigma\cdot(y[n]-x[n])\\
&y[n+1]=y[n]+h\cdot\left(r\cdot x[n]-y[n]-x[n]\cdot z[n]\right)\\
&z[n+1]=z[n]+h\cdot\left(x[n]\cdot y[n]-\beta\cdot z[n]\right)
\end{aligned} \quad (8)$$

3. Implementation Stage

3.1 The Xilinx System Generator (XSG) Technology

The Xilinx System Generator is a high level MATLAB-Simulink based software platform that is used to create fast and easy designs on FPGA boards, execute Hardware Co-Simulation of design and implement real-time onboard applications [15]. XSG has libraries which consists of bit or loop based blocks inside MATLAB-Simulink for applications such as arithmetic, logical, memory and Digital Signal Processing (DSP). The only difference between XSG blocks and common Simulink blocks is that XSG blocks can be used in discrete-time domain with fixed-point number representation format.

3.2 Fixed-point Number Representation Format

In this study, 32-bit signed fractional numbers are used in arithmetic operations such as addition and multiplication process. In order to use in a design fractional numbers, there are two ways in literature that are floating-point and fixed-point number representation formats. In the design process of discrete time model equations, 2's complement 32-bit fixed-point number format is preferred. *Qm.n* is used for representing fixed-point number format where *m* indicates the number of bits that are arranged for integer part of number while *n* for fractional part. Therefore, the format is arranged as *Q16.16* and illustrated in Fig. 3. The resolution of the format is obtained as $2^{-n} = 2^{-16} = 1.5259$ e-5 [16].

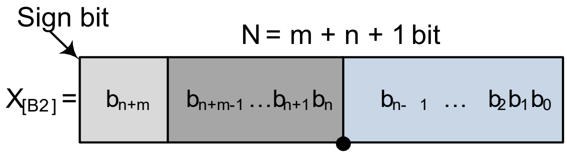

Figure 3. *Qm.n* fixed-point number representation format.

3.3 Implementation Results and Comparisons

In the implementation stage, discrete time models that are discretized by three numerical methods are designed on Spartan 3e XC3S1600e FPGA development board by using XSG platform with 32-bit signed 2's complement fixed-point number representation format in real-time. Change of *x* state variable for each one of three methods design and Simulink reference model is shown in Fig. 4.

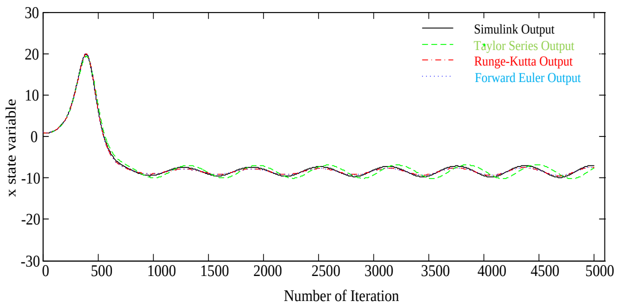

Figure 4. Change of each *x* state variable of designs.

In order to compare designs by meaning of accuracy and complexity, mean square error (MSE) and maximum Lyapunov exponent (MLE) values are determined. Table 1 represents MSE and MLE values of designs that are used to discretize the Lorenz system.

Table 1. Mean Square Error (MSE) and Maximum Lyapunov Exponent (MSE) values of designs.

Discretization Method	MSE	MLE		
		λ_{1max}	λ_{2max}	λ_{3max}
Taylor Series Expansion	0.6742	0.0295	0.0249	0.0021
Runge-Kutta	0.0884	0.0980	0.0075	0.0074
Forward Euler	0.0874	0.1103	0.0077	0.0086
Simulink Model	-	0.1359	0.0828	0.0164

In Taylor series expansion method, 2nd order expansion is executed. Therefore, the MSE value of this method is nearly eight times higher than the others. Considering results of Table 1, FE discretization method can be used with greater accuracy and complexity. Implementation results for *x-y* phase plane portrait of each one three methods are given in Fig. 5 (a), (b) and (c).

The screen views of three designs with discretization methods on XSG platform are illustrated in Fig.6, 7 and 8. Table 2 and 3 represent number of arithmetic circuits, XSG blocks and resource utilization on FPGA for each discretization method.

Table 2. Number of used arithmetic circuits and XSG blocks

Arithmetic circuits and XSG blocks	Taylor Series	Runge-Kutta	Forward Euler
Addition	6	9	3
Subtraction	8	6	1
Multiplication	18	16	8
Register	3	3	3
Constant	15	15	7

Table 3. Resource utilizations on FPGA for each method.

FPGA resources	Taylor Series	Runge-Kutta	Forward Euler
Used Logic Slices	2146	1856	888
Used Flip-Flops	3225	2624	1360
Used LUTs	3719	3248	1496
IOBs	96	96	96
Mults/DSP48s	78	64	32

As seen in Table 2 and 3, FE method uses almost half of both XSG blocks and FPGA resources that RK and Taylor series methods use.

4. Conclusions

As a result of this study, it is clearly understood that Forward Euler discretization method has the best performance for discretization of the Lorenz chaotic system. However, Runge-Kutta method has better accuracy and uses less resource on FPGA than Taylor series. Also, in the implementation stage Taylor series expansion method is executed for 2nd order. If the order of expansion is increased, accuracy of Taylor series expansion method can get better while MSE value decreases. On the other hand, resource utilization of higher order Taylor series expansion method increases.

As a future work, the Lorenz chaotic system circuitry will be installed on board. The similar work will be processed on board by using basic circuit elements and signal converters as digital to analog and vice versa.

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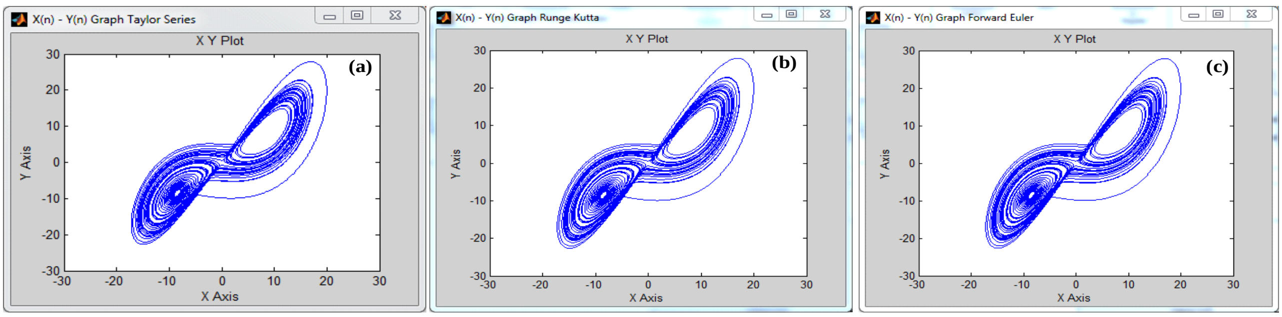

Figure 5. *x-y* chaotic phase plane portrait for the design with a) Taylor series expansion, b) Runge-Kutta and c) Forward Euler.

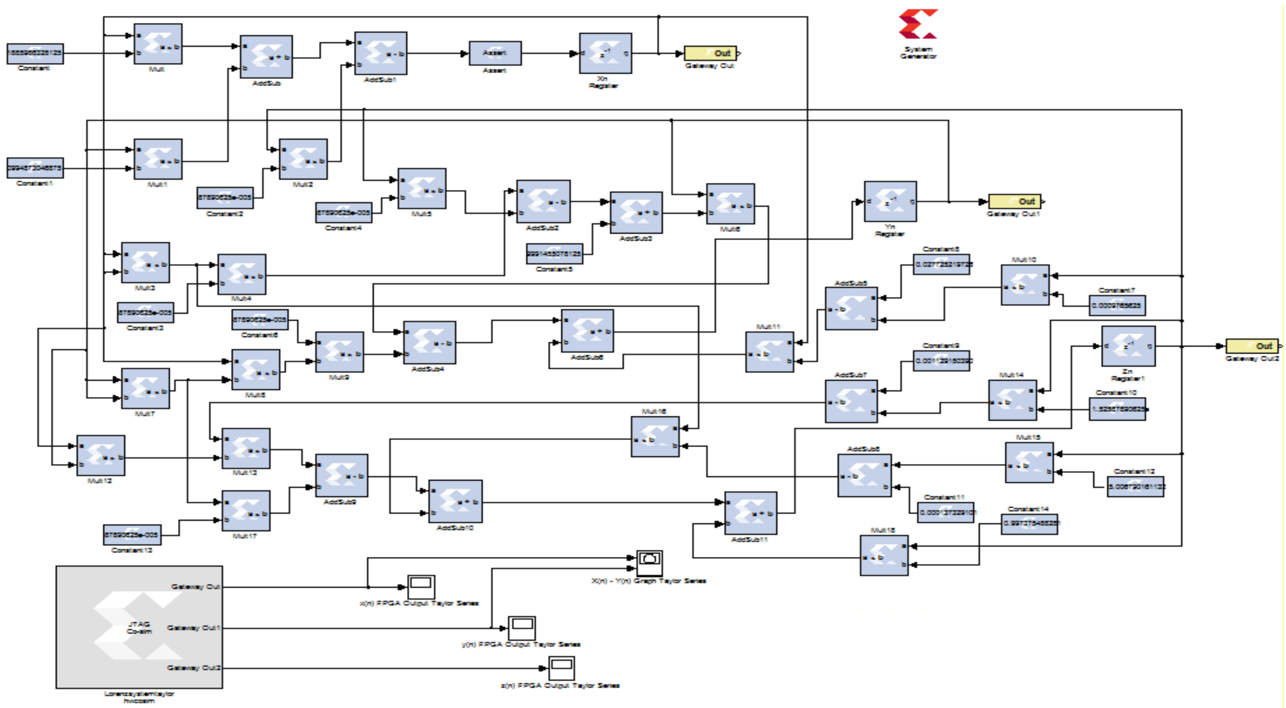

Figure 6. Implementation view of Lorenz system with Taylor series expansion method on XSG platform.

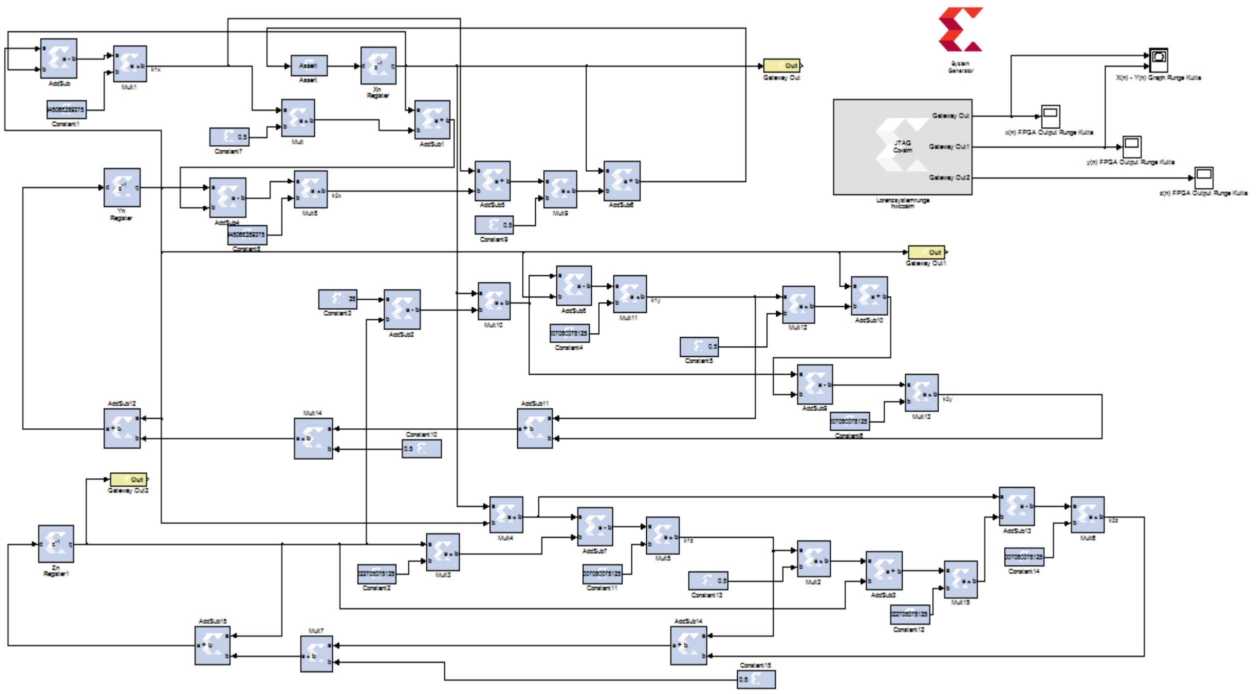

Figure 7. Implementation view of Lorenz system with Runge-Kutta discretization method on XSG platform.

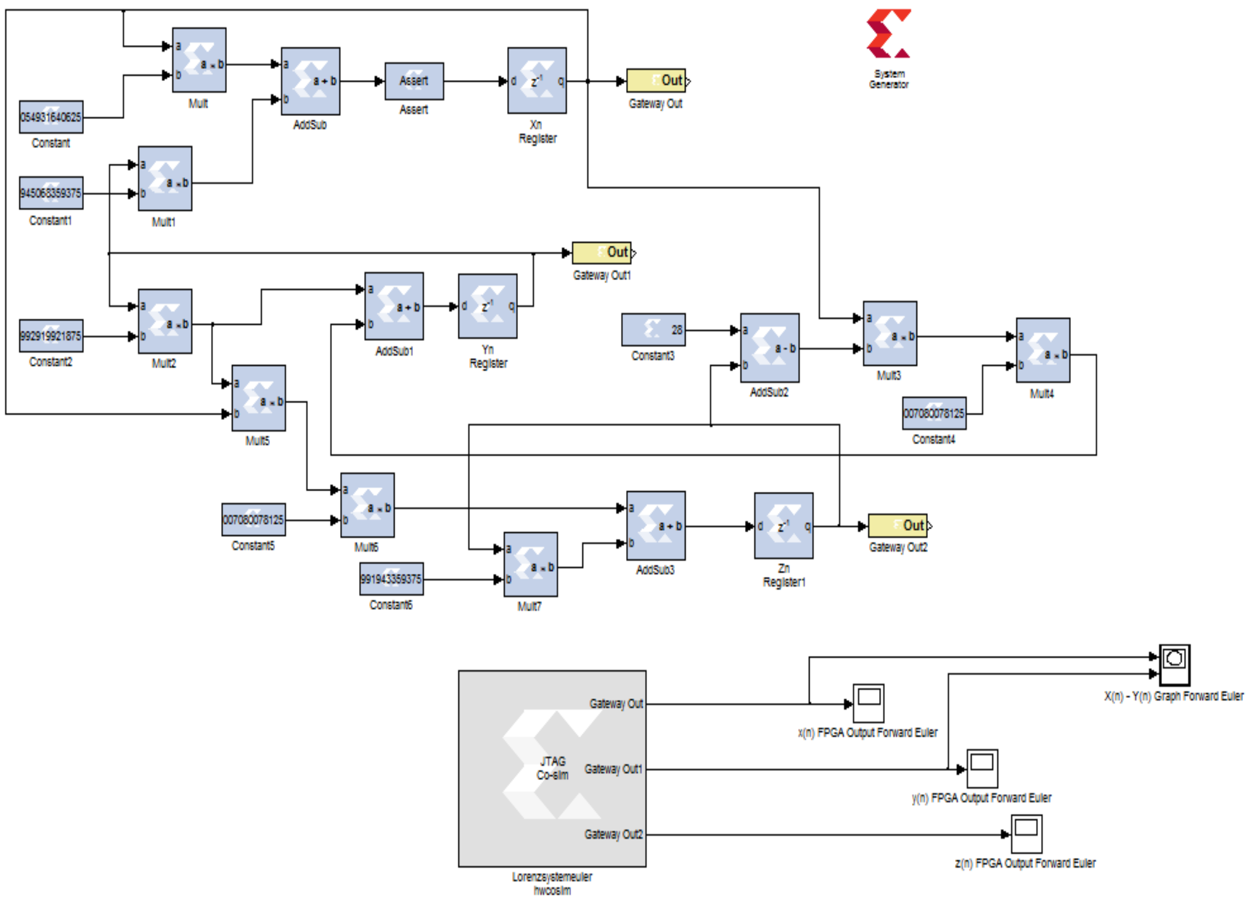

Figure 8. Implementation view of Lorenz system with Forward Euler discretization method on XSG platform.