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Dielectric Characterization of Si-Based Heterojunction with TiO_2 Interfacial Layer

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ÖZET: In this study, Al/TiO_2/*p*-Si/Al heterojunction is fabricated and investigated some electrical and dielectric characteristics. Atomic layer deposition technique was used for synthesize of TiO_2 interfacial layer due to the some advantages such as uniformity and stability of surface. For determining electrical and dielectric characteristics, impedance spectroscopy measurements were performed in range from -1 to +1 V bias voltages and 10 kHz-1MHz frequency range at room temperature. As an electrical parameters, interface states distribution and series resistance values was determined. In addition to these, it is found that the dielectric properties such as dielectric loss and constant, real and imaginary parts of electric modulus, loss tangent and AC electric conductivity values was depended on frequency and voltage strongly. The electrical and dielectric characteristics show that interface states and polarization values of fabricated device can follow AC signal at low frequency values.

Anahtar Kelimeler: Dielectric properties, TiO_2, MIS structure, atomic layer deposition (ALD).

TiO_2 Ara Katmanlı Si-Tabanlı Heteroeklemin Dielektrik Karakterizasyonu

ABSTRACT: Bu çalışmada, Al/TiO_2/*p*-Si/Al heteroeklemi üretildi ve bazı elektrik ve dielektrik karakteristikleri araştırıldı. TiO_2 arayüzey katmanının sentezlenmesi için yüzey düzgünlüğü ve kararlılığı gibi sahip olduğu bazı avantajlardan dolayı atomik katman kaplama tekniği kullanıldı. Elektriksel ve dielektrik karakteristiklerinin belirlenmesi için, oda sıcaklığında, -1 ile +1 V beslem voltajı ve 10 kHz-1MHz frekans değerleri aralıklarında empedans spektroskopisi ölçümleri yapılmıştır. Elektriksel parametreler olarak arayüzey halleri dağılımı ve seri direnç değerleri belirlenmiştir. Bunlara ek olarak, dielektrik kaybı ve katsayısı, elektriksel modülün gerçek ve imajiner kısmı ve AC elektrik iletkenliği gibi dielektrik parametrelerin frekansa ve voltaja güçlü bir şekilde bağlı olduğu bulunmuştur. Elektrik ve dilelektrik karakteristikler üretilen aygıtın arayüzey halleri ve polarizasyon değerlerinin düşük frekanslarda AC sinyalini takip edebildiğini göstermektedir.

Keywords: Dielektrik özellikler, TiO_2, MIS yapı, atomik katman kaplama (ALD).

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INTRODUCTION

In the electronic circuits, transition metal oxide thin films Al_2O_3, ZrO_2, TiO_2, HfO_2 and their compounds have been recently used for Complementary Metal Oxide Semiconductor (CMOS) devices (Turut et al., 2017; Gupta et al., 2017; Sekhar et al., 2017; Karabulut et al., 2018). Although they are extensively considered as an alternative of the SiO_2 gate, the usage of these films may result in several problems: poor interface quality before integrating into the devices, a large number of oxide trapped charges and thermal stability (Ye et al., 2003; Raeissi et al., 2008; Long et al., 2012). Once the popularity of these alternative films in industry, TiO_2 thin films attract the attention due to its prevalent applications related to photonic crystals, memory devices, solar cells and microelectronics (Ge et al., 2017; Sakthivel et al., 2017; Kalygina et al., 2017). TiO_2 is an n-type semiconductor, which has a refractive index of about 2.6 and has excellent stability with Si. Also, its dielectric constant ranges from 16 to 100 while its wide band gap is around 3.5 eV (Gyanan et al., 2016). In addition to these favored properties of titanium dioxide for electronic industry, it is extensively evaluated due to its properties such as chemical stability and non-toxicity (Dang et al., 2014). On the other hand, the preparation method of TiO_2 thin films is important since the procedure may affect the structural and electrical properties of the film. There are various techniques for synthesizing materials as interfacial layer using to electronic devices. In present work, ALD technique was used for obtaining of TiO_2. Because ALD has a very important advantages such as surface homogeneity, uniformity, suitable for large-scale study, self- limiting property during the surface reactions and certain control of thickness. Besides these advantages, low temperature applications are very important for material synthesis. Because it has lower cost than high temperature processes for synthesizing materials. The ALD technique is very suitable for low temperature applications (Karabulut et al., 2018).

In the previous work, we investigated the photovoltaic properties of the Al/TiO_2/p-Si/Al photodiode, and found that this structure exhibits high photosensitive behavior (Karabulut et al., 2018). In present study, we discussed the dielectric properties of this photodiode. Dielectric materials help to adjust flow of the electric charges between the semiconductor and metal as much as to understand conduction and polarization mechanism of metal-semiconductor devices. These dielectric materials can be affected by frequency and voltage (Orak et al., 2017). One of the most important parameter here is frequency due to electrical effect for integrated circuits. This study is aimed to study frequency-dependent dielectric properties of Al/TiO_2/*p*-Si device. Beside, further study is conducted to expand the knowledge on conduction and polarization mechanism of the TiO_2/*p*-Si device. To reach these goals, following quantities in the TiO_2/*p*-Si device are examined at room temperature using different frequencies: ac electric conductivity (σ), imaginary and real parts of electric modulus (M' and M''), loss tangent (*tan* δ), dielectric loss (ε'') and dielectric constant (ε').

MATERIALS AND METHODS

The silicon-based device with TiO_2 interfacial layer was fabricated by using *p*-type Si semiconductor substrate which has (111) surface orientation, 1-10 Ω-cm resistivity and thickness of 525±25 mm. For removing inorganic and organic contaminations on surface of substrate, it was submerged in acetone and propanol for 5 minutes, respectively. After this stage, contaminants-removed substrate was rinsed with deiyonized water and dried under N_2 gas flow. After cleaning process, high purity aluminum metal (Al) was evaporated to back side of Si semiconductor for made of ohmic contact at 6 x 10^{-6} Torr pressure, and thickness of ohmic metal contact was about 500 angstrom. After evaporation, it was annealed at 500 ^{0}C for 3 minutes under N_2 atmosphere. The polished surface of the prepared sample was coated with TiO_2 material for use as an interfacial layer. The atomic layer deposition technique was used for the coating process. The covered TiO_2 material was synthesized by the use of Savannah 100 thermal ALD reactor (Ultratech/ Cambridge Nanotech Inc.) at 150 ^{0}C substrate temperature, and used tetrakis(dimethylamino) titanium [$Ti(NMe_2)_4$] and H_2O as a precursors for titanium and oxygen, respectively. During the coating period, the times of staying in the coating unit of titanium and oxygen are 0.1 and 0.15 seconds, respectively. There is a purging step of 20 sec at each interval. The growth rate of coated TiO_2 film was approximately 0,4 angstrom per cycle for this recipe,

and total thickness of film was approximately 10 nm. After preparing interfacial layer, Al metals were evaporated on film for rectifying contact by the use of thermal evaporation technique with shadow mask, and the contact are were 1mm diameter and circular. After the fabrication process, the *C–V* and *G/w–V* measurements of Al/TiO_2/*p*-Si heterojunction were realized by using HP 4192A LF Impedance Analyzer at the dark and room temperature.

RESULTS AND DISCUSSION

Investigating of density of interface states (D_{it}) and series resistance (R_s) parameters is a very important place for determining device behavior. Because electrical characteristics are strongly influenced this parameters (Cherif et al., 2013). Relation of between D_{it} and voltage is determined for TiO_2/p–Si heterojunction by the use of Hill–Coleman technique, which is following equation (Gozeh et al., 2018);

$$D_{it} = \frac{2}{qA} \frac{\left(G_m/w\right)_{max}}{[(G_m/w)_{max}/C_{ox}]^2 + (1 - C_m/C_i)^2} \quad (1)$$

This technique is also given correlation of D_{it} and frequency. In equation, q is the electronic charge, *w* is the angular frequency which is equal to $2\pi f$, A is the contact area, C_m is maximum value of capacitance, $(G_m/w)_{max}$ is the measured value of conductance and C_i is the insulator layer capacitance, which is placed between semiconductor and metal layer, calculated from following equation at strong accumulation region (Yücedag et al., 2014);

$$C_i = C_{ma}\left[1 + \frac{G_{ma}^2}{(wC_{ma})^2}\right] \quad (2)$$

Series resistance (R_s) is one of the important sources of small energy loss in devices such as metal-semiconductor (MS), metal-insulator-semiconductor (MIS), photodetectors and solar cells. R_s may arise from various situations such as the quasi-neutral bulk resistance of semiconductor, the back ohmic contact of the semiconductor, the electrical interaction made of the probe wire to rectifier contact, impurities in films or contaminations of back contact and pedestal and non-uniformly doped atoms distribution in the semiconductor (Zeyrek et al., 2013; Bıyıklı et al., 2014).

The frequency and voltage dependent series resistance can also be specified for each frequency using measured capacitance and conductance values (C_{ma} and G_{ma}); however, the real value, which corresponds to the strong accumulation region at adequate high frequency of larger than 500 kHz, can be calculated using Nicollian and Brews equation (Nicollian and Brews, 2003):

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (wC_{ma})^2} \quad (3)$$

Fig. 1 shows the R_s profiles versus voltage plots for different frequencies. This figure highlights that R_s values do not vary in the accumulation and inversion regions although peaks are observed in depletion region at almost all considered frequencies. R_s values in accumulation region (high frequencies and forward bias

voltages) are approximately independent of voltage. Another remark should be underlined here is that peak intensities decrease by the increase of the frequency from 10 kHz to 1 MHz. This fact is observed here since interface states come in possession of effective at low frequencies. The peak positions in depletion region change to forward bias with increasing frequency due to a special density distribution of D_{it} at TiO_2/p-Si and reorganize and their rearrangement within electric field boundaries (Selçuk et al., 2014; Sze , 1981; Rhoderick and Williams, 1988).

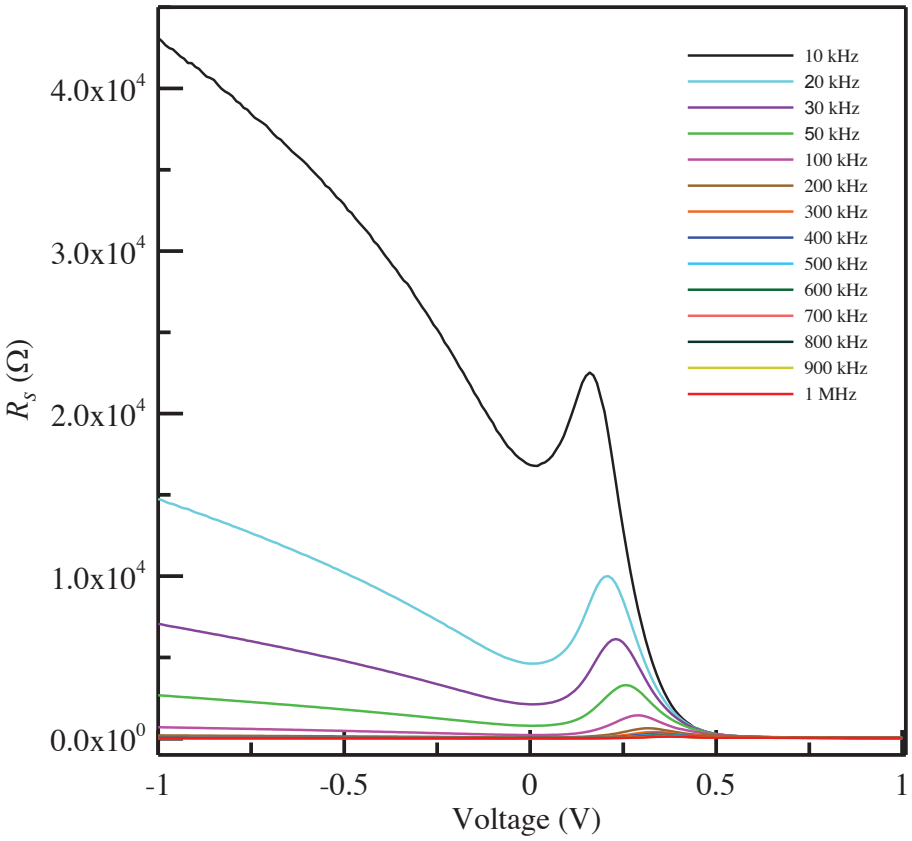

Figure 1. Series resistance versus voltage graph of Al/TiO_2/p-Si/Al heterojunction for various frequencies.

The calculated D_{it} and R_s parameters by using Equations 1 and 3 were plotted versus frequency and given in Figure 2. These values were obtained from capacitance and conductance measurements of mentioned device. As seen in figure, both of D_{it} and R_s values decrease up to 100 kHz, and after this point R_s values increase with increasing frequency while D_{it} values almost remain constant. The reason for behaviors of these parameters at low frequencies can be attributed to ability of follow AC signal.

But, the cause of alterations of these values with increasing frequency is attributed to the existence of traps in deep level (Turut et al., 2015; Turut et al., 2015). It is also apparent in given figure that the series resistance is strongly dependent to the frequency.

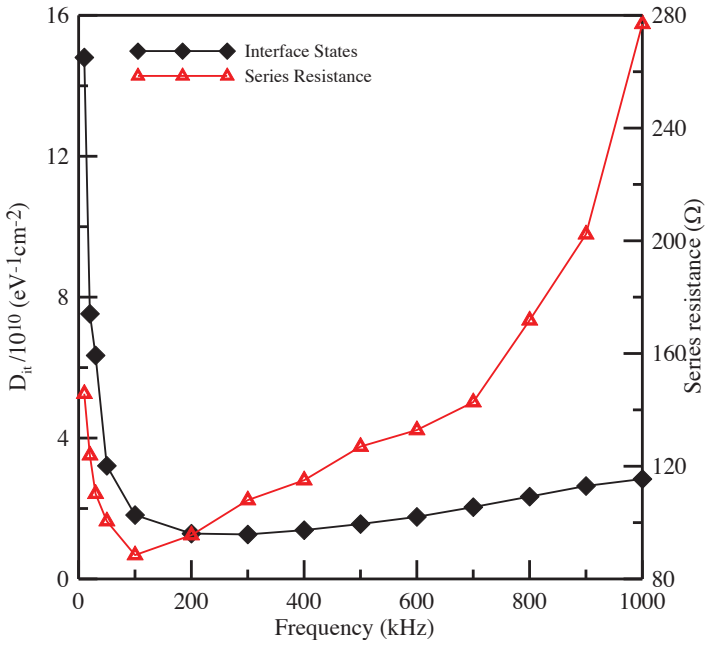

Figure 2. Graphs of interface state (D_{it}) and series resistance (Rs) versus frequency of Al/TiO_2/p–Si heterojunction

The mentioned quantities are calculated to investigate the voltage and frequency dependent dielectric properties of Al/TiO_2/p-Si heterojunction with help of *G-V* and *C-V* measurements that were given our previous work (Karabulut et al., 2018). Following equation can expressed the complex permittivity (Tataroğlu et al., 2008):

$$\varepsilon^* = \varepsilon' - j\varepsilon'' = \frac{C}{C_0} - j\frac{G}{wC_0} \tag{4}$$

where C, C_0, G, j, and represent the measured capacitance, the capacitance of the free capacitor, the measured conductance, imaginary root, real and imaginary parts of complex permittivity (ε^*), respectively. Here, defines the stored energy of device with applied voltage and presents the dipoles strength and gives the energy consumption for the dielectric materials (Karatas and Kara, 2011). and can be calculated as follows:

$$\varepsilon' = \frac{C}{C_0} = \frac{Cd_i}{\varepsilon_0 A} \tag{5}$$

and,

$$\varepsilon'' = \frac{G}{wC_0} = \frac{Gd_i}{w\varepsilon_0 A} \tag{6}$$

In equation above; A, ε_0 and d_i stand for contact area, permittivity of vacuum and interfacial layer thicknesses, respectively. Frequency dependent dielectric constant versus voltage graph is shown in Figure 3. As seen in Figure, dielectric constant increased with increasing frequency over 0.15 V. In addition, it is constant up to approximately 0.15 volt. Moreover, two peaks, one of which is small, which are related to accumulation and

depletion regions at low frequency values can be seen from figure 4. But, there is only one peak observed at high frequency values.

First peak is attributed to the density distribution of interface states and second one is due to the existence of interfacial layer and series resistance (Orak et al., 2017). The dielectric constant value began to fall above approximately 0.45 volts and the dielectric constant values at the high voltage occurred in the negative region. This is because the capacitance value and the dielectric constant value are directly proportional to each other. In the work we have done before, the capacitance values are found to be in the negative region at high voltages. It is thought that the cause of this situation is the inductive effect (Aydin et al., 2014). In other words, the presence of negative capacitance behavior in the high voltage region may be attributed to an inductive contribution to the impedance caused by the injection of minority carriers into the semiconductor. It is therefore seen that the dielectric constant is also in the negative region(Peko et al., 1997; Arslan et al., 2010).

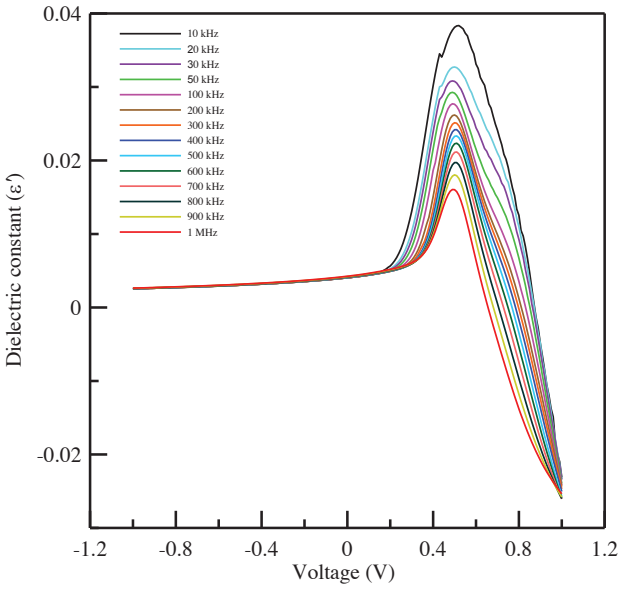

Figure 3. Graphs of dielectric constant () versus voltage of Al/TiO_2/*p*–Si heterojunction

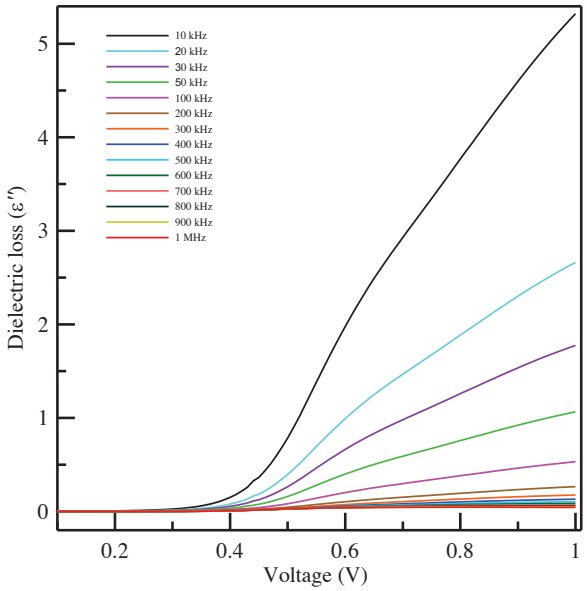

Figure 4. Plots of dielectric loss () versus voltage of Al/TiO_2/*p*–Si heterojunction

Figure 4 exhibits the dielectric loss versus voltage plots of fabricated structure. As can be seen from Figure 3 and 4, the and values are strongly dependent on voltage and frequency at high voltage. But, at low voltage values, which is inversion region, mentioned values remain approximately constant. The value decreases with increasing frequency such as . These behavior of dielectric constant and loss versus voltage are attributed to their inability to follow the AC signal at high frequency values. Because there is not enough time to change the direction of the AC signal (Kocyigit et al., 2018). To put it another way, the low values of the and are due to the presence of polarization and surface states.

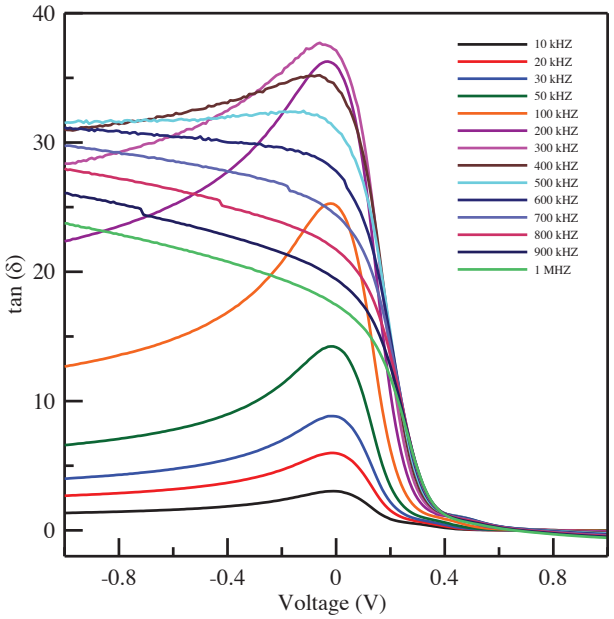

Figure 5. Loss tangent (δ) versus voltage plots of Al/TiO_2/*p*–Si heterojunction

Figure 5 shows the loss tangent (δ) versus voltage graph of Al/TiO_2/*p*-Si/Al heterojunction. As seen in this figure, in the case of forward bias region there is almost no change. However, δ values increase with increasing frequency values up to 300 kHz, after this point of frequency value they decrease till to 1-MHz frequency. As seen in Figure 5, some abnormal behaviors are observed in tanδ-*V* graph depending on the values of and. The observed peak values first increased and then decreased.

This change in the peak may be due to the rearrangement and restructuring of D_{it} in the externally applied DC electric current conditions. In addition, the capacitance and conductance values of fabricated devices are affected very sensitively by the series resistance and the interface quality of the device (Tecimer et al., 2014; Padma et al., 2013; Zeyrek et al., 2013).

The obtained results of tanδ-*V* graph shows that D_{it} and polarizations are effective in the applied bias conditions. In the literature, many researchers have found similar results and have attributed peak behavior just like this to the existence of interface states (Yücedağ et al., 2014).

To obtain real and imaginary electric modulus, the complex permittivity (ε*=1/*M**) is converted to the complex electric modulus (*M** =M'+jM'') form using following statement (Demirezen, 2013):

$$M^* = \frac{1}{\varepsilon^*} = \frac{\varepsilon'}{(\varepsilon')^2 + (\varepsilon'')^2} + j\frac{\varepsilon''}{(\varepsilon')^2 + (\varepsilon'')^2} = M' + jM'' \quad (7)$$

Figure 6 shows that values increases by the increase of frequency in depletion and inversion regions while it is not changed by frequency especially in the accumulation region. It is illustrated in Figure 7 that there are peaks on –V and these peak positions shift towards the accumulation region by the increase of frequency. These outcomes could be based on to the particular charges distribution in the surface states and relaxation times of charges (Kaya et al., 2016; Yang et al., 2015). It is found that and parameters of the fabricated heterojunction are depend on voltage and frequency strongly.

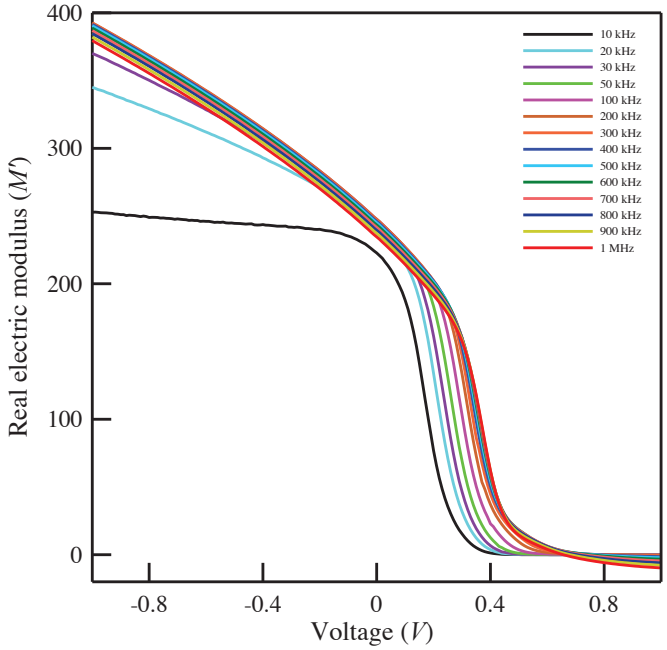

Figure 6. Real electric modulus versus voltage plots of Al/TiO_2/*p*–Si heterojunction

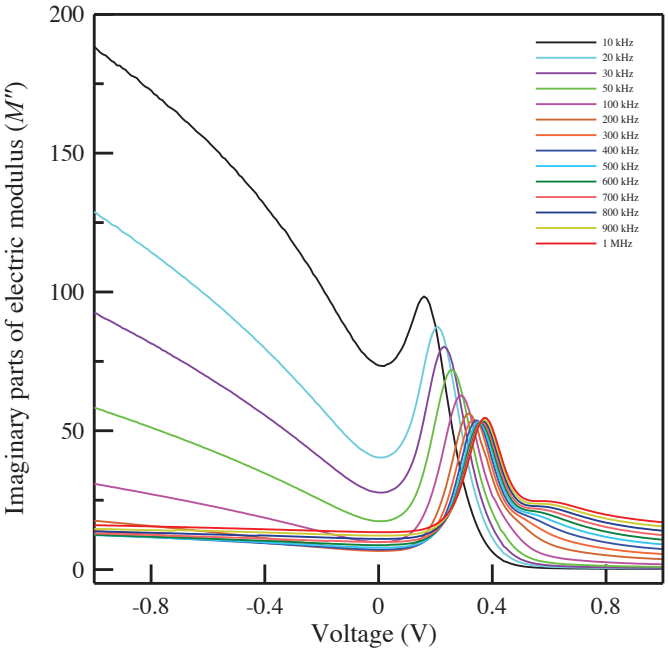

Figure 7. The imaginary parts of electric modulus versus voltage plots of Al/TiO_2/*p*–Si heterojunction

The AC electric conductivity (σ) value of fabricated Al/TiO_2/*p*-Si/Al heterojunction by the use of atomic layer deposition technique is obtained from the following formula (Kaya, 2015);

$$\sigma = \left(\frac{d}{A}\right)\omega C tan\delta = \varepsilon_0 \varepsilon'' \omega \quad (8)$$

The graph of the changing electrical conductivity (σ) with change of voltage for different frequency values is shown in Figure 8. As can be seen in figure, the AC electrical conductivity values are bent at high voltage region and the values of σ increase with increasing frequency up to bending region which is approximately after 0.7 volt. In addition to these, the AC electrical conductivity values decrease with increasing frequency after bending. It is observed that the progressive increase in σ_{ac} versus voltage graph with increasing applied bias voltage. This increase in σ_{ac} causes the eddy current to increase. This leads to an increase in energy loss due to the decrease in the series resistance value. Some researcher have fabricated Si-based structure with TiW-Pd2Si interfacial layer and obtained similar results. They reported the increase in σ_{ac} with increasing frequency by the progressive decrease in Rs (Afendiyeva et al., 2008).

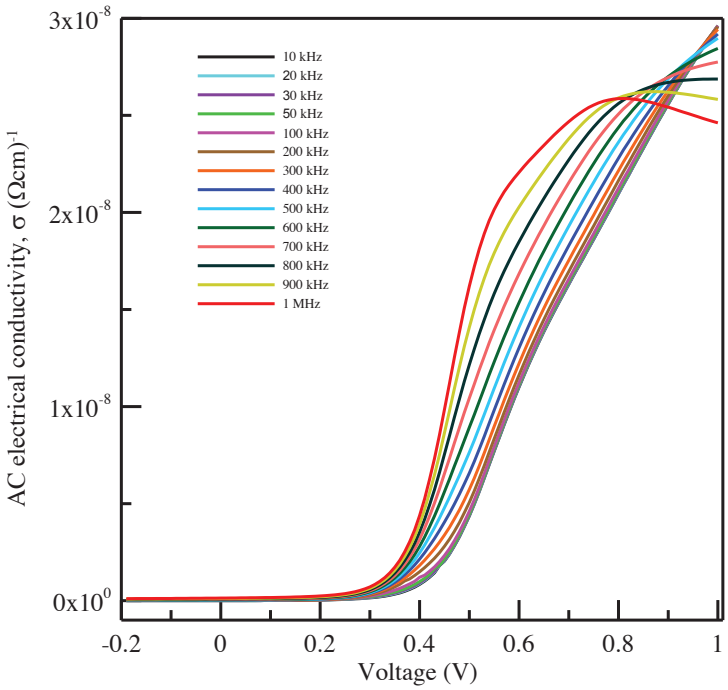

Figure 8. AC electric conductivity (σ) versus voltage plots of Al/TiO_2/*p*–Si heterojunction for different frequency values

CONCLUSION

The effects of interface states and series resistances on the electric and dielectric characteristics of Al/TiO_2/p–Si heterojunction are investigated by the use of frequency dependent capacitance-voltage and conductance-voltage measurements in the 10 kHz-1 MHz frequency range. The interface layer of the device was synthesized using the atomic layer deposition technique due to the advantages it has. The interface states and series resistance values of fabricated device were determined by varying frequency, and both of D_{it} and R_s values decrease up to 100 kHz, and after this point R_s values increase with increasing frequency while D_{it} values almost remain constant. According to present study, all dielectric parameters of the Al/TiO_2/p-Si/Al heterojunction, such as dielectric constant

and loss, real and imaginary parts of electric modulus, loss tangent and AC electric conductivity depend on the changing voltage and frequency strongly. It is observed that the and values of device increase with decreasing frequency values.

Besides these, tanδ reaches maximum value up to 300 kHz frequency then decreases till to 1 MHz. values increase with increasing frequency. In addition, there are curve points at particular voltage values in versus voltage graph. And these peaks shift towards to the forward bias region with increasing frequency. The σ values increases with increasing frequency and voltage up to almost 0.7 volt due to reduction of series resistance and polarization, and then they bend due to the presence of interface states. Last of all, it can be deduced that interface states and polarization of fabricated device can follow AC signal at low frequency values.

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