Virtual Group Control Algorithm for Modular Multilevel Converter

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Abstract- This paper deals with the group control method of MMC (Modular Multilevel Converter) HVDC system. The proposed scheme increases the number of SMs (Submodules) of MMC HVDC system to more than 500 (2GW class) without changing the sampling time. This method is called Cluster Stream Buffer (CSB) method, and the total SMs are divided into several clusters, and a cluster is composed of 32 SMs. It is easy for the Cluster Stream Buffer method to expand HVDC system to several GW Class and it is easy to keeping the system performances. Consequently, this method was validated using MATAB/Simulink program.

Keywords MMC HVDC(Modular Multilevel Converter HVDC), CSB(Cluster Stream Buffer;Level Selection Method), NLC(Nearsst Level Control), SM(Submodule).

1. Introduction

Recently, the installation of HVDC system is increasing due to the energy transit policy and the expansion of renewable energy around the world. Until now, HVDC system have been mainly composed of LCC (Line Commuted Converters) HVDC, but VSC (Voltage Source Converters) HVDC is mainly installed in the last 10 years, and 150[GW] is planned by 2030.

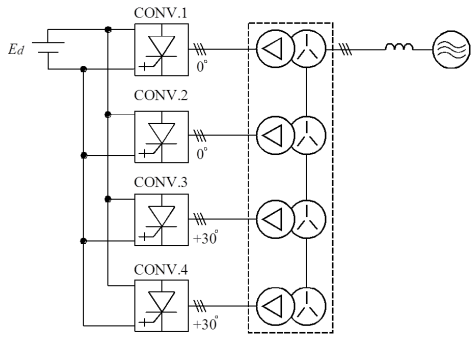
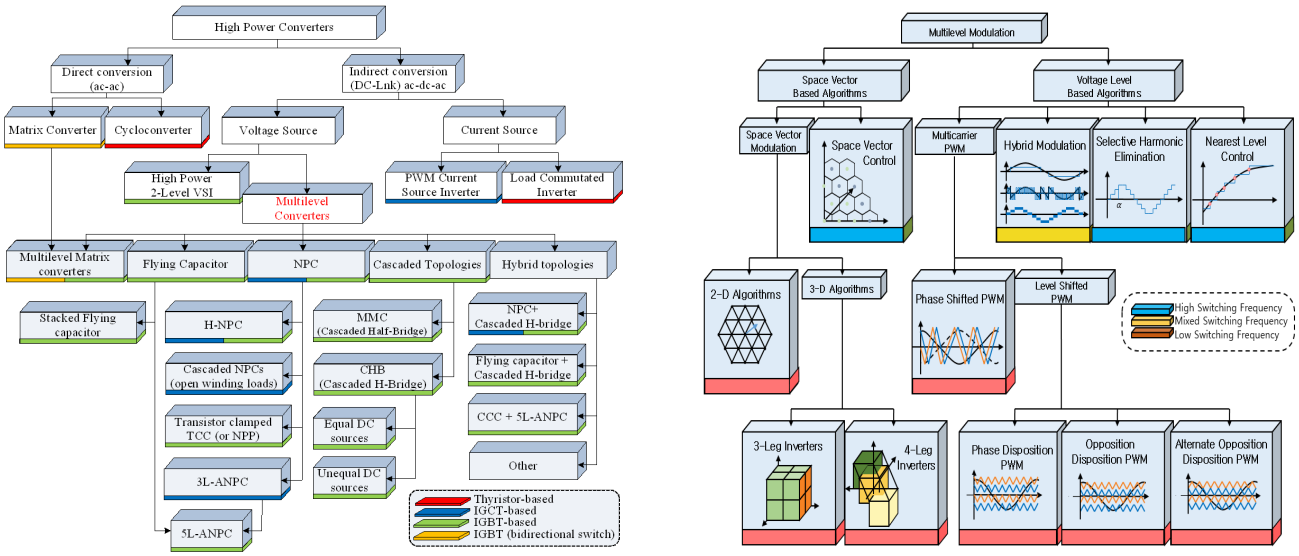


Fig. 1. High power converter topology with phase shift transformer

Since LCC HVDC system is highly dependent on AC system, it causes overvoltage, harmonic instability, and the resonance between AC system and HVDC system, while VSC HVDC system is independent of the AC system.

VSC HVDC system have several problems, that is it is difficult to make high power conversion equipment due to the limitation of the device, and the switching loss is too high because the PWM method is used. To solve these problems, a phase shift transformer is used as shown in Fig. 1, and MMC topologies are developed as shown in Fig. 2.

Fig. 2 shows the classification of the MMC topologies (Fig. 2 (a)) and switching algorithm (Fig. 2 (b)). In the VSC HVDC system, MMC and NLC (Nearest Level Control) are used as basic standards because it is excellent in all respects. The MMC topology proposed by R. Marquardt has the many advantages, high power capacity possibility and low harmonics and so on [1], [2].



(a) Technical classification for high power converter (b) Switching topology of modular multilevel converter

Fig. 2. Classification of high power converter and switching topology of MMC

In addition, since the MMC method is that IGBT is connected in series, it requires an electrical bypass switch (thyristor) and mechanical bypass switch (PMA type (Permanent Magnetic Actuator), pyromatic type).

The NLC (Nearest Level Control) method has been proposed to reduce switching loss within 1[%]. It is the simple and suitable for the NLC method to implement high of levels in the MMC HVDC system [3], [4].

As shown in Fig.3., ABB uses the method grouping submodules in hardware, this method controls a group module as SMs which is connected in series to compose a group module. This method is caused high-frequency harmonics and the unbalance between the IGBT devices, it is required snubber circuit to reduce the $\frac{di}{dt}$ and $\frac{dv}{dt}$.

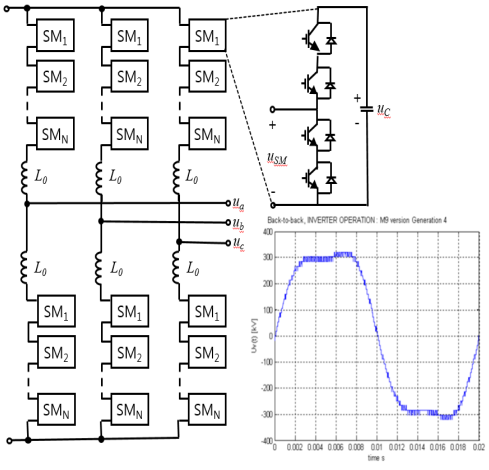


Fig. 3. Series connected module group control method (ABB's method)

One of the main issues in the MMC HVDC system is to increase the capacity to 1~2[GW] with the currently developed IGBT (Max. 3.3[kV], 1,500[A]), as the DC voltage is 500[kV] and 500 IGBTs of SM are connected in series. It is required high performance of the controller hardware and high speed of the sampling time and high speed of the communication to turn on/off IGBTs in real time.

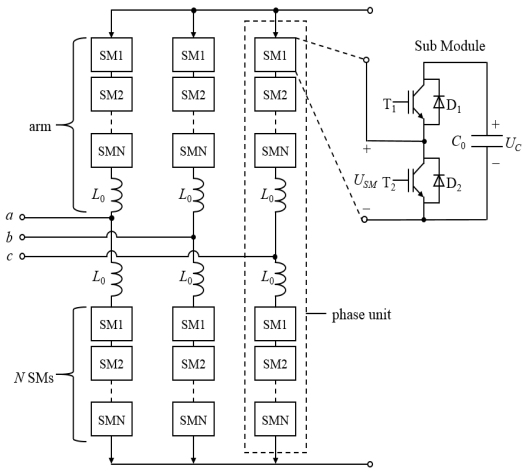
In this paper, CSB (Cluster Stream Buffer) method is proposed, which is consist of 32 levels as a cluster and can overlap the clusters in series [5]. The CSB method can be increased over 1 [GW] without changing the sampling time.

First, the basic characteristics of MMC is introduced and review the NLC method. On this base, the algorithm of the CSB method using fixed sampling time is dealt with and the feasibility on the proposed method is simulated by MATLAB /Simulink program.

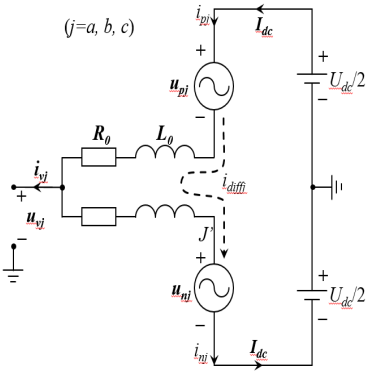
2. Basic Structure and Operation Principle of MMC

2.1. Basic structure

Fig. 4 (a) shows the basic structure of the MMC system. A three-phase MMC system is divided into six arms, and each arm contains N SMs and one inductor L_0. The upper and lower arm with in a single leg of MMC system comprise a phase unit. A half bridge SM circuit is shown on the right side of Fig. 4. The SM voltage, v_{SM}, is determined by the switching states of the upper and lower IGBTs. SM voltage becomes the capacitor voltage, v_c. Whereas, if the upper and lower IGBTs are turn-off and turn-on respectively, the SM voltage become zero. This means a SM has two normal operation states: inserted ($v_{SM} = v_c$) or bypassed ($v_{SM} = 0$).



(a) Basic structure of MMC



(b) Single-phase equivalent circuit of MMC

Fig. 4. MMC topology

A. Operational Principle

An equivalent single phase MMC system is shown in Fig. 4 (b). In Fig. 4 (b), the arm inductor and resistors are represented by L_0 and R_0, respectively. The total dc bus voltage is U_{dc}, the converter voltage of phase j is represented by u_{js} $(j = a, b, c)$. The line current of the each phase is denoted by i_{js} $(j = a, b, c)$. The arm voltages generated by series of the SMs express as u_{ju} and u_{jl} $(j = a, b, c, u: upper, l: lower)$.

The arm currents i_{ju} and i_{jl} in Fig. 4 can be expressed by (1) and (2).

$$i_{ju} = i_{jo} + \frac{i_{js}}{2} \quad (1)$$

$$i_{jl} = i_{jo} - \frac{i_{js}}{2} \quad (2)$$

where i_{jo} is the inner difference current of phase j, which flow through both the upper and lower arms.

And is given by:

$$i_{jo} = \frac{i_{ju}+i_{jl}}{2} \quad (3)$$

According to [6], the MMC HVDC system can be expressed by the following equations:

$$u_{js} = e_j - \frac{R_0}{2} i_{js} - \frac{L_0}{2} \cdot \frac{di_{js}}{dt} \quad (4)$$

$$L_0 \frac{di_{jo}}{dt} + R_0 i_{jo} = \frac{U_{dc}}{2} - \frac{u_{ju}+u_{jl}}{2} \quad (5)$$

where e_j in (4) is the inner EMF in phase j and is expressed as:

$$e_j = \frac{u_{jl}-u_{ju}}{2} \quad (6)$$

From the relation in (4), considering the ac grid network voltage, u_{js}, the line current, i_{js}, can be regulated by manipulating the control variable e_j. The inner dynamic performance of the MMC which characterize the relation between inner unbalance voltage by and leg current is given by (5) and it is redefined as:

$$u_{jo} = L_0 \frac{di_{jo}}{dt} + R_0 i_{jo} = \frac{1}{2}[U_{dc} - (u_{ju} + u_{jl})] \quad (7)$$

where u_{jo} is the unbalanced voltage $(j = a, b, c)$.

The unbalanced voltage, u_{jo}, can be operated to regulate the difference current i_{jo} in (7).

The references of the upper and lower arm current are given in (8) and (9).

$$u_{ju\_ref} = \frac{U_{dc}}{2} - e_j^* - u_{jo}^* \quad (8)$$

$$u_{jl\_ref} = \frac{U_{dc}}{2} + e_j^* - u_{jo}^* \quad (9)$$

The AC side dynamics is not affected by subtract the upper and lower arm references according to (4) and (6). As previously described, the e_j and u_{jo} is generated by the current controller and circulating current suppressing controller of the MMC system, respectively.

B. NLC method

As shown in Fig. 2, low-switching frequency modulation algorithms used in multilevel converter system is following as: SHE (Selective Harmonic Elimination) [7], [8]; NVC (Nearest Vector Control); and NLC (Nearest Level Control) in order to reduce the switching loss.

Among these, the SHE method is required a lot of calculated switching angle, is needed to compute offline and store in a lookup tables. So, the SHE method is too complex and is needed much calculations.

Therefore, the NLC modulation is used widely in HVDC system because of easier to implement and simple [6]. If the

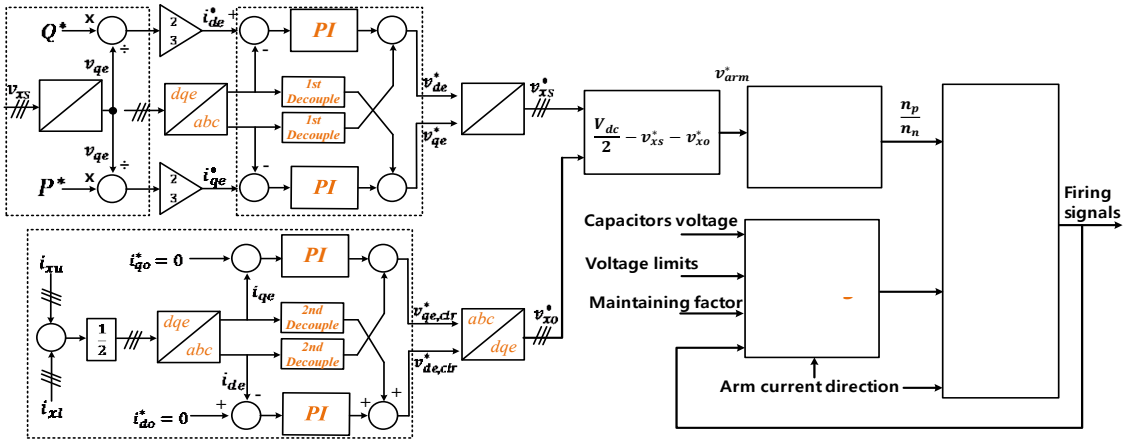


Fig. 5. MMC control diagram with NLC modulation

MMC HVDC system has an adequately large number of SMs, a relatively low harmonic amplitude and low THD (Total Harmonic Distortion) could achieved. Fig. 5 is shown the NLC Modulation's control diagram.

It is important to mention that in DSP(Digital-Signal-Processing) systems, the sampling frequency, f_s, of the reference voltage, u_{ref}, must be considered. When the sampling time, f_s, is applied to control the system with large number of SMs, the sampling frequency must be a high enough to ensure utilizing voltage levels of all SMs.(Fig. 6 (a), every SM generates one step voltage level, so each voltage step is u_c). Using insufficient sampling frequency reduces output voltage level that can be generated. (see Fig. 6 (b), the first and third voltage step are $2u_c$). The voltage reference, u_{ref}, in Fig. 6 (a) and (b) is a staircase waveform with the sampling time, $Ts = \frac{1}{fs}$, instead of a sinusoidal waveform (blue line in Fig. 6 (a) and (b)). The closest voltage level is determined by dividing the voltage reference by the capacitor voltage. (Here, u_c is considered to be a constant).

Finally, the closest voltage level is determined the number of SMs to be turn on. The round(x) function is used to determine the number of turn-on SMs.(e.g., round (3.4) = 3, round (3.6) = 4).

In each arm, the total number of turn-on SMs, n_{on}, is calculated of SMs to be switched on n_{on} is calculated [9].

3. Proposed Nlc Method:cluster stream buffer method

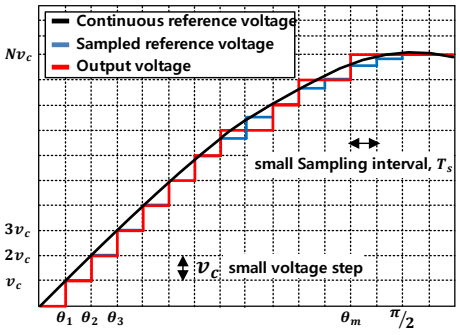
3.1. Cluster Stream Buffer method(CSB method)

The main issue in HVDC systems adopted MMC and NLC methods is to keep the sampling time constant and MMC output constant, as the number of SMs increases.

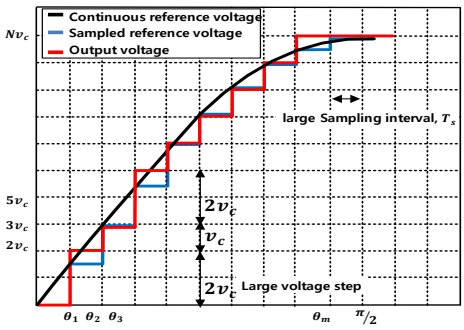
Fig. 6 shows that the MMC output characteristics changes according to the variation of the sampling time. When the interval of sampling time is large shown in Fig. 6 (b), it shows the possibility that the switching of the SM can implement 2 ~ 3 SMs or 5 SMs at the same time.

If multiple SMs switch simultaneously, it is necessary to add a snubber circuit to SMs for each SM's voltage and current distribution equally. This increases the loss of the HVDC system. Therefore, while keeping the sampling time constant, the requirement of a system with a single switching number of the SMs (no snubber circuit required) is necessary for a large capacity HVDC system.

Fig. 7 shows the actual implementation of the cluster stream buffer method, which shows that the number of switching level is commanded from the phase controller to CSB's controller. Fig. 8 (a) and (b) show the algorithm of the CSB method which is a combinations of clusters having each 32 SMs, and the number of cluster increases as the SM level (or voltage level) increases.



(a) Small sampling interval



(b) Large sampling interval

Fig. 6. MMC output characteristics according to sampling interval variation

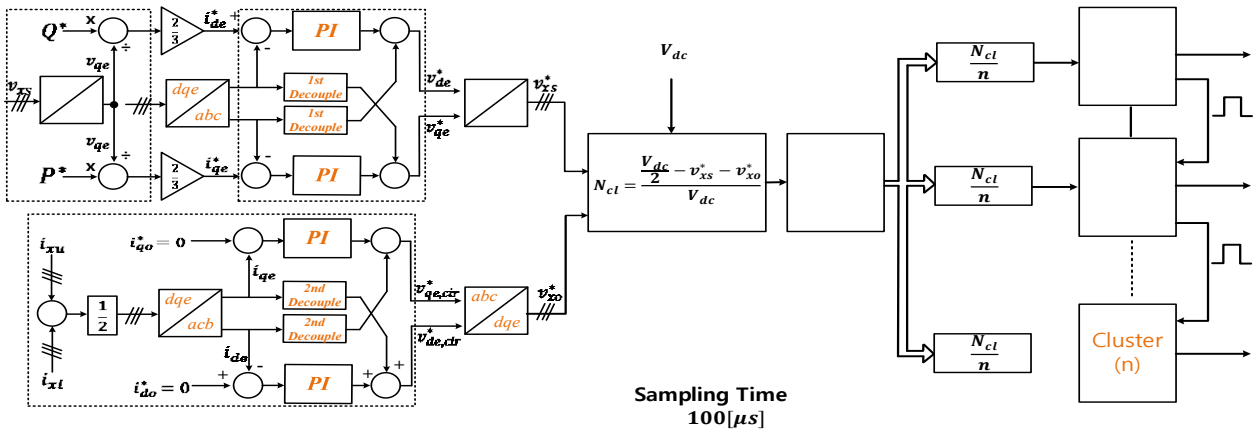
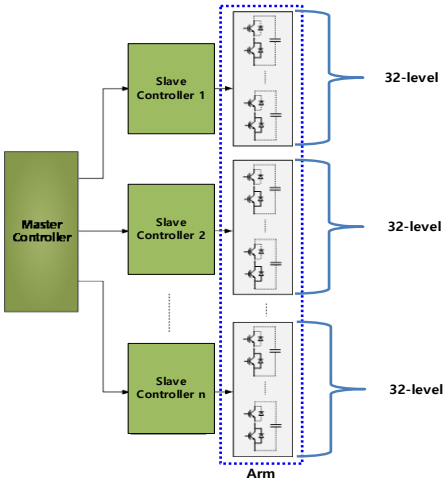
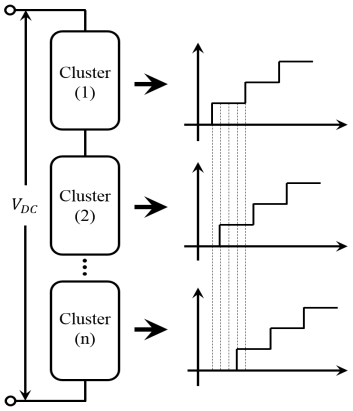


Fig. 7. Actual implementation of Cluster Stream Buffer method

The advantages of this method are to expand the scalability unrestricted (60[MW]→600[MW]) while keeping the fixed sampling time of the system and without degradation of the system performance and complexity. Unlike the module grouping method shown in Fig. 3 approach, which switches the IGBT devices simultaneously, the proposed algorithm guarantees switching the IGBT devices one by one.



(a) Virtual Group of Submodules



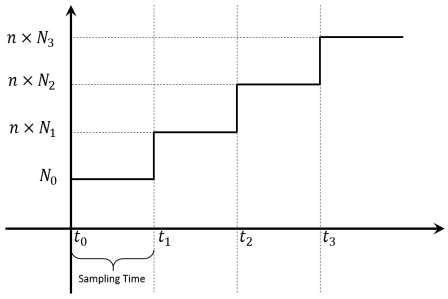
(b) Operation characteristic

Fig. 8. Cluster Stream Buffer Method

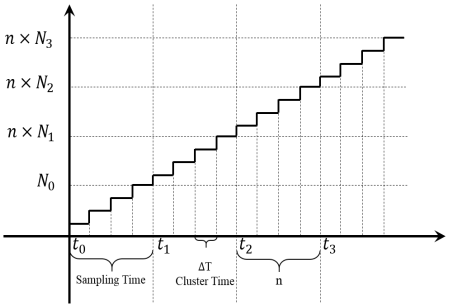
The CSB algorithm would be described as followed. The number of turn-on SMs in the MMC HVDC system, N_{cl}, is divided by the total number of clusters, n, and the result is transmitted to each cluster. The number of all SMs divided in to several clusters based on the system frequency as shown in Fig. 8 and the time delay of the SMs is switched in the same order as Cluster 1, Cluster 2, ⋯, Cluster n.

Then, the output of the MMC based VSC-HVDC system using the proposed algorithm shown in Fig. 9 (b) has a much higher level than the one without the algorithm shown in Fig. 9 (a).

The cluster shown in Fig. 8 (b) can be made of 32 levels or 16 levels. The number of IGBTs of a cluster can be chosen to be 16, 32 or 64. However, selecting 16 IGBTs in a cluster needs many cluster controllers while expanding the MMC system and 64 IGBTs in a cluster causes a reduction in the reliability of the system. Therefore, in this paper each cluster is designed to have 32 IGBTS.

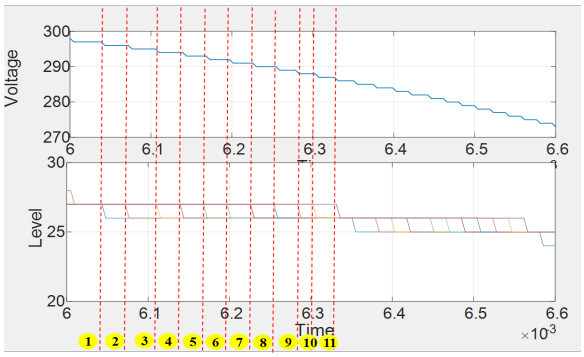


(a) without Cluster Stream Buffer method

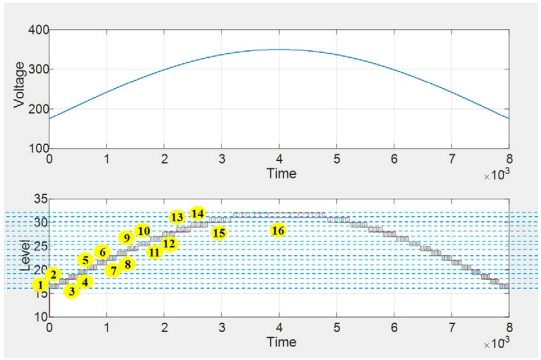


(b) with Cluster Stream Buffer method

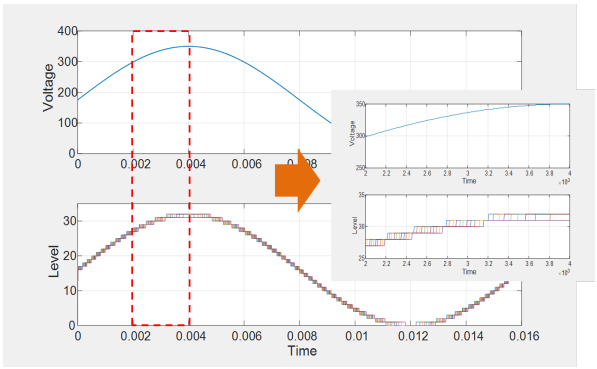
Fig. 9. Waveform characteristics of MMC system using Cluster Stream Buffer method



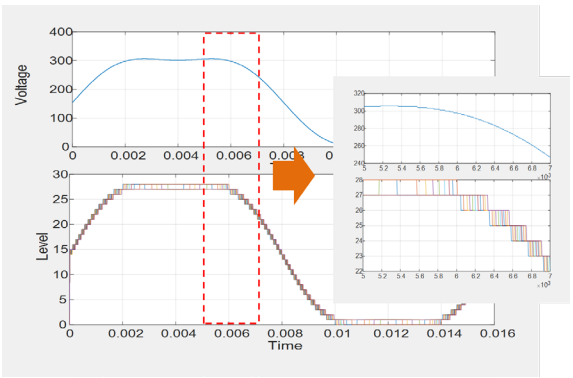
(a) 11 Clusters Operation



(b) 32 Levels (= 32 SMs)



(c) Without 3rd Harmonic Injection



(d) With 3rd Harmonic injection : 15[%]

Fig. 10. Simulation result of the proposed algorithm: Cluster Stream Buffer method

4. Simulation and Review

The performance of the CSB is confirmed through MATLAB/Simulink. The CSB modeled in MATLAB consists of 11 clusters and 1 master / phase controller. Each cluster consists of 32 SMs. The target system in this paper is a system with +/- 300 [kV], Symmetry Mono-Pole HVDC System, and 325 SMs per arm (without redundancy), and the total number of SMs including rectifier and inverter is 3,900. The sampling time of phase controller of HVDC system is 100[us], VBE part and sorting part are skipped.

Fig. 10 shows the characteristics of the proposed system, Fig. 10 (a) shows that the SM is not switched to the group but increases by one. Fig .10 (b) shows the operation waveform of the 32 levels cluster.

Fig. 10 (c) and (d) show the operating waveform when the third harmonic is added to the HVDC voltage command value. In this case, it does not operate up to the 32 levels and it goes up to the 27 levels. The reason for injecting the third harmonic in the converter system is to reduce the loss by reducing the magnitude of the current and by increasing the HVDC voltage to 32 levels by injecting the third harmonic (15[%] of fundamental), the current is 15[%], And the loss is also reduced by 15[%].

5. Simulation and Review

In this paper, an algorithm to control the SMs group of the MMC HVDC system is proposed. The advantages of the CSB method algorithm are summarized as follow:

1. By virtual performing group control of the SM, it is more economical than the method of controlling the transformer (classical method) or controlling the SM in hardware.
2. Compared to the hardware group control that switches the SM at the same time, the snubber circuit is unnecessary and the SM redundancy is reduced (compared with the ABB's method).
3. Sampling time is fixed while the number of SM increases.
4. HVDC system is easy to expand to several GW class.

Finally, the proposed algorithm was validated by MATLAB /Simulink program.

References

[1] R. Marquardt, "Stromrichterschaltungen Mit Verteilten Energiespeichern," German Patent DE 10103031A1, Jan. 24, 2001.

[2] A. Lesnicar and R. Marquardt, "A new modular voltage source inverter topology," presented at the EPE, Toulouse, France, Sep. 2003.

[3] A. Lesnicar and R. Marquardt, "An innovative modular multilevel converter topology suitable for a wide power range," in *Proc. IEEE Power Tech Conf.*, Bologna, Italy, 2003, p. 6.J. Dorn, H. Huang, and D. Retzmann, "A new multilevel voltage sourced converter topology for HVDC applications," in *CIGRE Session*, Paris, France, 2008

[4] G. S. Konstantinou and V. G. Agelidis, "Performance evaluation of half-bridge cascaded multilevel converters operated with multicarrier sinusoidal PWM techniques," in *Proc. IEEE Industrial Electronics and Applications Conf.*, 2009, pp. 3399–3404.

[5] Chan-Ki Kim, Chang-Hwan Park, Jang-Mok Kim, "Level Selection Algorithm with fixed sampling frequency for modular multilevel converter", IEEE-PEMC, Budapest, Hungary, 2018.

[6] S. Sirisukprasert, L. Jih-Sheng, and L. Tian-Hua, "Optimum harmonic reduction with a wide range of modulation indexes for multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 875–881, Aug. 2002.

[7] D. Zhong, L. M. Tolbert, J. N. Chiasson, and B. Ozpineci, "Reduced switching-frequency active harmonic elimination for multilevel converters," *IEEE Trans. Ind. Electron.*, vol. 55, no. 4, pp. 1761–1770, Apr. 2008.

[8] D. Zhong, L. M. Tolbert, and J. N. Chiasson, "Active harmonic elimination for multilevel converters," *IEEE Trans. Power Electron.*, vol. 21, no. 2, pp. 459–469, Mar. 2006.

[9] Chan-Ki Kim, Chang-Hwan Park, Jang-Mok Kim, "고정 샘플링 주파수에서의 모듈형 멀티레벨 컨버터레벨 선택 알고리즘" TKPE, vol. 23, no. 6, pp415-423, Dec. 2018