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Accurate Modeling of the Polysilicon-Insulator-Well (PIW) Capacitor in CMOS Technologies

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Abstract. A practical method enabling rapid development of an accurate device model for the PIW MOS capacitor is introduced. The simultaneous improvement in accuracy and development time can be achieved without having to perform extensive measurements on specialized test structures by taking advantage of the MOS transistor model parameters routinely extracted in support of analog circuit design activities. This method affords accurate modeling of the voltage coefficient of capacitance over the entire range of operating voltages. Furthermore, a compact subcircuit representation is proposed, which takes the distributed parasitic series resistance associated with the PIW capacitor into account, thereby allowing modeling of the limitations imposed on high-frequency performance as well as the quality factor. The validity of the proposed method is verified based on capacitance versus voltage measurements performed using a test vehicle fabricated in a submicron CMOS technology.

Keywords: Polysilicon-insulator-well MOS capacitor model, CMOS

1. INTRODUCTION

Integrated circuit (IC) implementation of analog circuits generally requires passive components. In radio frequency (RF) circuit applications, for example, area-efficient inductors with high values of quality factor and resistors with low self-capacitance and temperature coefficients are highly desired, but seldom available. Capacitors with high quality factors and low temperature coefficients, however, are readily available albeit at the cost of increased process complexity. In CMOS technologies, the gate capacitance of the MOS transistor can be used to form a polysilicon-insulator-diffusion (PID) capacitor whose bottom plate consists of a heavily-doped (degenerate) implant of the same type as the source and drain. This structure, however, requires an additional masking and processing step. Metal-Oxide-Semiconductor (MOS) capacitors are not only an attractive choice for implementation of on-chip capacitance in CMOS technologies, but also are the predominant monolithic capacitors employed in bipolar ICs. The MOS capacitor structure can also be employed in GaAs-based ICs using HfTiON or a polymer-based thin film as the gate dielectric, and in ICs based on the silicon-on-insulator (SOI) technology using HfLaO as the gate insulator [1-3]. A MOS capacitor can be implemented without any modification to the standard CMOS process by constructing a depletion-mode MOSFET, using n^+ source-drain implants in an n-well (in a p-substrate CMOS technology). A simple schematic of this capacitor, which will be hereafter referred to as a polysilicon-insulator-well (PIW) MOS capacitor, is shown in Figure 1.

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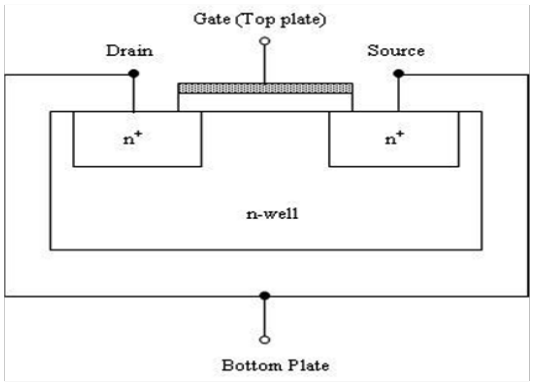

Figure 1. Schematic of the cross section of the PIW Capacitor.

The decrease in process complexity associated with constructing PIW MOS capacitors, nevertheless, is achieved at the expense of a higher voltage coefficient, since the channel formed in the n-well is not doped to degeneracy. While most foundries provide accurate models for standard devices, the depletion-mode MOSFET formed in the n-well is usually neither characterized nor modeled. Accurate simulation of the behavior of PIW MOS capacitors requires characterization of a test vehicle containing the structure (ideally with the same dimensions as that used in the circuit) to build a transistor model for the individual depletion-mode MOSFET segments comprising the structure. Since, such a model is seldom available from the foundry, and the required modeling effort is relatively extensive, an approximate model with reasonable accuracy is desirable. In this work, a practical method allowing development of an accurate model for the PIW MOS capacitor is presented. This model is obtained through ready generation of model parameters for the depletion-mode MOSFET formed in the n-well. The accuracy of the proposed model for the depletion-mode MOSFET is experimentally confirmed by simulating the capacitance versus voltage (C-V) behavior of the resulting MOS capacitor, and comparing it to the measured C-V data obtained using the PIW MOS capacitor test structure. Furthermore, the appropriate representation of the PIW MOS capacitor is identified in it terms of a subcircuit. The subcircuit representation permits inclusion of the parasitic series resistance, thereby enabling accurate modeling of the quality factor as well as the high-frequency performance of the circuit.

2. PHYSİCAL MODEL

As opposed to a PID capacitor, the bottom plate of a PIW capacitor is composed of the relatively lightly doped n-well. A PIW MOS capacitor implemented in a deep submicron CMOS technology, therefore, exhibits a significant voltage coefficient due to the non-uniformity associated with the well doping. This voltage dependence is particularly severe in CMOS technologies with a retrograde well doping profile due to the presence of a retarded electric field. While the PIW MOS capacitor enters the deep accumulation mode at relatively low positive gate voltages, at gate voltages close to the flatband voltage of the MOS structure a depletion region starts to form underneath the gate due to a reduction in the electrostatic attraction between the positively charged gate and the negatively charged free electrons. The contribution of depletion capacitance in series with the oxide capacitance must, therefore, be included in the computation of the overall capacitance to account for the reduction of the value of the PIW capacitance at smaller applied gate voltages. Accounting for this contribution is particularly important in presence of a retrograde well doping profile, since the doping concentration would be smaller near the surface and a retarded electric field would oppose diffusion of free electrons to the area underneath the gate. Accurate modeling of the PIW capacitor using a simple capacitor element in SPICE simulations, therefore, requires

specification of voltage coefficients of capacitance in the definition of this element. The voltage coefficient of the gate capacitance, however, can be readily accounted for in SPICE simulations by modeling the PIW capacitor as an n-channel depletion-mode transistor whose source and drain are connected to one another. Using this approach the PIW capacitor is modeled as a true MOS capacitor, since the contribution from depletion capacitance is taken into account by the intrinsic gate capacitance model for the MOS transistor.

Accurate modeling of the PIW capacitor for high-frequency applications also requires inclusion of the parasitic resistance in series with the gate. In addition, the quality factor of the MOS capacitor is determined by the series resistance associated with the channel and that associated with the polysilicon forming the gate. Since the source and drain are connected to one another in the PIW capacitor implementation, the series channel resistance is simply shorted out in SPICE simulations. A subcircuit representation for the PIW capacitor is, therefore, required to include the influence of parasitic series resistances in circuit simulations. Since area-efficient implementation of a PIW capacitor necessitates use of a finger structure in the physical design (layout), it is important to define the capacitor as a parallel combination of subcircuits each representing a single finger in order to account for the series channel resistance accurately. The subcircuit representation of the MOS capacitor provides a more accurate description of the distributed nature of the gate capacitance structure, which tends to be quite important in high-frequency applications. Nevertheless, a subcircuit representation involves a trade-off between accuracy and simulation time. As depicted in Figure 2 the effective series resistance of the channel and that of the polysilicon are identified as separate elements for each finger in the definition of the subcircuit. The effective series resistance of the channel, $r_{ds\text{-}eff}$, depends on the value of the channel resistance, r_{ds}, which can be approximated by the drain-to-source resistance of a minimum-feature-sized MOSFET with effective channel length $L_{min\text{-}eff}$ operating in the linear region The corresponding channel width, W_{finger}, is that of a single gate finger in the layout of the PIW capacitor. The expression for r_{ds} is given by

$$r_{ds} = \frac{L_{min\text{-}eff}}{\mu_n C_{ox} W_{finger} (\bar{V}_{GS} - V_T)} \tag{1}$$

where μ_n is the electron mobility, C_{ox} is the gate oxide capacitance per unit area given by the ratio of the dielectric constant of silicon dioxide to its thickness, V_T is the threshold voltage of the device, and $\bar{V}_{GS}$ is the average gate-to-source voltage determined based on variation of the voltages at the MOS capacitor terminals.

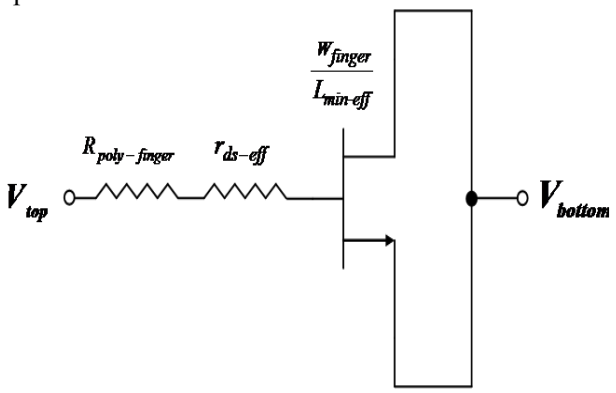

Figure 2. Subcircuit representing the PIW capacitor in SPICE simulations.

A more accurate value for r_{ds} can be determined based on SPICE simulations using the transistor models derived for the depletion-mode NMOS transistor in an n-well as described above. As shown in Figure3, a worst-case estimate for the effective series resistance of the channel, $r_{ds\text{-}eff}$, is equal to one-fourth of the channel resistance, $r_{ds}/4$. This estimate accounts for

the maximum resistance extending from the centre of the channel to the source and drain regions, which is equivalent to the parallel combination of two $r_{ds}/2$ resistances [4].

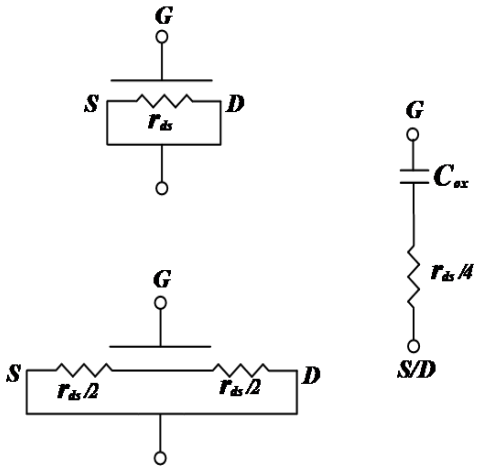

Figure 3. Worst-case estimate for the effective series resistance presented by the MOSFET channel

3. EXPERİMENTAL VERİFİCATİON

The test vehicle for characterizing the PIW capacitors consisted of a multi-fingered NMOS transistor of minimum feature dimension (L_{min}=0.35μm) fabricated in a 0.35μm p-substrate CMOS technology with an n-well region forming the body of the transistor. Minimum allowable device length was used so as to maximize the quality factor by minimizing the channel resistance at a given applied voltage. The gate capacitance was measured by connecting the source and drain terminals together. The modeled-versus-measured C-V characteristics of a typical PIW capacitor are shown in Figure 4. The modeled data was obtained based on the NMOS transistor model for wide devices of minimum feature gate length. In particular, the MOSFET SPICE model parameters determining the threshold voltage and the well concentration, typically denoted by Vth0 and Nsub respectively, were adjusted to reflect the fact that PIW capacitors are constructed as depletion-mode MOSFETs with n^+ source-drain diffusions in an n-well. The modeled-versus-measured fit depicted in Figure4 corresponds to a coefficient of correlation of 0.99.

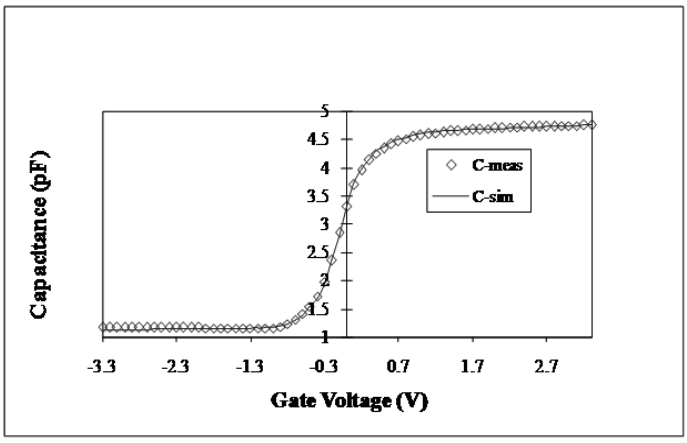

Figure 4. Typical modeled-versus-measured C-V data for a PIW capacitor.

4. DİSCUSSİON

If the gate capacitance of standard MOSFET is employed to form a capacitor care must be exercised to maintain device operation in the strong inversion mode, with the gate-to-source voltages significantly exceeding the threshold voltage. At gate voltages close to the threshold voltage of the MOS structure, the semiconductor surface is depleted and the overall MOS capacitance, given by the series combination of the gate oxide capacitance and the depletion capacitance, exhibits pronounced voltage dependence. Use of a PIW capacitor constructed as a depletion-mode NMOS transistor in an n-well significantly reduces the voltage dependence of the MOS capacitor. As is evident from Figure 4, with the threshold voltage of the device being negative the semiconductor surface resides in the accumulation mode over a much wider range of gate-to-source voltages, namely from approximately 0.2V to V_{DD}=3.3V. The proposed method accurately accounts for the voltage dependence of capacitance over the entire voltage range as demonstrated by the accuracy of the modeled-versus-measured fit of Figure 4.

The worst case estimate of the effective series channel resistance given in section 2, assumes a single-section gate structure flanked on each side by half of the channel resistance as indicated in Figure 3. A more reasonable approximation for the effective series resistance associated with the PIW capacitor can be performed using steady state sinusoidal analysis by treating the device structure as a lumped *RC* network consisting of a relatively small number of sections. The number of sections chosen depends on the frequency of operation. At sufficiently high frequencies, where the physical dimensions of the circuit become comparable to the shortest wavelengths of interest, circuit elements must be treated as distributed. Therefore, in order for lumped circuit analysis to remain valid, a larger number of sections must be chosen at higher frequencies. For a three-section gate structure, sinusoidal steady state analysis using a T-model gives an effective series channel resistance of $r_{ds}/8$.

Approximation of the effective series resistance associated with silicon solely based on the channel resistance, however, grossly overestimates the effective series resistance, since the part of the gate capacitance overlapping the source and drain is exposed to a smaller series resistance as compared to the part near the centre of the channel [4]. That is, portions of the gate capacitance near the source and drain corresponding to the overlap of these regions with the gate should be regarded in association with the parasitic series resistance of source and drain, which tends to be considerably smaller than the resistance of the inversion layer in the centre of the channel. This effect is particularly important in deep submicron CMOS technologies as the extent of the lateral diffusion of source/drain regions underneath the gate becomes a significant fraction of the drawn gate length. Regardless of the specific component dominating the series resistance associated with the PIW capacitor, however, use of large device widths tends to reduce the effective series resistance.

The decrease in process complexity associated with constructing PIW MOS capacitors, nevertheless, is achieved at the expense of a higher positive temperature coefficient, since the well is not doped to degeneracy. This temperature coefficient is even higher in technologies with a retrograde well doping profile, where the doping concentration at the surface is diminished.

4. CONCLUSİONS

A practical method has been presented which allows ready development of an accurate model for the polysilicon-insulator-well (PIW) capacitors fabricated in CMOS technologies. The model for the PIW capacitor is derived from that of the standard NMOS transistor and describes the measured capacitance versus voltage characteristics of the device with excellent accuracy. The relevant considerations for estimation of the effective series resistance associated with the device structure were discussed and the appropriate implementation of the PIW capacitor as a subcircuit was presented.

REFERENCES

[1] Li-Sheng Wang, Lu Liu, Jing-Ping Xu, Shu-Yan Zhu, Yuan Huang, Pui-To Lai, "Electrical Properties of HfTiON Gate-Dielectric GaAs Metal-Oxide-Semiconductor Capacitor With AlON as Interlayer", IEEE Trans. on Electron Devices, Vol. 61 , No. 3, pp.742-746, 2014.

[2] E.H. Oulachgar, C. Aktik, , M. Scarlete, "Fabrication and Characterization of GaAs MOS Capacitor With CVD Grown Polymer-Based Thin Film as a Gate Dielectric", IEEE Trans. on Electron Devices, Vol. 57 , No. 8, pp.1942-1947, 2010.

[3] Wan Wenyan, Cheng Xinhong, Cao Duo, Zheng Li, Xu Dawei, Wang Zhongjian, Xia Chao, Shen Lingyan, Yu Yuehui, Shen DaShen, "Properties of HfLaO MOS capacitor deposited on SOI with plasma enhanced atomic layer deposition", Journal of Vacuum Science & Technology A: Vacuum, Surfaces, and Films, Vol. 32, No. 1, pp. 01A127 - 01A127-4, 2014.

[4] T.H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, New York: Cambridge University Press, 1998, p. 39.