



Designing and simulation SOI MOSFET transistor to enhance DIBL parameter and improve self-thermal effects

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Abstract. In this study, a new structure for FD SOI MOSFET has been presented to improve DIBL parameter and also to enhance self-heating effect. The main idea of this structure is to change the thickness of BOX layer in transistor in order to improve DIBL parameter and self-heating effect.

Keywords: Self-Heating Effect, FD SOI MOSFET, DIBL.

1. INTRODUCTION

Due to the large-scale integration of silicon devices, considerable problems such as reducing switching speed and increasing power consumption in functional circuits are appearing. That's why, silicon on insulator technology is replaced by body silicon technology [1]. In this technology, a layer as the insulator causes improving a great deal of features of transistors in functional circuits. Advantages of MOSFET transistors in silicon on insulator technology compared with Bulk transistors include decreasing short-channel effects, increasing circuit's speed and less parasitic capacitance. This technology has shown his superiority in different contexts such as increased immunity against activation of parasitic transistor and creating leakage currents, decreasing supply voltage, protection against radiation etc. [2, 3] This causes increasing efficiency of these transistors in Analog and Digital circuits which are working with low power and voltage [1].

These advantages in SOI technology is the reason for buried oxide layer. In most of cases, this layer is made from silicon oxide, but low thermal conductivity of the buried oxide compared with silicon [4] has created many problems such as appearing self-heating effects and reducing device cooling capability. Also, increasing temperature causes decrease in electron mobility in devices and also causes decrease the maximum transistors current in saturation.

2. FD SOI TRANSISTOR

One of the advantages of silicon on fully depleted insulator technology compared with body silicon technology is enhancement in immunity against short-channel effects due to making silicon film with T_{Si} thickness less than link depth X_j and depth of discharge region X_{dep} [5], but with decreasing device dimensions (In this particular design 32nm scale), problems driven from short-channel effects are decreasing. Here, we intend to change device such as metal gate and

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very thin body. We want to minimize these effects. Schematic of this studied device has been shown in figure 1.

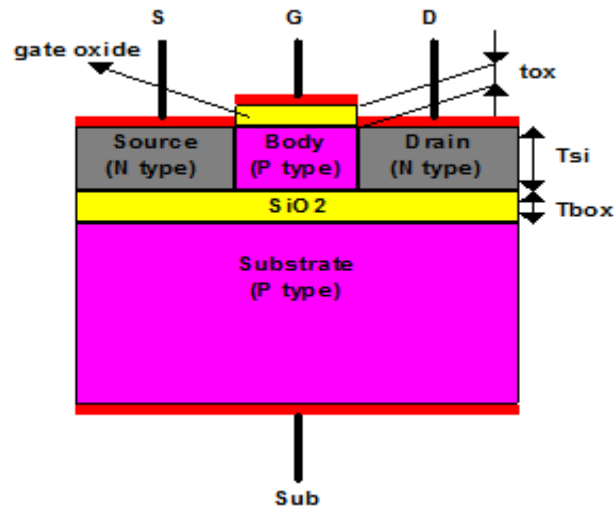


Figure 1. Schematic of silicon device on fully-depleted insulator.

Decreasing device dimensions to decrease short-channel effects forces us to increase body doping. Increasing in body doping causes decrease in carriers' mobility which this parameter causes limitations for device scaling. Here, in order to solve arisen problem, no doping bodies' technology has been used. No doping bodies or with low doping (10^{15}cm^{-3}) can be used to reach high mobility of carriers and improving drive current. Also, these kinds of bodies are appropriate for minimizing threshold voltage changes (V_{TH}) due to statistic changes of doping.

3. SILICON FILM THICKNESS AND SUBSTRATE DOPING

In silicon on fully depleted insulator transistors, short-channel effects are controlled by very thin bodies and there is a possibility to maintain no doping region. Decreasing silicon film thickness (T_{Si}) will lead to decrease capability of front gate control on active region of stronger channel and also reduction in source/drain effect on channel. So, short-channel effects are decreased. Advantages of using very thin films is immunity against threshold voltage changes due to doping changes and promoting carriers' mobility and decreasing gate tunneling current [6,7].

Based on rules of ITRS council, to design silicon on fully depleted insulator devices, silicon film thickness (T_{Si}), has to be follow 2 following relations [7, 8]:

$$T_{Si} \leq \frac{1}{4} L_G \quad (1)$$

$$T_{Si} < X_{dmax} \quad (2)$$

Due to this issue that studied device has 32 nm channel length, so $T_{Si} \leq 8 \text{nm}$ and on the other hand, X_{dmax} based on $\sqrt{4\epsilon_{Si}\phi_F/qN_A}$ relation are obtained. In this study, devices with very thin bodies are being used. So, in these devices, 5 nm silicon film thickness devices have been considered.

Substrate doping based on its resistance has been obtained from relation (3):

$$\rho = \frac{1}{q\mu N_{SUB}} \tag{3}$$

Q is electron loading and equals to $1.6 \times 10^{-19}C$ and μ is substrate majority carrier mobility and N_{SUB} is substrate doping and ρ is an especial substrate resistance.

4. DESIGNING AND SIMULATION OF FD SOI

In the ultra-thin body, if the temperature increases, it is too much raised. Parameters such as mobility and current stimulus are influenced and decreased. In this paper, it is simulated using ISE-TCAD and external features of FD SOI reach to 32nm. Hydrodynamic model in this simulation has been used. Applying this model in nm scale can modify temperature features in MOSFET.

In hydrodynamic model, energy conservation equations in electron and channels and networks are solved. In this model, unlike Drift diffusion model of T_P and T_N , it is not equal to T_L network temperature [9]. Based on ITRS’s necessities about designing FDSOI MSOFET, layer thickness is based on the following equation:

$$1) T_{si} \leq \frac{1}{4} Le$$

$$2) T_{si} < X_{dmax}$$

X_{dmax} , Le are channel length with maximum empty width, respectively. In SOI (reviewed in this study), silicon layer thickness has to be equal to 5 nm. Features of MOSFET designed and explored in this paper is as the following:

Table 1. Physical features of studied FD SOI device.

Gate length	32
Front gate oxide thickness $t_{ox}(nm)$	1
Silicon oxide layer thickness (nm)	30
Silicon film thickness $T_{si}(nm)$	5
Source /drain impurity concentration (cm-3)	$10^{20} \times 1$
Channel impurity concentration (cm-3)	$10^{15} \times 1$
Substrate impurity concentration (cm-3)	$10^{12} \times 5/3$ & $10^{15} \times 1$

5. INVESTIGATING DIBL PARAMETER

DIBL is one of the effects of short-channels in SOI and reflection of electronic effect of drain terminal voltage (VD). It is on the source channel with the highest barrier when VD voltage is increasing. Also, VD is increasing; resource channel with the highest barrier is decreasing and leads to increase in junction in most of resource carriers in the channel. Therefore, VT will be

decreased with V_D . While we have increase in leakagecurrent [10], BOX thickness is just $30(\text{SiO}_2)$ nm.

$$36mV_N = DIBL$$

In the weak inversion region, there is a potential dam for channel and source regions. Height of this dam is driven from diffusion and drift currents between these two regions. Dam height for channel carriers is ideally controlled by gate voltage. In this case, conductivity transition is maximized. Reducing dam height for channel carriers in the source edge due to drain electronic field effect causes DIBL to occur. Increasing numbers of input carriers into channel from source causes increasing silence of draincurrent. Therefore, drain current is controlled not only by gate voltage, but also by drain voltage [6].

This parasitic effect is calculated by decreasing threshold current by drain voltage.

$$DIBL = \frac{V_{TH}(V_D=1.1V) - V_{TH}(V_D=0.05V)}{1.1 - 0.05} \quad (4)$$

For the shorter gates, dam's height for holes near the ends of the drain electric field effects are reduced and accumulated holes in the body can easily be poured into the source [11].

To obtain DIBL, V_{TH} in V_D has to be obtained equal to V_{DD} and 0.05 volt. This value can be obtained from I_d - v_g chart as the following figure.

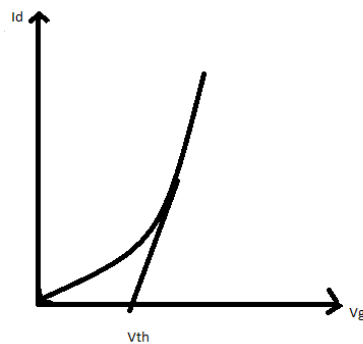


Figure 2. Descriptive chart of I_d - v_g .

In figure 3, changes of DIBL parameter based on BOX thickness changes have been shown. As it was seen, T_{BOX} decrease causes decrease in DIBL.

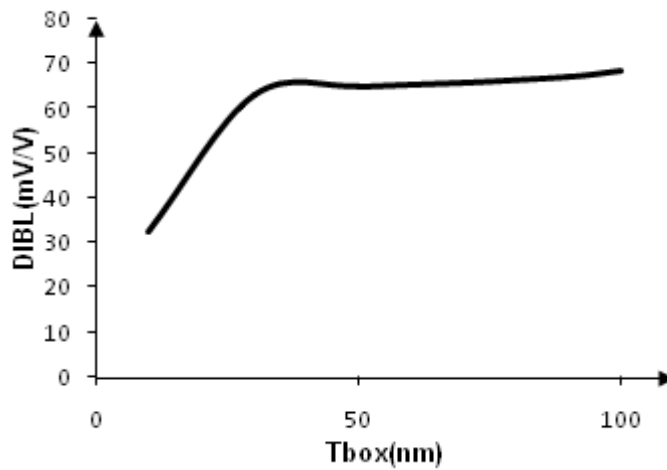


Figure 3. DIBL changes based on TBOX changes.

6. SELF-HEATING EFFECTS

Features of silicon on insulator MOSFET due to silicon oxide (BOX) are affected by self-heating effects. To investigate this effect more, we examine maximum changes of channel temperature with BOX thickness changes. Figure 4 shows T_{MAX} changes based on T_{BOX} changes. According to this figure, BOX thickness decrease (silicon oxide) will lead to decrease the maximum temperature of channel. Due to this issue that silicon oxide thickness will make thermal exchange of channel with silicon substrate easier and subsequently, self-heating effects will be decreased. With choosing 30nm thickness silicon oxide, in addition to choose an optimal point for DIBL parameter, also from viewpoint of self-heating, thickness is optimal.

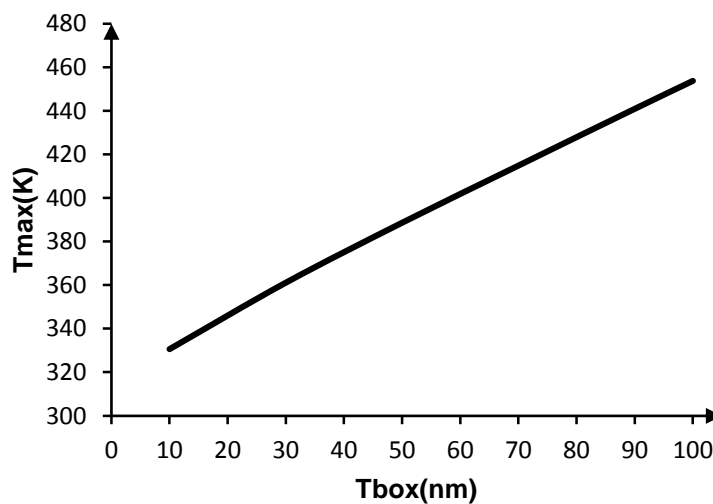


Figure 4. Maximum temperature of channel based on silicon oxide (BOX) thickness for silicon on fully depleted insulator device.

Having very thin body in Silicon-on-insulator devices causes decreasing in short channel effects and leakage current reduction and good capability of scaling. On the other hand, due to thinness of silicon film, problem of parasitic capacitors and thereby, co-heating will be increased. On the other hand,heat distribution by regions of source / drain will be lessened. Therefore, temperature of thin film will be increased and self-thermal effects will be severely increased and self-thermal will cause decreasing performance of silicon-on-insular MOSFET (such as reducing mobility and drive current etc.).

Due to changes in thickness of silicon oxide from 0.1 micron to 30 nanometers, the maximum temperature of channel has been decreased. Thus, self-thermal in this MOSFET has been enhanced.

7. CONCLUSION

In this study, with choosing silicon oxide thickness in FD SOI MOSFET device equal to 30nm, in addition to choose an optimal point for DIBL parameter, also from viewpoint of self-heating, thickness is optimal.

By simulating this structure and investigating DIBL parameter and also temperature, it will lead to present a suitable designing window, so that designed transistor not only causes improving short channel effects in this area, but also, it has the low temperature.

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