



## Vlsi Implementation Of Digital Image Segmentation Algorithm For Gray Scale Images

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**Abstract.** This paper proposes a realization of digital algorithm for gray scale image segmentation with some modification on LEGION algorithm. .LEGION is one of the best algorithms for digital image segmentation. It is based on region growing method and has all the advantages of region growing approach. This algorithm was simulated in model-sim5.8 C and realized using Xilinx 6.3 tools. The segmented image results were verified by using Matlab.

**Keywords:** Image Segmentation, Oscillator Network, FPGA Implementation, VHDL, Region Growing, Leader Cell

### 1. INTRODUCTION

Image segmentation is the process by which the original natural image is partitioned into meaningful regions. In other words image segmentation is segregating the interested parts from the original image.

Image segmentation is very important while processing the image in higher levels such as object tracking, the image is not segmented, and the tasks said above take complicate manipulations and very long Processing time unnecessarily. After segmentation, only interested parts undergo processing and the processing time will be reduced and manipulation also be simplified. Several image segmentation algorithms have already been proposed and can be classified into five groups [6], namely,

1. Pixel classification
2. Edge-based approaches
3. Region based approaches
4. Modal based approaches
5. Hybrid approaches

The hybrid approach combines both region-based approach and model based approach.

Locally Excitatory and Globally Inhibitory Oscillatory Networks – Legion

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**DESCRIPTION:**

LEGION stands for locally excitatory globally inhibitory oscillatory network [1].Image segmentation using this method, has some advantages when compared to other models. LEGION is composed of the following elements:

A model of a basic oscillator (each pixel in an image represents one oscillator).

Local excitatory connections to produce phase synchrony within each object.

A global inhibitor that receives inputs from the entire network and feeds back with inhibition to produce de-synchronization of the oscillator groups representing different objects.

**1.1 Legion model:**

LEGION was proposed by Term an Wang as a biologically plausible computational framework for image segmentation and has been used successfully to segment binary and gray-level image data. It is a network of relaxation oscillators, each constructed from an excitatory unit 'X 'and an inhibitory unit

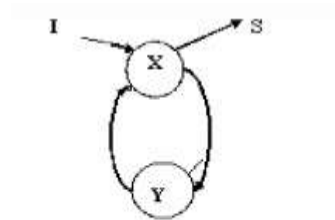


Figure 1. Diagram of single oscillator.

'Y 'as shown in Fig.1. Unit ' X ' sends excitation to unit ' Y ' which responds by sending inhibition back to unit ' X '. When external input stimulus ' I ' is continuously applied to ' X ', this feedback loop produces oscillations. Neighboring oscillators are connected via mutual excitatory coupling, as well as the global Inhibitor. In this Fig.1. a single oscillator with an excitatory unit ' X ' and an inhibitory unit Y in a feedback loop. A triangle indicates an excitatory connection and a bubble indicates an inhibitory connection. ' I ' indicate external input and ' S ' indicates the coupling with the rest of the network. Fig.2 shows a 2D architecture with 4-neighborhood coupling. The global inhibitor, shown with a black circle, is coupled with the entire network [3]-[5]. The white circle represents oscillators.

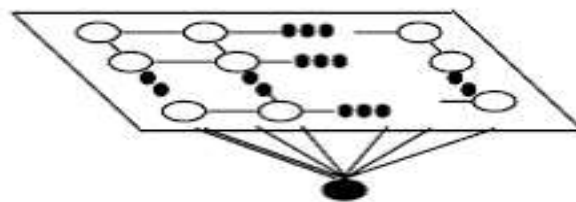


Figure 2. Architecture with 4 – neighborhood coupling.

### 3. DIGITAL IMAGE SEGMENTATION ALGORITHM

The algorithm has six functional steps with some modification on EGION[3] described above. They are given below.

Initialization.

Calculation of Leader cell.

Self excitation of Leader cell.

Calculation of dependent cell.

Excitation of dependent cell.

Inhibition of all excited cells.

#### 3.1 Initialization Step:

1. The global inhibitor 'G' is initialized as zero.
2. The image is stored in 'I' matrix which has dimension of 2D. In this matrix, I(a, b) represents the intensity value of the pixel in 'a' row and 'b' column.
3. Calculation of connection weights:

Weight matrix is a 4D one. It represents the weight value between pixels. It is calculated by using the following formula,

a) Gray scale images

$$W(a, b, c, d) = I_{max} / [1 + |I(a, b) - I(c, d)|]$$

Where

$$W(a, b, c, d)$$

Represents the weight value between pixel (a, b) and pixel (c, d).

#### 3.2 Calculation Of Leader Cell:

Define a Leader cell matrix 'L' and initialize it as zero.

For each pixels (a, b) in matrix 'I' Initialize  $W_t = 0$ ;

For all neighbor pixel (c, d)

$$W_t = W_t + W(a, b, c, d)$$

If  $W_t > th_1$  then  $L(a, b) = 1$  Else null;

Where  $th_1$  is a pre-defined threshold and now the matrix 'L' contains leader cells, which have the value 1 in the 'L' matrix.

### 3.3 Self – Excitation Of Leader Cell:

The leader cells have the capability of self-oscillatory. Define a 2D matrix 'E' containing the oscillatory pixels and initialize to all zeroes. For all pixels (a, b) in the matrix 'L', If (excitable cells = false) then stop;

//all leader cells are analyzed. So stop.

//If a leader cell is got then it is self excited. The global inhibitor 'G' made 1.

//Else if (find leader () == (a, b) and L (a, b) ==1)

Then

E (a, b) = 1; G = 1;

Go to next step.

Else go to self – excitation step;

### 3.4 Calculation Of Dependent Cell:

If pixel ( c , d ) is a neighbor and  $W ( a , b , c , d ) > th2$  then pixel( c , d ) is a dependent cell.

### 3.5 Excitation Of Dependent Cell:

If the difference between E ( a , b ) and I ( c , d ) is less than another threshold then E ( c , d ) = 1; Else E( c , d ) = 0; [It is called *selective gating*]

### 3.6 Inhibition Of All Excited Cells:

Inhibit all the excited cells. Now one segmentation is over. Go to the first step if still more segmentation. Otherwise stop of the algorithm.

## 4. SEGMENTATION CHIP MODEL:

The chip consists of six blocks namely,

1. Input ROM block
2. Weight calculation block
3. Leader cell block
4. Locally Excitatory block
5. Segregation and Inhibition block
6. Output RAM block

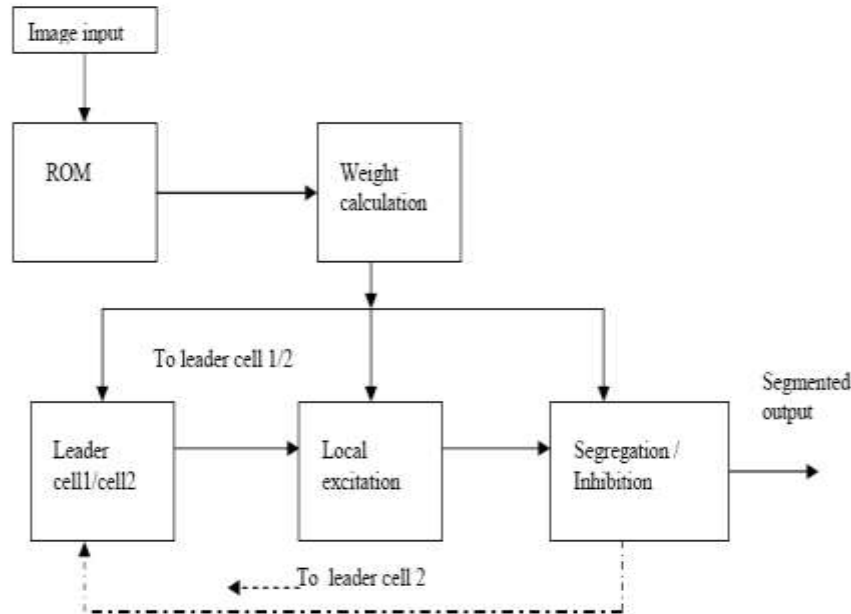


Figure 3. Blocks of the segmentation chip model.

Now we will discuss the six blocks one by one

#### 4.1 Input Rom Block:

VHDL [7] deals with only numbers and not images. However, image can be treated as a 2D matrix consisting of integer values. The integer values can be varied from 0 to  $(2^n - 1)$  for a 'n' bit gray image. For example, an 8 bit gray image has integer values 0 to 255, where 0 represents the dark and 255 represents the bright. The intensity values in between has the proportion of the dark and bright.

#### 4.2 Weight Calculation Block:

The second block of image segmentation is weight calculation block. VHDL process starts from here. The input of weight calculation block is the intensity values from input ROM. The weight is calculated by the given formula

$$Wt = W(a, b, c, d) = I_{max} / [1 + |I(a, b) - I(c, d)|]$$

At the time of calculating a weight of a pixel, the weight values between the pixel and its spatial neighbors are calculated and added.

#### 4.3 Leader Cell1:

The input to the leader cell is the weight values of the pixels from weight calculation block and a threshold value. The processing of leader cell 1 is simple. It merely compares the weight value of a pixel with the given leader threshold value. If the weight value exceeds the threshold then a '1' is stored for the pixel in an array. If the weight value is less than the threshold then a '0' is stored for the pixel in the array. After processing the array consists of 1's and 0's.

#### 4.4 Local Excitation Block:

The input to the local excitation block is ROM input, leader cell output and a local threshold value. This block starts to scan the leader cell from the top of the array and goes to the bottom of the array. If it encounters a 1 in leader cell array then the pixel is made as 1 in its output array.

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Then the intensity value of that pixel and the spatial neighbor pixels are getting from the input ROM and calculate the weight value. Then compare the weight value with the local threshold value. If it is greater than the local threshold value, then the neighbor pixel is made as '1' in its output array. Otherwise, the neighbor pixel is made as '0' in the output array. In the same manner, all the neighbor pixel values are stored in output array of local excitation block. If the leader cell value is other than 1, the pixel won't eligible for local excitation. The process repeats row size times in order to make sure all the neighboring cells are excited in a segment.

### 4.5. Segregation Block:

There may be more possibilities for two or more entirely different regions are clustered in a pass. But if those different regions are segmented as it is, then there is no meaning for segmentation. Those regions should be segregated before producing the output. The job of segregation block is to segregate the different regions and inform the previous blocks about the actions. Then only in the next pass the leader cell block will consider the non-outputted pixels for considering the leader cell again. The inputs to the segregation block are the input ROM values, the output array of local excitation block and a segregation threshold value. It has two outputs. One is segmented output and the second one is an array-consisting the details of outputted pixels. The no outputted pixels have value 0 in this array. The outputted pixels having values other than zero. The process of segregation block is as follows. It scans the output array of local excitation block for a 1 value. It scans from the top to bottom in the one dimensional array which is equal to scan from top left to bottom right of the 2D image. If it encounters a '1' immediately it collects the corresponding pixels ROM value and memorized it. The scanning process will be terminated as soon as it reaches a 1 value. Since, it scans from the top of the array the '1' which is in the top has higher priority. A designer can choose his own priority. In this paper the priority was given to the top pixel. Now, again the scanning process begins. Again it looks for 1's. But the process is not terminated after encountering the first '1'. It goes until it reaches the bottom most, last value in the array. If it meets a '1' in this pass, it collects the intensity value of the corresponding pixel and it compares the value with the memorized intensity value. If the difference between the two intensity values within the segregation threshold, the pixel is made as '1' in its output array, otherwise it is made as '0'. If the pixel value is made as '1', its intensity value is stored in another output array and otherwise a default value is stored.

In this paper, the default value is chosen as 255. Similar to local excitation block, if the input array has value other than '1', then the pixel is discarded and in output label array the same input value stored and in output intensity array the default value is stored. Now the output label value is given to leader cell 2 blocks and output intensity array is given to output RAM. The cells with label '0' only considered for next pass and other cells won't consider for next segmentation. So, segregation block is doing the job of inhibition also.

### 4.6. Leader Cell 2:

Leader cell 2 has three inputs. One is from weight calculation block and the other from segregation block and the third is, of course, the leader threshold value. The block scans the labeling output array from the segregation block for 0 values. If it finds a 0, it collects the pixel's weight value from weight calculation block. Similar to leader cell 1 the weight value is compared with the leader threshold value and if exceeds a 1 is stored in the output array or else the 0 retains. If the label value of a pixel is other than 0 the label is simply incremented once. So, contrary to leader cell 1, its output has 0s 1s and other values. The output is given to local excitation block.

So, local excitation block may have inputs in an array with only 0s and 1s (from leader cell 1) or various combinations (from leader cell 2). Local excitation block, as stated previously concentrated on 1s and its neighboring 0s only. Other pixels are discarded and their labels are copied in its output array. If the pixels with 0 as label and placed spatially nearer to the leader

pixel may have label 1. This output is given to segregation block. This process repeats the number of segmentation times. All the individual segment results are stored in individual RAMs. Finally RAM values are converted in to images.

#### 4.7. Algorithm Flow:

The program flow is explained for a 5 by 3 matrix image. Remember it is a toy problem. Actual image size will be very high compared with this 15 pixel image. In order to explain the flow only, this example is taken.

1) Input ROM values.

24	36	36
127	24	36
127	127	24
128	126	24
36	24	127

2) Weight calculation block values.

276	550	786
516	573	1060
767	773	826
344	476	1043
24	280	135

3) Leader cell1 output

The Leader threshold value is taken as 1000.

0	0	0
0	0	1
0	0	0
0	0	1
0	0	0

4) Local excitation block output

The Local threshold value is taken as 200.

1	1	1
0	1	1
0	0	1
0	0	1
0	1	0

5) Segregation: Label output

Segregation threshold is taken as 10.

1	0	0
0	1	0
0	0	1
0	0	1
0	1	0

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6) Segregation: Segmented output 1.

```
24   255  255
255  24   255
255  255  24
255  255  24
255  24   255
```

7) Leader cell 2 output (Second pass)

```
2    0    0
0    2    1
0    0    2
0    0    2
0    2    0
```

8) Local excitation output

```
2    1    1
0    2    1
0    0    2
0    0    2
0    2    0
```

9) Segmentation: Label output

```
2    1    1
0    2    1
0    0    2
0    0    2
0    2    0
```

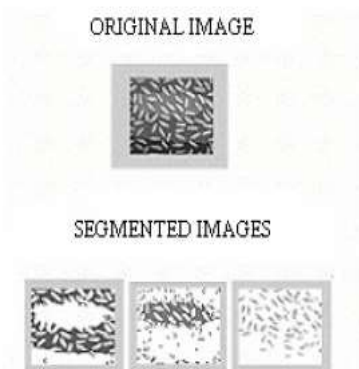
10) Segmentation: Segmented output 2.

```
255  36   36
255  255  36
255  255  255
255  255  255
255  255  255
```

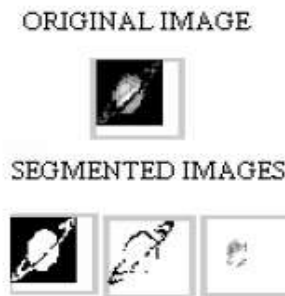
Similarly this flow repeats the segmentation number of times.

### 5. SEGMENTATION RESULTS

In the following images, the top one represent original images and bottom three represent segmented images







**Figure 4.** Gray Scale Image.

## 5. CONCLUSION

In this paper image is segmented by slightly modifying the LEGION approach. Here the analog technique of LEGION is converted into digital technique. And the architecture of the above algorithm is realized in FPGA...Using Model-sim 5.8 C tool the architecture is simulated and using Xilinx 6.3 the architecture is synthesized. The segmented images are verified by using Matlab tool.

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