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Effects of (0.01Ni-PVA) interlayer, interface traps (D_{it}), and series resistance (R_s) on the conduction mechanisms(*CMs*) in the Au/n-Si (*MS*) structures at room temperature

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ABSTRACT: In order to determine effects of interlayer, D_{it}, and R_s on the CMs, both Au/n-Si and Au/(0.01Ni-PVA)/n-Si (*MPS*) structures were fabricated on the n-Si wafer and their electrical parameters were extracted from the current-voltage (*I-V*) and capacitance-voltage (*C-V*) measurements. The ideality factor (n), zero-bias barrier height (Φ_{Bo}), rectifying rate (*RR* at ±5V), R_s, shunt resistances (R_{sh}), and density of D_{it} (at 0.40eV) values were found from the *I-V* data as 1.944, 0.733 eV, 3.50×10^3, 64.8 Ω, 0.23 MΩ, $1.62\text{x}10^{13}$ $eV^{-1}cm^{-2}$ for *MS* and 1.533, 0.818 eV, 1.15×10^7, 5.0 Ω, 57.5 MΩ, $8.82\text{x}10^{12}$ $eV^{-1}cm^{-2}$ for *MPS*. Fermi energy (E_F), barrier height ($\Phi_B(C\text{-}V)$), depletion-layer width (W_D) values were obtained from the *C-V* data as 0.239 eV, 0.812 eV, $1.14\text{x}10^{-4}$ cm for *MS* and 0.233 eV, 0.888 eV, $9.31\text{x}10^{-5}$ cm for *MPS*. These results indicated that the *MPS* structure has lower R_s, D_{it}, leakage current and higher *RR*, R_{sh}, *BH* compared with *MS* and so this interlayer can be successfully used instead of conventional insulator interlayer. The Ln(I)-Ln(V) plot at forward-bias region has three linear parts corresponding to the low, intermediate, and higher voltages. In these regions; conduction mechanism (*CM*) is governed by ohmic, trap charge-limited current (*TCLC*) and space charge-limited current (*SCLC*), respectively.

Keywords: Comparison of the *MS* and *MPS* structures, Polymer interlayer, Conduction mechanisms (*CMs*), Energy dependent interface trap density,

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INTROUCTION

Today, the main scientific and technical problems of metal-semiconductor (MS) structures or Schottky diodes (SDs) with and without an oxide or organic/polymer is relevant to the improving quality/performance of them by reduce unwanted interface traps/states (D_{it}), series resistance (R_s), and leakage current. However a complete description of CMs of them through barrier and understanding the nature of barrier-height (BH) between metal and semiconductor still remain a challenging problem yet. Since interfacial oxide or polymer layer is higher than a few hundred angstroms, MOS/MIS and MPS structures transforms to capacitor. These structures contain a native or deposited interlayer sandwiched a metallic rectifier/gate and metallic ohmic contact and can be stored mores electric charges or energy. In recent years, polymers/organic materials are used widely in industrial applications such as electronic/electrochromic equipment's such as SDs, light-emitting diodes (LEDs), photo diodes (PDs), and field effect transistor (FETs) because of their good flexible, easy processing, and low molecular weight, low cost when compared to the traditional oxide interlayer. (Abthagir and Saraswathi, 2001; Gupta and Singh 2004; Yeriskin et al., 2011; Gokcen et al., 2012; Akhlaghi et al., 2018; Badali, et al., 2018; Çetinkaya et al., 2018).

Among polymer materials, PVA is more interesting due to its high dielectric constant, good charge storage capacity, and solubilized crystalline structure polymer in water and can be acquired industrially by the alkaline hydrolysis of solutions of poly(vinyl acetate) (PVAc) due to hydrogen bonds between hydroxyl groups on the chain and water molecules. Therefore, in this study, (0.01Ni-PVA) solution was grown on the n-Si wafer by electrospinning method which has some advantages compared with the spin coating such as cost effective and easier for us. First, during the electrospinning process, metal can be dispersed homogenously in polymeric material. Additionally, nano-sized particles (nanofibers) are produced instead of micro-sized materials via electrospinning technique. Moreover, semiconductor wafers can be coated more uniform compared with spin coating.

The performance of MS, MIS and MPS structures are depend on the existence of D_{it} level, BH and interlayer inhomogeneity at M/S interface, and R_s of them (Card and Rhoderick, 1971; Sze, 1981; Sharma, 1984). In this respect, it is more important, the investigation effects of D_{it}, interlayer, and R_s on the performance of these structures. An insulator layer formed by the traditional methods at M/S interface cannot passivate the active dangling-bonds at surface. Therefore, in the last two decades, high-dielectric materials such as ferroelectric and polymer composites began used instead of insulator layer to increase quality of MS (Demirezen et al., 2012; Durmuş et al., 2013; Reddy, 2014; Reddy et al., 2014; Ersoz et al., 2016; Yeriskin et al., 2017; Ulasan et al., 2018). Such doped metal in the polymer leads to increases of the conductivity due to high physical interactions between organic polymer chains, via H-bonding at hydroxyl dopant materials interface and so the conduction mechanisms become quite different from the classic MS structures (Demirezen et al., 2012; Yeriskin et al., 2017).

The main goal of this study is to determine the effects of (0.01Ni-doped PVA) interlayer, interface traps (D_{it}), and series resistance (Rs) on the (CMs) and performance of MS and MPS structures. For this purpose, both the MS and MPS structures were fabricated on the same n-Si wafer and their main physical parameters were obtained from the I-V and

C-V data and obtained results compared. Experimental results show that the MPS type structure has lower R_s, D_{it}, leakage current and higher RR, R_{sh}, BH when compared with MS structure. The double-logarithmic I-V plot shows three linear regimes with different slopes which correspond to the low, intermediate, and higher bias voltages and in these regions current transport governed by ohmic, TCLC, SCLC mechanisms, respectively.

MATERIALS AND METHODS

The Au/(0.01 Ni-doped PVA)/n-Si structures were performed on the Phosphor-doped Si (n-type) wafer with (100) orientation, 5.08 cm diameter, 1-5 Ω.cm resistivity and 280 μm thickness. Firstly, wafer was cleaned with RCA cleaning procedure in the ultrasonic bath and after rinsed deionize-water with 18 Ω.cm it dried with N_2 gas. Immediately, the cleaned n-Si was transferred in the vacuum chamber to perform back ohmic contact. Secondly, high-pure (99.999%) Au metal with 120 nm thick was evaporated onto the back side of n-Si wafer at 10^{-6} Torr and then was annealed at 500 °C in nitrogen ambient at 5 minutes to get low-resistivity ohmic contact. After that the prepared (0.01 Ni-PVA) solution was grown on the wafer using electrospinning-method. Finally, the circular dots with $7.85x10^{-3}cm^2$ and 120 nm thickness of high-purity Au rectifier contacts were evaporated on the (0.01 Ni-PVA) interlayer. In this way, the performed processes of Au/(0.01 Ni-d PVA)/u-Si structures were completed. For electrical measurements, the fabricated MS and MPS structures were pasted onto the Cu-holder by a silver dag. Through an IEEE-488 AC/DC converter card, the I-V and C-V measurements were fulfilled by utilizing a source-meter (Keithley 2400) and an impedance analyzer (HP 4192 A LF), respectively.

RESULTS AND DISCUSSIONS

A. Current-Voltage (I-V) Characteristics

The ln(I)-V plots of the MS and MPS structures were drawn to determine the influence of (0.01Ni-doped PVA) interlayer, D_{it}, and R_s series resistance on the on the CCMs and presented in Fig. 1. It is clear that the ln(I) vs V plot of the MPS structure has a good rectifier behavior, i.e. while the value of current is almost independent from the voltage in the reverse bias region and it increases as exponentially with increasing voltage in forward bias region when compared with MS structure. However, lnI-V plot of the MS structure is quite deviated from the linearity for high-voltages ($V \geq 0.5V$) due to the effect of high R_s rather than MPS structure. The relation between I and V for these structures on the base of thermionic emission (TE) theory ($V \geq 3kT/q$) is given as follow (Sze, 1981; Sharma, 1984)

$$I = AA^{*}T^{2}\exp\left(-\frac{q}{kT}\Phi_{Bo}\right)\left[\exp\left(\frac{q(V-IR_s)}{nkT}\right)-1\right] \quad (1)$$

In Eq.1, A^* is the Richardson constant (112 $A/(cm^2K^2$ for n-type Si), A is the diode area (7.85 $x10^{-3}$ cm^2), and I_o in the front of brackets is the reverse-bias saturation current.

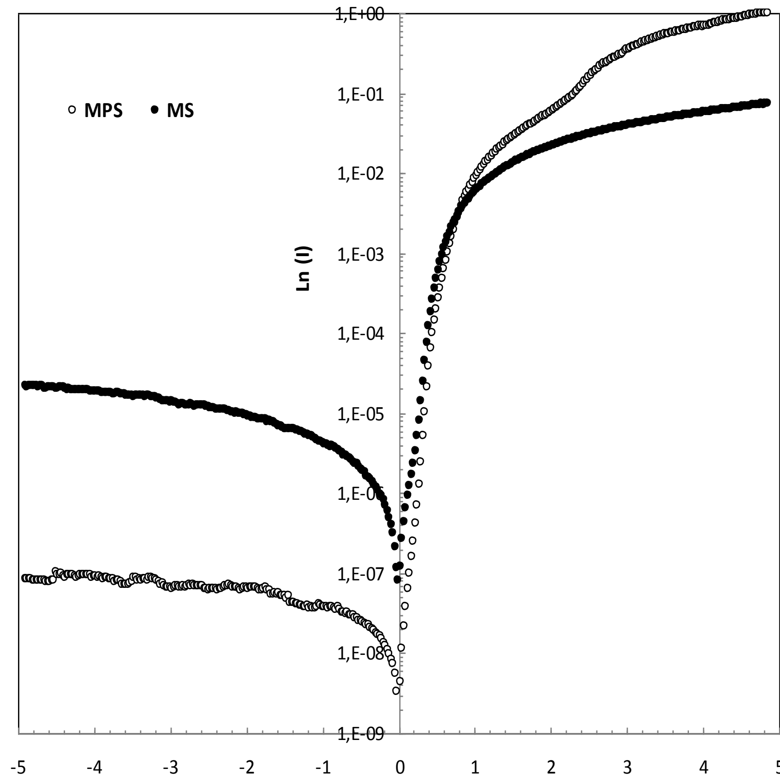

Figure 1. The semi-logarithmic I-V plots for the Au/n-Si and Au/(0.01Ni-PVA)/n-Si structures.

Both the I_o and n values for MS and MPS structures were estimated from the intercept and slope of the linear part Ln(I)-V plot, respectively, through the relation.

$$n = \frac{q}{kT}\left(\frac{dV}{d(\ln I)}\right) \quad (2a)$$

$$\Phi_{Bo} = \frac{kT}{q} Ln\left(\frac{AA^{*}T^{2}}{I_0}\right) \quad (2b)$$

The I_o, n, Φ_{Bo}, and RR values were found from the linear regions of the ln(I)-V plots as 3.97x10^{-8}A, 1.944, 0.733 eV, 3.50×10^{3} for MS and 1.46x10^{-9} A, 1.533, 0.818 eV, 1.150×10^{7} for MPS structure, respectively. The of R_s and R_{sh} value were also determined from the Ohm's law (Ri=dVi/dIi) which are corresponding to the enough high forward (+5V) and enough low reverse (-5V) bias voltage, respectively. They were found as 64.8 Ω and 5.0 Ω for MS, and 0.23 MΩ and 57.5 MΩ for MPS structure, respectively. All these experimental electrical parameters which are determining the performance or quality of these structures were given in Table 1.

Table 1. The obtained some main experimental I_o, n, Φ_{Bo}, R_s, R_{sh}, RR, and D_{it} values for the MS and MPS structures at room temperature.

Samples	I_o (A)	n	Φ_{Bo} (eV)	R_s at 5V (Ω)	R_{sh} at 5V (MΩ)	RR at ±5V (I_F/I_R)	D_{it} at 0.4 eV ($eV^{-1}.cm^{-2}$)
MS	3.97×10^{-8}	1.940	0.733	64.8	0.23	3.50×10^{3}	1.62×10^{13}
MPS	1.46×10^{-9}	1.533	0.818	5.0	57.5	1.15×10^{7}	8.82×10^{12}

It is clear that the value of n for MS and MPS is higher than unity due to the native (SiO_2) and grown (0.01Ni-PVA) interlayer, interface traps, image-force lowering, generation-recombination, tunneling through the BH or via traps, and the presence of some patches or lower-barriers at M/S interface (Werner et al., 1988; Durmus et al., 2013; Alialy et al., 2015; Tan, 2017). In other words, the existence of the barrier inhomogeneity which contains low-BHs or patches leads to an increase in the value of n. The double-logarithmic I-V plots for the MS and MPS structures were drawn to determine the possible CMs in the whole forward bias regime were given in Fig. 2.

It can be clearly seen in Fig.2, these plots show three different linear parts with different slopes (m) for the MS and MPS structures obey power-law behavior ($I \sim V^m$) (Aydogan et al., 2005). For part I, the values of m were found as 1.32 for MS and 1.80 for MPS type structures which are lower than and so imply the ohmic conduction is dominate for lower voltages. This is a result of the insertion of charge-carriers from the electrode into the p-Si (Forrest, 1997). For part II, the values of m were found as 6.67 for MS and 8.29 for MPS type structures which are much higher than the unity or two and so imply the CM is governed by the TCLC with an exponential interface trap distribution because of an increase in amount of injected-electrons causes filling of traps and increase of the space charges (Ocak et al., 2009). For part III, the values of m were found as 2.76 for MS and 4.41 for MPS type structures which indicate that the device moves towards "trap-filled" limit because of the electrons injection, which are escape from the traps and contribute to the SCLC (Yeargan and Taylor, 1968; Nagaraju, 2017).

Usually, many defects/impurities can be occurred at M/S interface during the elaboration of these MS and MIS or MPS structures. All these defects are called as interface states/traps (N_{ss} or D_{it}) and they can alter the quality of these devices. These traps can be also originated dangling bounds depend on the chemical composition of the interface between inter-layer and semiconductor (Card and Rhoderick, 1971; Sze, 1981; Sharma, 1984; Reddy, 2014; Yerişkin et al., 2017). Therefore, a special density distribution of these traps was obtained from the forward bias I-V by considering the V-dependent BH and n both MPS and MPS structures and represented in Fig. 3. According to Card and Rhoderick (1971), n and effective BH (Φ_e) values in the forward bias region are function of voltage due to the existence of interlayer, D_{it}, and barrier in-homogeneities.

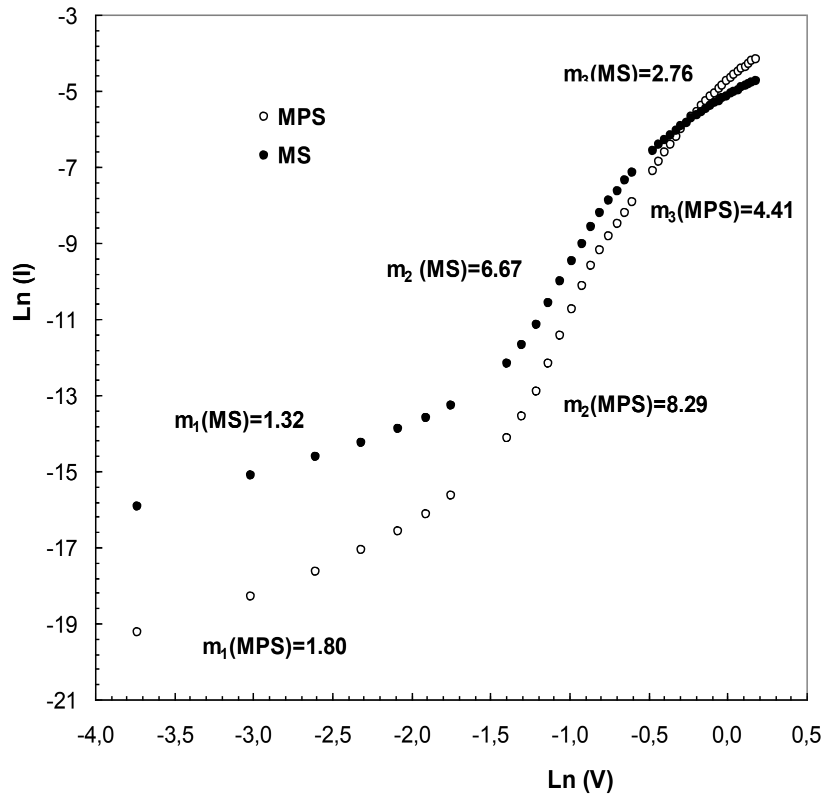

Figure 2. The double-logarithmic forward bias I-V plots for the MS and MPS structures.

$$n(V) = \frac{qV}{kT.Ln(I/I_o)} = 1 + \frac{\delta}{\varepsilon_i}\left[\frac{\varepsilon_s}{W_D} + qN_{ss}(V)\right] \tag{3a}$$

$$\Phi_e = \Phi_{Bo} + \alpha\,(V) = \Phi_{Bo} + \left(1 - \frac{1}{n(V)}\right)V \tag{3b}$$

In Eq. 3 (a) and (b); the quantities of α (=dΦe/dV), W_D, ε_s, and ε_i are the voltage coefficient of the BH, the depletion layer thickness, the dielectric of semiconductor and inter-layer, respectively. In addition, the energy of traps (E_{ss}) for n type semiconductor are estimated with respect to the E_c of it is given as Eq.4 (Card and Rhoderick, 1971; Sze, 1981).

$$E_c - E_{ss} = q(\Phi_e - V) \tag{4}$$

Thus, the N_{ss} vs (E_c - E_{ss}) profiles of the MS and MPS structures and represented in Fig.3. It is clearly that the values of interface traps show an exponential growth from mid-gap of Eg towards the bottom of Ec. The values of N_{ss}/D_{it} at 0.40 eV was found as 1.62×10^{13} $eV^{-1}cm^{-2}$ for MS and 8.82×10^{12} $eV^{-1}cm^{-2}$ for MPS, respectively.

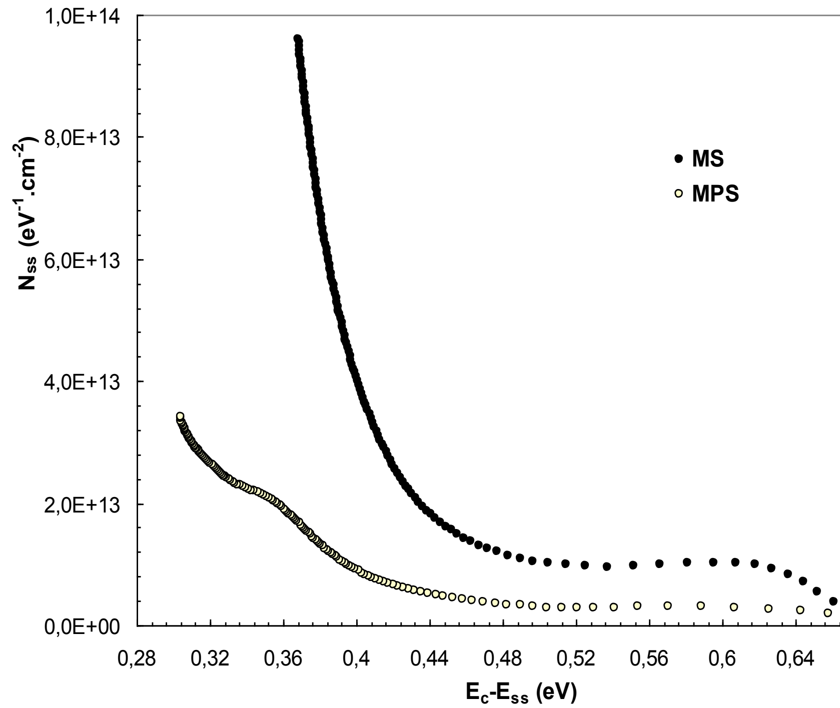

Figure 3. The energy-dependent profile of Dit for the MS and MPS) structures.

As can be clearly seen in Fig.3, the magnitude of D_{it} for the Au/(0.01Ni-PVA)/n-Si (MPS) structure is considerably lower than the MS structure in the whole band gap of semiconductor because of the saturation dangling-bonds by (0.01Ni-PVA) polymer layer. Similar results have been reported by Gökçen et al., (2012) in the Au/(Co-PVA)/n-Si, Badali et al., (2018) in the Ag/(Ru-PVP)/n-Si, Yerişkin et al., (2017) in the Au/(graphene-PVA)/n-Si, and Reddy et al., (2014) in the Au/PVDF/n-InP (MPS) structures.

B. Capacitance-Voltage (C-V) Characteristics

The experimental C-V plot of the MS and MPS structures at 1 MHz were given in Fig. 4. It is clear that the C-V plot show a peak behavior for both the MS and MPS structure. But, the observed two peaks for the MPS structure is the result of a special distribution of D_{it} in the bend gap of Si. These anomalous peaks in the forward bias C-V curves was also observed by various researchers and usually it was attributed to the existence of D_{it}, R_s, and minority-carrier injection in the literature (Werner et al., 1988; Lin et al., 2008; Bilkan et al; 2015; Kaya, 2015; Orak and Koçyiğit, 2016; Taşçıoğlu et al., 2017; Yeriskin et al., 2017; Karabulut, 2018).

Here, N_c is the effective density of states in the conduction band of Si ($2.8x10^{19}$ cm^{-3} for n-Si). The value of W_D was also calculated by using N_D and V_D (=Vo+kT/q) by using the following relation (Sze, 1981).

$$W_d = (2\varepsilon_s\varepsilon_o V_d/qN_D)^{1/2} \quad (7)$$

As can be seen in Fig.5, the existence of native or deposited inter-layer and interface traps leads to a large intercept of intercept voltage. In this case, the obtained higher value of BH can be

modified by using the c_2 (=N_D(exp.)/N_D(theor.)) constant which is the ratio of the obtained experimental value of N_D(exp.) to its theoretical value N_D(theor.) as following form (Card and Rhoderick, 1971).

$$1/n \approx c_2 = \varepsilon_i/(\varepsilon_i + qN_{ss}) \quad (8)$$

Thus, the value of Φ_B(C-V) was calculated for the fabricated MS and MPS structure as follow:

$$\Phi_B(\text{C-V}) = (c_2 Vo) + kT/q + E_F \quad (9)$$

The obtained V_o, N_D, E_F, W_D and Φ_B(C-V) values from the C^{-2}-V plot were given in When Table 1 and 2 are compered, the value of Φ_B(C-V) is higher than the Φ_B(I-V) almost as E_F level due to the nature of measure method and so voltage dependent of BH.

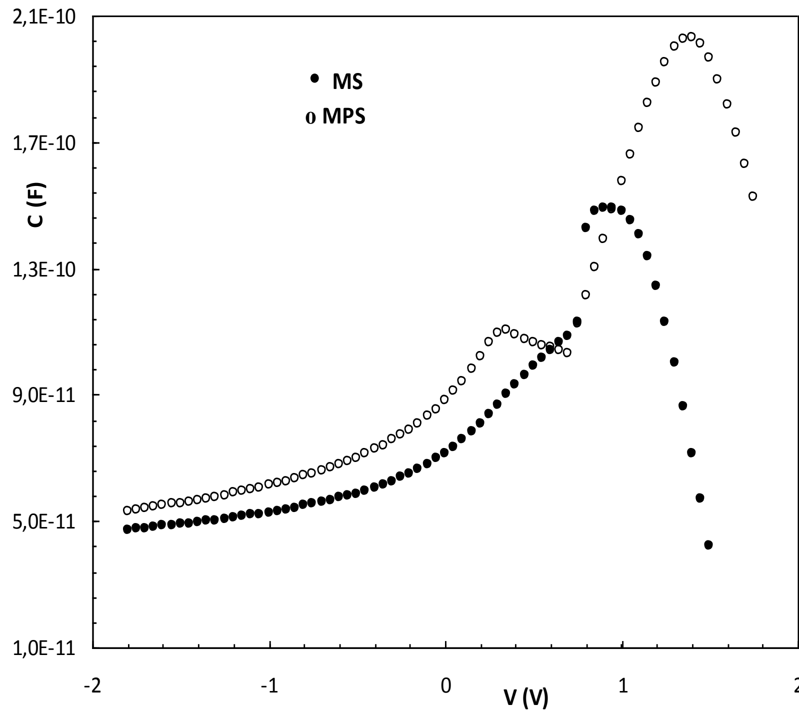

Figure 4. The C-V plots for the MS and MPS structures.

Table 2. The qV_o, N_D, E_F, W_D, c_2, Φ_B(C-V), and D_{it} values of the MS and MPS structures.

Samples	qV_o (eV)	N_D (cm^{-3})	E_F (eV)	W_D (cm)	c_2	$n \approx 1/c_2$	Φ_B(C-V) (eV)	D_{it} at 0.4 eV (eV^{-1}.cm^{-2})
MS	0.970	$9.77\text{x}10^{14}$	0.239	$1.14\text{x}10^{-4}$	0.565	1.77	0.812	$0.83\text{x}10^{13}$
MPS	0.849	$1.28\text{x}10^{15}$	0.233	$9.31\text{x}10^{-5}$	0.743	1.35	0.889	$1.96\text{x}10^{12}$

Additionally, the value of D_{it} was calculated from the Eq.8 for MS and MPS structure and was also given in Table 2. It is clear that the values of D_{it} for the MPS structures are lower than the MS structure. In conclusion, all these experimental results are confirmed that the use of (0.01Ni-PVA) interfacial organic layer at Au/n-Si (MS) interface leads to an increase the performance of the Au/n-Si (MS) structure in respect of lower values of R_s, N_{ss} or D_{it}, leakage current and higher values of RR, R_{sh}, BH, and capacitance. The high values of capacitance is also means that more and more electronic charges or energy storage capacity. Therefore, it can be successfully used an alternative to the oxide layer.

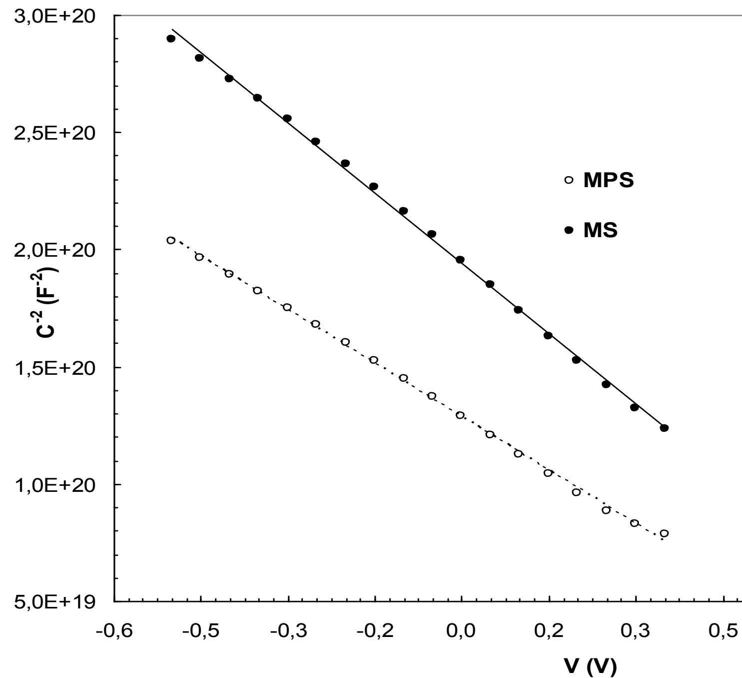

Figure 5. The C^{-2}-V plots for the MS and MPS structures.

CONCLUSION

In order to determine the effects of (0.01Ni-PVA) interlayer, D_{it}, and R_s on the CMs, both the Au/(0.01Ni-PVA)/n-Si and Au/n-Si structures were performed on the same n-Si wafer and then their main electrical parameters obtained from the I-V and C-V measurements. The obtained experimental value of BH from the C^{-2}-V plots for MPS and MS structures were found higher than those from forward bias Ln(I)-V plots because of the nature of measurement method and voltage dependent. The RR ($=I_F/I_R$) for MPS structure 3286 times higher than MS structure. The Ln(I)-Ln(V) plot was also drawn and they have three linear regimes for low, intermediate, and higher voltages and in these regimes CM is governed by ohmic, TCLC, and SCLC, respectively. The experimental values of D_{it} for the MPS structures were obtained both the I-V and C-V data were also considerably lower than MS structure. The obtained all experimental results are confirmed that the (Ni-doped PVA) organic layer causes

quite decrease in the values of D_{it} and R_s and increase in R_{sh}, RR and BH. In conclusion, (Ni-PVA) inter-layer can be successfully used an alternative to the oxide layer regarding the enhancements in device parameters.

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