Research Article GU J Sci 32(2): 572-580 (2019)

Gazi University

Journal of Science

http://dergipark.gov.tr/gujs

Temperature-Aware X-filling for Very Large Scale Integrated Circuits

Thilagavathi KARUNAMURTHY[1], Sivanantham SATHASIVAM[1,*]

[1]*School of Electronics Engineering, Vellore Institute of Technology, Vellore-632014, India*

Article Info

Received: 05/06/2018
Accepted: 12/11/2018

Keywords

Hotspot
X-Filling
Thermal-Uniformity
Test Power
Peak Temperature

Abstract

The excess switching activity during testing increases the power dissipation beyond the normal operation of the circuit. The non-linear power distribution creates localized heating called hotspot which results in the structural damage and increased cooling package cost. The temperature of a particular block depends on heat generation and dissipation of the circuit blocks. The uniformity in power distribution among the circuit blocks is the key requirement for temperature reduction. The unspecified bits present in the test patterns are utilized to reduce the switching activity during testing. In this paper, we present an event-driven based power analysis and temperature aware X-filling to reduce the total power dissipation among the circuit blocks in such a way to reduce peak temperature. To reduce the peak temperature, the power dissipation of each block is monitored with the help of fillings the X-bits. The experiments are carried out with the ISCAS'89 benchmark circuit and show a significant reduction in peak temperature and ensure uniform power distribution during testing.

1. INTRODUCTION

Advances in semiconductor manufacturing technology bring complex System-on-Chip (SoC) design with high transistor density and reduced feature size [1]. It increases the clock frequency for high performance and entails the excessive power dissipation during testing [2]. It is mandatory to reduce the power dissipation during testing as it tends to increase the yield loss and cooling package cost due to circuit overheating. However, the reduced power dissipation is not uniformly distributed among the circuit blocks which increase the heat generation. There should be equilibrium condition between heat generation and heat dissipation of circuit. The reduced power dissipation is in greater saving in heat generation but the heat dissipation depends on the thermal gradient which is the function of the circuit and ambient air. The excessive test power dissipation increases the heat generation rapidly hence increased peak temperature. The peak temperature causes localized heating called a hotspot. As the increase in hotspot count greater in cooling package cost and structural damage [3]. The peak temperature reduction during testing is necessary for SoC design. The transition reduction is no longer sufficient to reduce the peak temperature as it requires power reduction with respect to the spatial distribution. The temperature of a block highly depends on the power dissipation of that block. The uniform power density of blocks is the major concern for uniform temperature distribution which minimizes the peak temperature.

Various techniques are available to reduce the temperature during testing which can be reducing the temperature difference up to Celsius [4]. The low power testing techniques are suitable for peak temperature reduction such as test vector reordering, scan cell/chain reordering, X-filling, power-aware Automatic Test Pattern Generation (ATPG), and power-aware Design for Testability (DFT) [2]. Thermal-aware scan cell reordering is presented in [5] based on overheat pre-compensation. The global scan vector order is selected based on hotspot prediction. The temperature aware test vector reordering is presented in [6]. The X-bits are filled to reduce the overall power dissipation of the circuit for temperature reduction. The overall power reduction is not enough for the linear temperature distribution in shrinking feature size and device density

*Corresponding author, e-mail:ssivanantham@vit.ac.in

[7]. The power density of each block has to be considered to minimize the temperature differences of the circuit. Another X-filling is proposed to reduce the power dissipation of each block based on the criticality of every test sets [8]. The flip-flop switching activity has a major impact in every block; it decides the power density which is referred to as critical flip-flops. The criticality is used to calculate the power density with respect to the switching activity of critical flip-flops. The entire test sets are filled with existing X-filling techniques [9-11] and choose the best test sets for thermal-aware filling. The identification of critical flip-flips and back-tracing X-bits is very difficult for complex SoC design.

The existing low power X-filling techniques do not reduce the switching activity in a uniform manner [10] [16] [19]. The switching transitions for different X-filling techniques presented in Table 1. It is obviously noted from Table 1, the switching transitions are not reduced uniformly hence non-uniform power distribution across the circuit blocks with respect to any particular X-filling. It is clear that one X-filling approach is not sufficient for uniform power distribution which in turn affects the temperature variation of the circuit. However, one filling technique is suitable for a reduction in overall total power dissipation during testing. In this paper, we present the X-filling algorithm which considers all existing X-filling for every circuit to obtain uniform power distribution. The power density of every block is monitored using event-driven power analysis. The contribution of this paper as follows,

Table 1*.Comparison of scan-in average power results of existing X-filling techniques*

Circuits	Original Test sets	0-filling	1-filling	4m-filling	MT-filling
S5378f	13476	3336	3085	3796	2435
S9234f	22268	5692	5870	5511	3466
S13207f	136262	12416	16319	6710	7703
S15850	204830	12742	26503	14209	13381
S38417	1275445	172665	174770	142560	112198
S38584	1027407	136634	149640	117550	88298

- A unique power simulator for calculating the power density of each block. The power simulation is event driven where every event is considered as a test pattern. The power density is determined whenever the test pattern is applied to the circuit. It provides accurate power values obtained from commercial tools.

- Every pattern is filled with four different X-filling techniques such as 0-filling [9], 1-filling [9], Minimum Transition (MT) filling [11], and 4m filling [10]. The fitness function decides the low power density test pattern. It iterates for all the test patterns for every circuit. It does not require any flip-flop information and back-tracing for X-bit. The completely filled test patterns ensure uniform power density of each block and apply for thermal simulation.

- The uniform power distribution has a major impact on heat generation which reduces the peak temperature compared to previous methods. The proposed thermal-aware filling is validated with the ISCAS'89 benchmark circuit and provides a significant reduction in peak temperature.

The layout of this paper is as follows, section 2 describes the thermal simulation, section 3 describes the thermal-aware X-filling algorithm, section 4 describes the experimental results, and section 5 concludes this paper.

2. OVERVIEW OF THERMAL SIMULATION

2.1. Thermal Simulator

The heat conduction from package to heat sink and heat convection from heat sink to ambient air are the dominant factors for the temperature at the die level. The duality present between heat transfer and electrical phenomena. Heat flow is referred to as the current which is passing through a thermal resistance and tends

to calculate temperature difference is equal to voltage. The thermal resistances are enough to calculate the steady-state behavior whereas thermal capacitance is needed to calculate dynamic behavior. Thermal capacitance determines delay before temperature changes to a steady state when power changes simultaneously. In SoC design, each physical component is referred to as heat storage capacitance and thermal resistance which are transfers heat through the ambient air with other components. Thermal capacitance and thermal resistance are referred to as C_{th} and R_{th} respectively. Hotspot [13] is a thermal simulator which provides duality between electrical, thermal resistance, and thermal capacitance among the circuit blocks. It is used to calculate the transient and steady state temperature based on architectural level and electro-thermal modeling. The junction temperature T_j is depended on ambient temperature T_a and power dissipation of chip P_{chip} as shown in Equation 1.

$$T_j = T_a + P_{chip} R_{ja} \tag{1}$$

The Hotspot [13] requires power and floor plan information of each block present in the circuit and outputs the temperature variance of the circuit. The specification for the chip, heat sink, heat spreader, and interface materials are given by Hotspot in the configuration file.

2.1.1. General Flow of Thermal Simulator

The thermal simulation is performed with the help of different commercial tools for a set of test patterns of the circuit. The following steps are involved in Figure 1.

- The test patterns are generated using Mintest combinational ATPG [12] with unspecified bits.
- The unspecified bits are filled using a thermal-aware X-filling algorithm presented in Figure 3.
- The scan inserted synthesized gate-level netlist is generated from Synopsys DFT Compiler [17] where normal D flip-flops are converted into scan flip-flops with TSMC 65nm technology.
- The scan inserted gate-level netlist is given to Cadence Modus to generate the floor plan file from RTL-to-GDS II which provides the block information of the circuit as a *.def* file.
- The scan inserted netlist and filled external Mintest pattern is applied to Tessent Fastscan for external pattern fault simulation.
- A power simulator is an event-driven simulator. It takes switching activity of each pattern and scan inserted netlist as inputs which are designed using Synopsys Power Compiler with TSMC 65nm technology. It provides the power dissipation of each block present in the circuit with respect to every test pattern. The power values are taken from the technology library provided during synthesis.
- The power information of each block and floor plan information is given to Hotspot [12] as inputs. It generates the steady-state and transient temperature for each block.

3. THERMAL-AWARE X-FILLING

This section presents a thermal-aware X-filling to minimize the temperature variation of the circuit. The test pattern with X-bits gives the flexibility for a reduction in power, test data volume, and temperature without compromising the fault coverage. The power dissipation in VLSI circuits is in different types such as a static, dynamic, and short circuit. The dynamic power depends on the supply voltage, clock frequency and switching activity as shown in Equation 2. The supply voltage and clock frequency have already been utilized for power reduction at the design cycle which affects the circuit performance if these are changes during testing. Due to this reason test engineer focused on reducing switching activity for test power reduction. The switching activity is calculated based on charging and discharging of the output load capacitance.

$$P_d = 0.5 \times C_{load} \times \left(\frac{V_{DD}^2}{T_{cyc}}\right) \times N_G \tag{2}$$

where C_{loud} is load capacitance, V_{DD} is the supply voltage, T_{cyc} is the global clock period, and N_G is the number of transition at gate output. The reduced switching activity of the test pattern is a promising solution for low power testing. Moreover, the switching activity of the test pattern with respect to each block has to be considered for thermal-aware testing. The proposed filling considered the power information at the block level for filling the X-bits. We proposed event driven power simulator to calculate the power dissipated at each block when applying the filled patterns. The proposed power simulator values are accurate which are taken from Synopsys Power Compiler [18]. The following section elaborates the power simulator designed for thermal-aware X-filling.

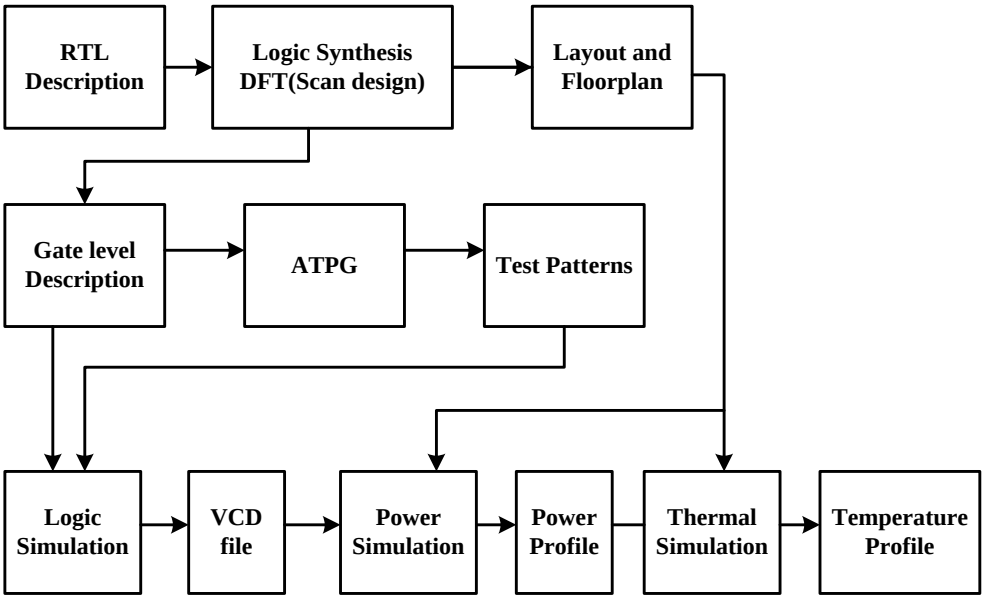

Figure 1*.General Flow of Thermal Simulation*

3.1. Event-Driven Power Simulator

The proposed power simulator is event-driven simulator where the event belongs to a test pattern. Whenever changes happen in the event, it will report the total power dissipation of circuit and individual power values of each block. The power simulator is automated using Perl script which takes the input of scan inserted netlist and switching information of test pattern. It integrates the two different commercial tools with the help of an automated script. The fault simulation is carried out using Tessent Fastscan with completely filled external patterns and generates a test bench for each pattern. The switching information is recorded using Synopsys VCS compiler which takes test bench obtained for a particular test pattern, scan inserted gate-level netlist and technology library as inputs. Next step is to calculate power values at block level with the help of Synopsys Power Compiler; it takes recorded switching activity of a test pattern and the circuit as inputs. It generates the hierarchical power report at the block level. The proposed power simulator is less time to consume and adopted for any circuit. This power simulator is applicable for both single scan chain design and multiple scan chain design because it requires only test pattern and corresponding switching activity at the block level.

3.2. X-filling Algorithm

It is well known that the X-bits are exploits for temperature reduction with desired fault coverage. The test patterns are generated externally and applied to the circuit during scan testing to capture the total power dissipation. The circuit has been divided into multiple blocks. Each block contains flip-flops and gates. The power dissipation of each block decides the power density of that block. If the power density is uniformly distributed then the heat generation and heat dissipation attain equilibrium condition; it leads to reduce the temperature variation among the circuit blocks. The proposed algorithm assigns weighted power to each test pattern which is determined using the ratio of the total power dissipation of the circuit for a particular test pattern or test set and individual block power dissipation. The total power dissipation is referred to as

P_{tot} of circuit and power dissipation of block b_j is referred to as P_{bj}. The weighted power W_p is described for test pattern t_i with respect to block b_j in Equation 3.

$$W_{Pi} = \sum_{j=1}^{m} \frac{P_{tot}}{P_{bj}} \tag{3}$$

Initially, the test patterns are filled with existing low power X-filling techniques such as 0-filling [9], 1-filling [9], MT-filling [11], and 4m filling [10] which are circuit and technology independent. The X-bits are mapped with 0's and 1's using 0-filling and 1-filling respectively. The MT-filling is filled X-bit with left most specified bits of every X-bits. The 4m filling is recently proposed for test data volume reduction in which X-bits are divides in multiples of *4* and mapping the X-bits with adjacent specified bits to increase the correlation [10] algorithmically. To increase the correlation between the test patterns further, we can divide the X-bits in multiples of 2^n. Table 2 illustrates the four different X-filling with the example.

Table 2. *Example of different X-filling techniques*

Test sets: 00101000110XX100011011X01XX01X10XX1XXXXX	
0-filling	0010100011000100011011001000101000100000
1-filling	0010100011011100011011101110111011111111
4m-filling	0010100011011100011011001000111011111111
MT-filling	0010100011000100011011101110111000111111

The proposed X-filling algorithm is explained in Figure 1 . Based on *N* values, the filling is chosen for every test pattern. Every pattern is filled with this four different X-filling and produces a completely specified test pattern. The power dissipation is calculated for each test pattern filled by different X-filling from power simulator. The weighted power is assigned for different filling using equation 3. The proposed algorithm is searching *Maxima* and it is computed using fitness function in equation 4, where the maximum value of weighted power among the X-filling techniques is selected; it tends to provide the low power density at the block level. Hence, the uniform power distribution is achieved among the circuit blocks for the corresponding test pattern. The process is repeated for all the test pattern. Every filled test pattern is validated not only switching transitions and also power information at the block level. The fitness function is calculated using equation 4.

$$Fitness\ Function = Max\left(\sum_{i=1}^{N} W_{Pi}\right) \tag{4}$$

In the proposed algorithm, X-bits are filled with 0-filling if *N=1* and calculates the weighted power for that test pattern. The variable *temp* is initialized with zero. If the weighted power of 0-filling is greater than *temp*, then it replaces with weighted power. The same test pattern is filled by 1-filling and calculates the weighted power. If the 1-filling weighted power is greater than *temp* value, it updates with 1-filling. The above-said process is repeated for other X-filling techniques for every pattern. The algorithm outputs the completely filled test pattern with maximum weighted power. Then, the test pattern and corresponding power values are considered for thermal simulation.

The heat generation is reduced with the help of low power density block. The highest value of fitness function ensures that low power density and uniform power distribution across the circuit blocks. The floor plan information of each block is obtained from the commercial tool. The block information and corresponding power values are applied to a thermal simulator for temperature calculation.

```
Input: Test pattern with unspecified bits
T=t0,t1, ...., tm-1, tm, tm+1,...,tn
Output: Completely filled test pattern
1 for N = 1 to 4
2   if N==1 then
3              Fill X-bit with 0's in a test pattern ti
4             Calcute Wpi  for ti
5        if temp < Wpi then
6              set temp = Wpi
7       end
8   end
9    else if N==2 then
10             Fill X-bit with 1's in a test pattern
11             Calcute Wpi  for ti
12       if temp < Wpi then
13              set temp = Wpi
14      end
15  end
16  else if N==3 then
17             Fill X-bit with MT-filling in a test pattern
18             Calcute Wpi  for ti
19       if temp < Wpi then
20              set temp = Wpi
21      end
22  end
23  else if N==4 then
24             Fill X-bit with 4m-filling in a test pattern
25             Calculate Wpi  for ti
26      if temp < Wpi then
27              set temp = Wpi
28      end
29  end
30 end
```

Figure 2. *X-filling algorithm flow*

4. RESULTS AND DISCUSSION

The proposed thermal-aware X-filling and power simulator are evaluated for peak temperature reduction in SoC design. The power simulator is designed using Perl script and X-filling is implemented in C program on Intel core, 2GHz i3 processor, and 2GB RAM. The experiments are verified on the ISCAS'89 benchmark circuit [14]. The test patterns are generated using Mintest [12] ATPG with dynamic compaction.

The test sets are reordered before applying for X-filling. The test patterns are reordered in descending manner such a way that the number of specified bits present at the beginning of test pattern which comes as the first pattern. It is a proven technique explained in power-aware scan cell reordering [15]. The reordered test patterns are applied to the thermal-aware X-filling algorithm. The proposed strategy is capable of reducing the temperature and increase uniform power distribution over the blocks. The X-filling techniques are not limited to only these four techniques considered in this paper. The X-filling technique which does not require any circuit information and modification in the design, and adapted to any SoC design can be utilized for proposed thermal-aware X-filling. Table 3 presents the peak temperature of each circuit for different X-filling techniques [9-11]. From Figure 3, it is clear that a significant reduction in peak temperature is achieved as compared to the existing thermal-aware filling.

Table 3. *Peak temperature for different X-filling against other techniques in Kelvin*

Circuit	0-filling	1-filling	MT-filling	4m-filling	[7]	[8]	Proposed
s5378	520.49	486.03	493.21	510.05	480.12	471.69	458.45
s9234	587.98	667.45	625.99	598.28	550.62	506.22	513.71
S13207	441.62	591.13	577.01	489.34	429.61	402.44	359.92
S15850	485.51	625.53	568.72	482.29	397.2	378.92	364.43
s38417	536.37	548.37	517.99	514.19	472.47	431.97	425.12
s38584	592.03	775.7	663.05	587.61	481.06	468.42	417.52
Avg.	527.3	615.7	574.3	530.2	468.5	443.2	423.1

Table 4. *% Reduction in peak temperature compared to previous techniques*

Circuit	0-filling	1-filling	MT-filling	4m-filling	[7]	[8]
s5378	12	6	7	10	5	3
s9234	15	25	20	17	10	2
S13207	19	39	38	26	16	11
S15850	25	42	36	24	8	4
s38417	21	22	18	17	10	2
s38584	29	46	37	29	13	11
Avg.	20.1	30	26	20.5	10.3	5.5

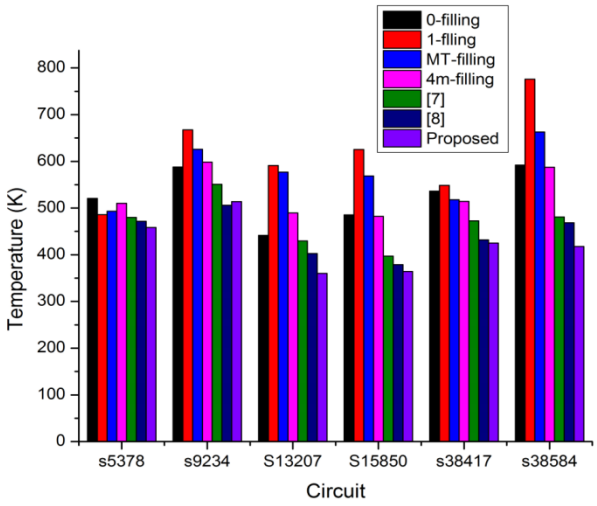

Figure 3. *Peak temperature for different X-filling*

The proposed thermal aware X-filling achieves 20%, 30%, 26%, 20.5%, 10.3%, 5.5%, reduction in peak temperature as compared with 0-filling [9], 1-filling [9], MT-filling [11], 4m- filling [10], [7] and [8] respectively as shown in Table 4.

5. CONCLUSION

We have presented thermal-aware power-uniformity X-filling to minimize the peak temperature and obtain uniform power distribution using fast and accurate event driven power simulator. From the results, it shows that the peak temperature reduction is obtained from 5.5% to 30% as compared to previous methods. This X-filling strategy ensures the uniform power distribution and reduces the excessive heat generation during

test application. The proposed X-filling can be further extended for temperature-aware test data compression since X-bits are the dominant factor in test data volume reduction.

CONFLICTS OF INTEREST

No conflict of interest was declared by the authors.

REFERENCES

[1] Garginie, P., "Roadmap Past, Present and Future", https://linxconferences.com/wp-content/uploads/2016/04/02-01-Gargini- ITRS-2.0-2.pdf/, (2015).

[2] Girard, P., "Survey of low-power testing of VLSI circuits", IEEE Des. test, 19(3): 82–92 (2002).

[3] Girard, P., Nicolici, N., Wen, X., "Power-Aware Testing and Test Strategies for Low Power Devices", 1st ed. Springer Publishing Company, Incorporated, (2009).

[4] Bota, S. A., Rossello, J.L, De Benito, C, Keshavarzi, A., Segura, J., "Impact of thermal gradients on clock skew and testing", IEEE Design and Test of Computers, 23(5): 414–424, (2006).

[5] Cho, M., Pan, D.Z., "Peakaso: Peak-temperature aware scan-vector optimization", Proceedings of IEEE VLSI Test Symposium, (2006).

[6] Dutta, A., Kundu, S., Chattopadhyay, S., "Test vector reordering to reduce peak temperature during testing", Annual IEEE India Conference (INDICON), 1–6, (2013).

[7] Yoneda, T., Nakao, M., Inoue, M., Sato, Y., Fujiwara, H., "Temperature variation-aware test pattern optimization," 16th IEEE European Test Symposium (ETS), 214–214, (2011).

[8] Dutta, A., Kundu, S., Chattopadhyay, S., "Thermal aware don't care filling to reduce peak temperature and thermal variance during testing", 22nd Asian Test Symposium, 25–30, (2013).

[9] Chandra, A., Chakrabarty, K., "Test data compression and test resource partitioning for system-on-a-chip using frequency-directed runlength (FDR) codes", IEEE Transactions on Computers, 52(8): 1076-1088, (2003).

[10] Yuan, H., Guo, K., Sun, X., Ju, Z., "A power efficient test data compression method for soc using alternating statistical run-length coding", Journal of Electronic Testing, 32(1): 59–68, (2016).

[11] Sankaralingam, R., Oruganti, R.R., Touba, N.A., "Static compaction techniques to control scan vector power dissipation" Proceedings of IEEE VLSI Test Symposium, 35–40, (2000).

[12] Hamzaoglu, I., Patel, J.H., "Test set compaction algorithms for combinational circuits", Proceedings of ACM international conference on Computer-aided design. ACM, 283–289, (1998).

[13] Stan, M.R., Skadron, K., Barcella, M., Huang, W., Sankaranarayanan, K., Velusamy, S., "Hotspot: A dynamic compact thermal model at the processor-architecture level", Microelectronics Journal, 34(12): 1153–1165, (2003).

[14] Brglez, F., Bryan, D., Kozminski, K., "Combinational profiles of sequential benchmark circuits", IEEE International Symposium on Circuits and Systems, 1929–1934, (1989).

[15] Pathak, S., Grover, A., Pohit, M., Bansal, N., "Locco-based scan chain stitching for low-power dft," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, 25(11): 3227–3236, (2017).

[16] Thilagavathi, K., Sivanantham, S., "Two-stage low power test data compression for digital VLSI circuits", Computers and Electrical Engineering, 71: 309-320, (2018).

[17] Synopsys Inc., Design Compiler User Guide, Version B-2008.09 ,(2008).

[18] Synopsys Inc., Power Compiler User Guide, Version D-2010.03-SP2 ,(2010).

[19] Sivanantham, S., Mallick, P.S., Raja Paul Perinbam, J., "Low-power selective pattern compression for scan-based test applications", Computers and Electrical Engineering, 40(4): 1053-1063, (2014).