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A Modified Nearest Level Modulation Scheme for a Symmetric Cascaded H-Bridge Inverter

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Abstract

An efficient pulse width modulation scheme for Cascaded H-Bridge inverter (CHBI) is proposed in this paper. The proposed modulation scheme is a low switching frequency modulation scheme termed as modified Nearest Level Modulation (mNLM) scheme. Compared to the conventional nearest level modulation (NLM) scheme, the proposed modulation scheme reduces the total harmonic distortion (THD) at the ac output of the inverter. The mNLM follows an algorithm presented in the paper in order to arrive at a set of switching angles for MLI which offers reduced THD. Simulation is carried out using MATLAB/Simulink 2015b software and hardware is presented which validates the simulation results. Results show that there is a notable reduction in the THD content with the use of proposed modulation scheme. Because of the improved THD content, improvement in the other inverter parameters such as rms voltage, rms current and increased output power is also observed.

NOMENCLATURE:

V_{dc} - dc voltage value

N_{level} - No. of levels

S_x - Switch no. (x)

α_i - Firing angle

V_{rms} - rms voltage

ABBREVATIONS:

CHBI - Cascaded H-bridge inverter

MLI - Multilevel inverter

NLM - Nearest level modulation

mNLM - modified nearest level modulation

THD - Total harmonics distortion

SHE - Selective harmonics elimination

SPWM - Sine pulse width modulation

SVM - Space vector modulation

IGBT - Insulated-gate bipolar transistor

DC-MLI - Diode Clamped MLI

FC-MLI - Flying Capacitor MLI

1. INTRODUCTION

Multilevel inverter (MLI) is a power electronics device which can generate a high power stepped ac waveform. The stepped ac waveform is achieved by the proper combination of several dc sources at the input of MLI. With the use of medium-power semiconductor devices, the MLI is able to deliver a quality ac output with lesser harmonic distortion and a higher number of levels [1]. The MLIs are able to draw input current with low distortion [2]. In recent years, the applications of MLIs are widespread. They have found applications with renewable energy, grid-connected systems, stand-alone systems and use in power system applications [3-5].

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The MLIs emerged in the year 1981 in the form of a neutral-point-clamped inverter (DC-MLI) by Nabae et al [6, 7]. This was followed by development of a new MLI topology named as Flying Capacitor MLI (FC-MLI) by Meynard and Fosch in 1992 [8]. In the year 1995, cascaded H-bridge MLI topology came into existence [9]. This topology is considered as a revolutionary topology because of its ability to operate without the use of diodes and capacitor as was the case with the previous two topologies. The CHBI topology also led to the invention of many newer MLI topologies. The MLI topologies can be classified into symmetrical and asymmetrical types on the basis of the magnitude of dc voltage sources. In a symmetrical MLI topology, the dc voltage source at the input carry equal voltage magnitude. On the other hand, an asymmetrical MLI carries input dc voltage sources of unequal magnitude [10-14]. The striking feature of an asymmetrical MLI over symmetrical MLI is the ability to generate higher number of levels considering the same MLI topology. This results in a lesser THD, but it also comes at the cost of increased switching frequency.

The focus of this paper is on the cascaded H-bridge inverter (CHBI), which is a series combination of several full-bridge inverters with separate dc sources [15]. The series connection is useful for increasing the number of levels at the ac output. The CHBI has played a key role in facilitating medium-voltage and high-power applications. The modular structure of MLI offers greater reliability and easy maintenance when compared to the other two conventional topologies. The CHBI integrated with many new topologies helps improving the overall converter efficiency leading to hybrid MLI topologies. Apart from the field of power electronics, the CHBI has found applications in the field of power systems such as dynamic voltage restorer and for grid-connected applications.

An MLI can be operated very effectively based on the switching sequence of the semiconductor switches. To operate an MLI, there are many conventional modulation schemes. Some of them are selective harmonic elimination (SHE), sine pulse width modulation (SPWM), space vector modulation (SVM), nearest level modulation (NLM) etc., [16-20]. Modulation schemes can be classified into low switching frequency and high switching frequency. In low switching frequency modulation schemes, the switches operate under line frequency to a few kHz, while high-frequency modulation schemes operate the switches under several kHz [21].

By operating the MLI under low switching frequency, the device switching losses can be reduced to a great extent. The other benefits of operating the switches under low frequency are lesser cooling requirements and operating costs. SHE, NLM, SVM, predictive control are some of the examples of low switching frequency modulation schemes. The NLM works on the phenomenon of a sine wave. A reference signal is compared with the sine wave for generating switching pulses which drive the gate pulses of the switches. By a proper switching of the semiconductor switches, the MLI is able to generate a staircase output which reciprocates a sine wave. The switching frequency is usually lesser than 1 kHz and, as the number of levels increases, the output contains lesser harmonic content. This paper proposes a modified version of NLM where the harmonic content is significantly less than seen in the use of conventional one. As a result, the overall converter parameters have seen significant improvement.

2. CHB-MLI TOPOLOGY

Figure 1 is the circuit diagram of CHBI. The CHBI presented consists of twelve IGBTs and three dc sources. The twelve switches have been arranged in the form of three H-bridges cascaded with each other [22]. By turning on the switches S_1-S_2, S_5-S_6 or S_9-S_{10}, the corresponding voltage source is reflected as positive output at the load. Similarly, by turning on the switches S_3-S_4, S_7-S_8 or S_{11}-S_{12}, the corresponding voltage source is reflected as negative output at the load. The CHBI can generate ac voltage output of 7 level.

In a symmetric configuration, all the dc voltage sources have identical magnitude. When the three voltage sources are symmetric in the CHBI, it leads to a 7 level output. The three generated levels are V_{dc1}, $V_{dc1}+V_{dc2}$ and $V_{dc1}+V_{dc2}+V_{dc3}$. A higher number of levels can be generated by extending the number of voltage sources and switches.

In order to extend the symmetrical configuration for the generation of a larger number of levels, the equations (1) and (2) can be utilized. equation (1) represents the dc voltage values, while(2) represents the number of level (N_{level}) attained.

The value of each dc source is denote by,

$$V_{dc,j} = V_{dc}\, for\ j = 1,2,3,\ldots \tag{1}$$

where *j* is the number of dc voltage source.

$$N_{level} = 2x + 1\ for\ x = 1,2,3,\ldots \tag{2}$$

where *x* is the number of full bridge inverter.

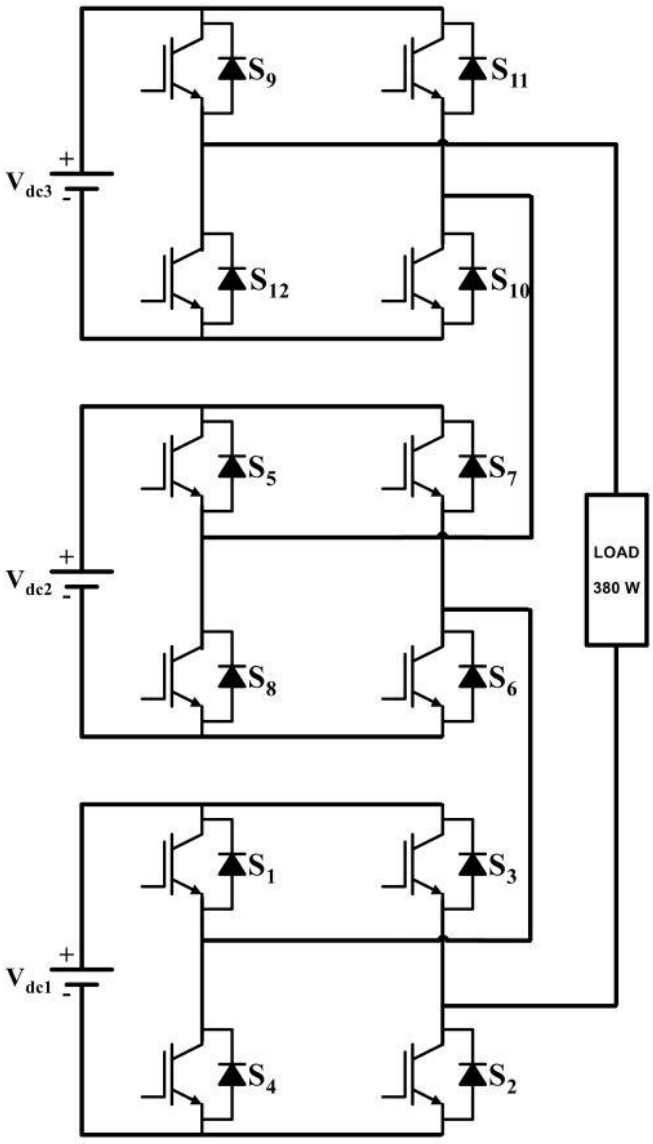

Figure 1. *CHBI Topology*

3. PROPOSED LOW SWITCHING FREQUENCY MODULATION SCHEME

The NLM utilizes a low switching frequency approach to drive the MLI. The phenomenon of a sine wave is the basis of operation of NLM. The NLM scheme helps in synchronizing the MLI output with that of a sine waveform. This is shown in Figure 2.

The firing angle calculation to each switch should be such that on overlapping a sine waveform and the multilevel output waveform of equal peak voltage, the sine waveform cuts through the rising edge of the multilevel output at exactly half of its magnitude. This is illustrated in Figure 2. The equation (3), the switching angle for a NLM scheme can be calculated [23],

$$\alpha_i = \sin^{-1}\left(\frac{i-0.5}{n}\right);\ \text{for } i = 0,1,2,3,...,n \tag{3}$$

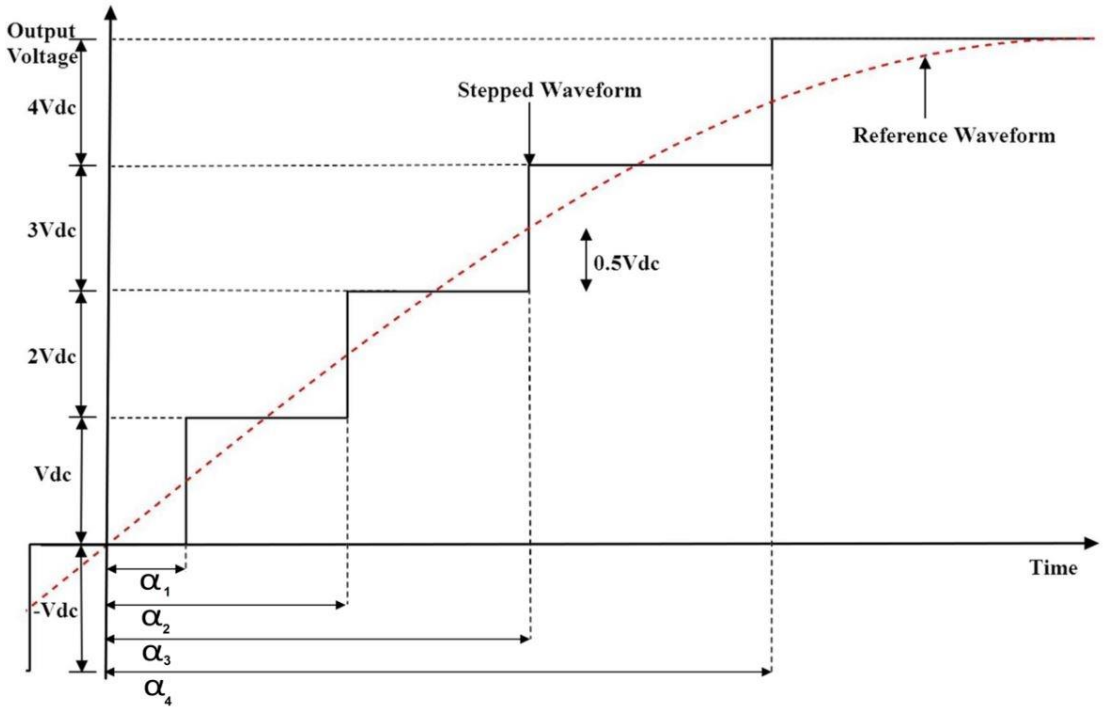

Figure 2. *Conventional Nearest Level Modulation Scheme*

The complete algorithm of mNLM scheme is shown in Figure 3. In the proposed modulation scheme, the number of levels (n) and the number of angles (i) of the MLI are defined. Using equation (3), the value of each angle is calculated depending on the number of angles. The value of the angles calculated is in degree units.

With the calculated values of the angles, the THD is determined using equation (4) [24],

$$THD = \frac{\sqrt{\frac{\pi^2 n^2}{8} - \frac{\pi}{4}\sum_{i=0}^{n-1}(2i+1)\alpha_{i+1} - \left(\sum_{i=1}^{n}\cos(\alpha_i)\right)^2}}{\sum_{i=1}^{n}\cos(\alpha_i)} \tag{4}$$

The next step of iterations begins when the THD is obtained. The iteration begins when the first switching angle is decreased by 1 degree. With this new set of switching angle, the new THD is calculated. The same switching angle is further reduced by 1 degree if the new THD is found to be less that the previous one. This will continue till there is no further reduction in THD. Now the next switching angle is taken, and it is reduced by 1 degree. If the new THD is found to be less than the previous one, then the process continues.

This process will go on till all the angles are completed in their respective turn. After the last switching angle is iterated, the process again starts from the first angle with the new switching angle values. This iteration process will go on till there is no further reduction of THD. The process so far explained will be repeated with a decrease in switching angle of 0.1 degree. Once the final values of switching angles arrive, when there is no further reduction in THD, then the process is terminated. The significant iteration results for a 7 level MLI output is shown in Table 1. It can be observed that to settle at a least THD value of 11.5344%, it took 28 iterations.

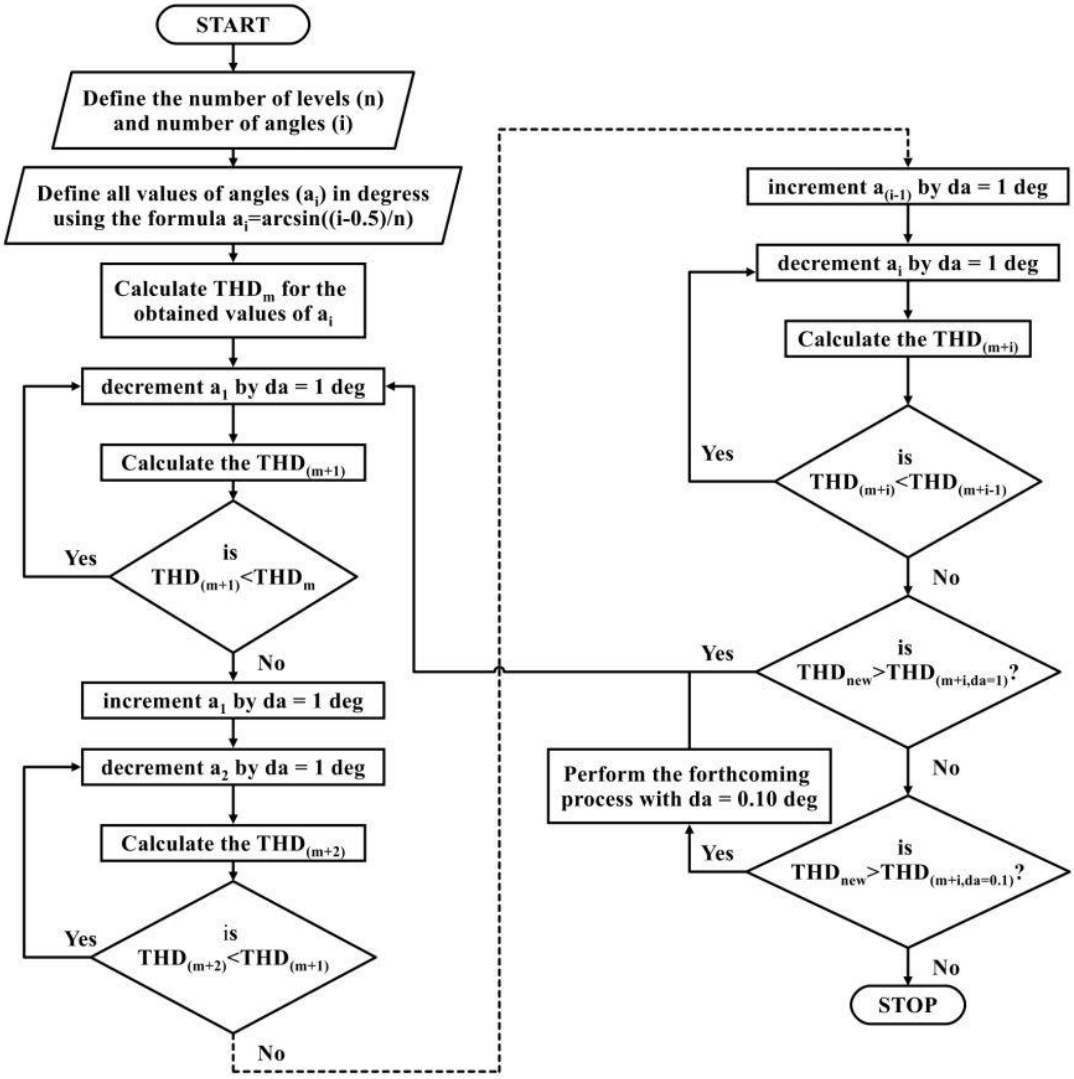

Figure 3. *Proposed Modulation Scheme*

Table 1. *Modified NLM (Results of significant iterations)*

Iteration	1	9	15	22	28
α_1 (deg)	9.60	9.60	8.60	8.60	8.60
α_2 (deg)	30.00	29.00	28.00	27.80	27.60
α_3 (deg)	56.44	51.44	50.44	50.44	50.44
THD	12.2270	11.6322	11.5422	11.5366	11.5344

4. RESULTS AND DISCUSSIONS

This section presents the simulation and hardware results of mNLM on CHBI. The circuit was simulated with MATLAB/Simulink 2015b package. The MLI was operated to generate a power of 380 watts. A 110 Vrms ac output was generated at 50 Hz frequency. The resistor load was rated at 36 ohms, whereas, the resistor-inductive load was rated at 35 ohms and 50 mH. Figures 4 and Figure 5 show the simulation results for a R load and RL load respectively. It was observed that the CHBI generated a seven level output. The fundamental voltage for R load was seen as 158.7 V and 165.8 V for NLM and mNLM respectively. On the other hand, the fundamental voltage for RL load was seen as 158.1 V and 167.3 V respectively.

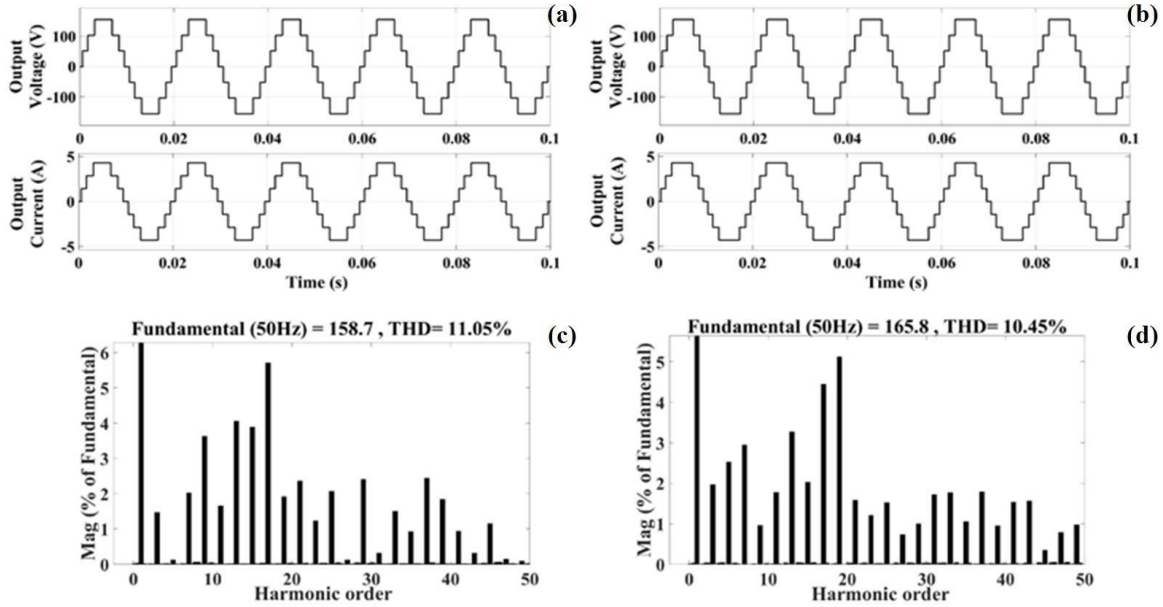

Figure 4. *Simulation results of CHBI with R Load (a) Output voltage and output current waveforms using NLM (b) Output voltage and output current waveforms using mNLM (c) Voltage THD using NLM (d) Voltage THD using mNLM*

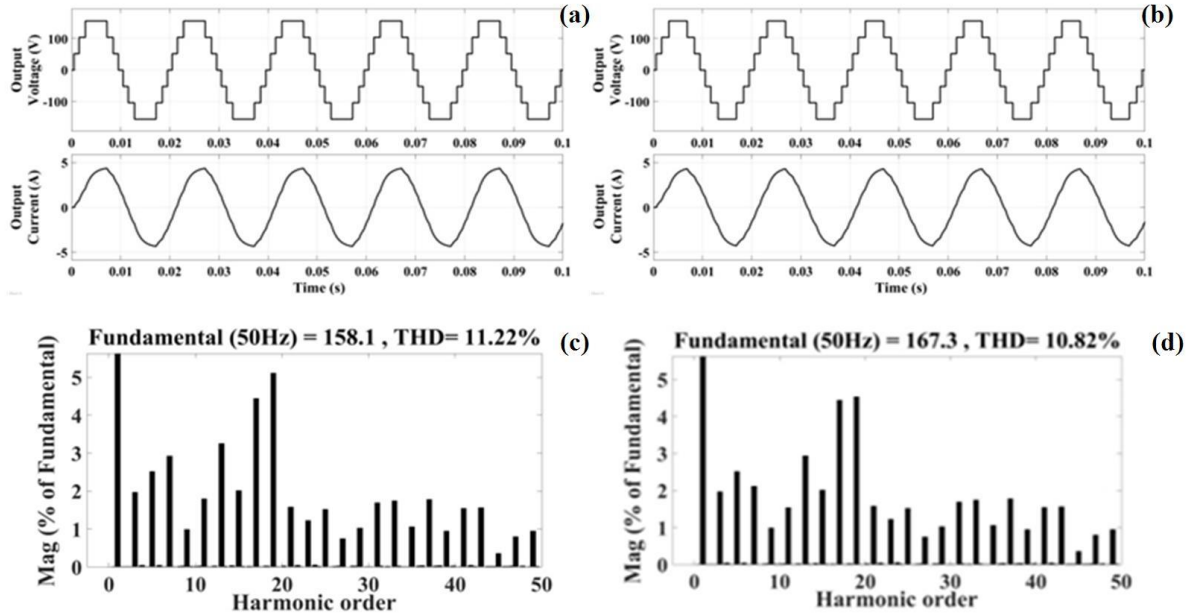

Figure 5. *Simulation results of CHBI with RL Load (a) Output voltage and output current waveforms using NLM (b) Output voltage and output current waveforms using mNLM (c) Voltage THD using NLM (d) Voltage THD using mNLM*

To carry out the hardware prototype, three Aplab/(0-64 V, 10A) dc sources were taken. Twelve IGBT switches (H15R1203) rated at 1200 V and 15 A were used with TLP250 optocoupler to drive gate terminal of each switch. The pulses were generated using Atmega32 micro controller. The power quality analyzer Fluke 435b was used to observe the ac output of the MLI. Figure 6(a) and Figure 6(b) presents the voltage and current waveforms for R load using NLM and mNLM scheme respectively. Figure 6(c) and Figure 6(d) shows the corresponding voltage THD using NLM and mNLM scheme respectively. Figure 7 presents a replica of Figure 6 output for RL load. The complete hardware setup is shown in figure 8.

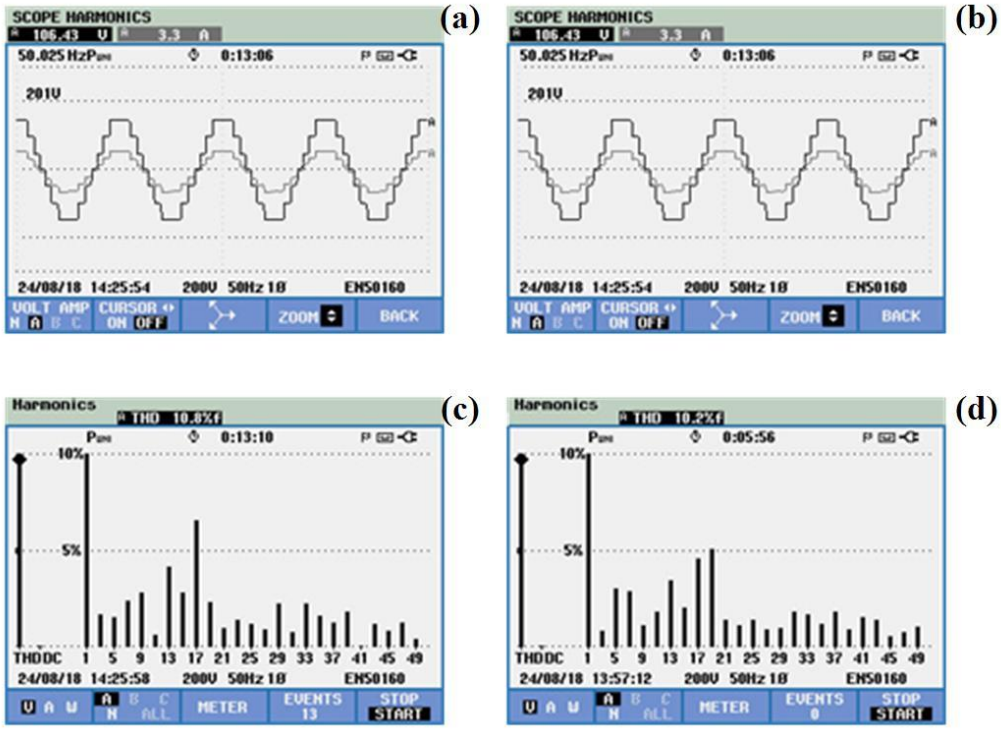

Figure 6. *Hardware results of CHBI with R Load (a) Output voltage and output current waveforms using NLM (b) Output voltage and output current waveforms using mNLM (c) Voltage THD using NLM (d) Voltage THD using mNLM*

Table 2 and Table 3 summarizes the simulation and hardware results comparison of various MLI parameters with the use of NLM and mNLM. It was observed that rms voltage and rms current improved significantly to yield higher power output. The Table 2 and Table 3 conclude that the implementation of the proposed modulation scheme had significantly improved the overall power quality of the ac output. For a R load, it was observed that by implementing the proposed modulation scheme, the voltage THD had reduced from 11.05% to 10.45%. Similarly, for a RL load it was observed that the THD reduced from 11.22% to 10.82%. It was seen that the rms voltage generated by using NLM and mNLM for a R load was 106.43 V and 110.28 V respectively. The rms current was seen to have improved from 3.3 A to 3.4 A with the use of mNLM. The voltage THD has seen a very good difference of 0.6% between NLM and mNLM. The generated power increased from 350 W to 379 W and 351 W to 375 W under simulation and hardware results respectively. Similarly for a RL load, the voltage THD reduced from 11.22 % to 10.82 % and 11.1 % to 10.6 % under simulation and hardware conditions respectively. The rms current has improved from 3.2 A to 3.4 A under both simulated and hardware results. Combined with the increased in the rms voltage, the generated power under RL load has increased from 336 V to 365 V and 332 V to 364 V for the simulated and hardware experiments respectively.

The IEEE standard 519-2014 suggests the THD to be within 8% for voltage of less than 1kV [25]. The current THD is found to be within the standards. For the voltage THD, the CHBI can be extended to 9 level and 11 level to bring the THD values within IEEE 519-104 standards. The mNLM scheme can be easily extended to higher levels.

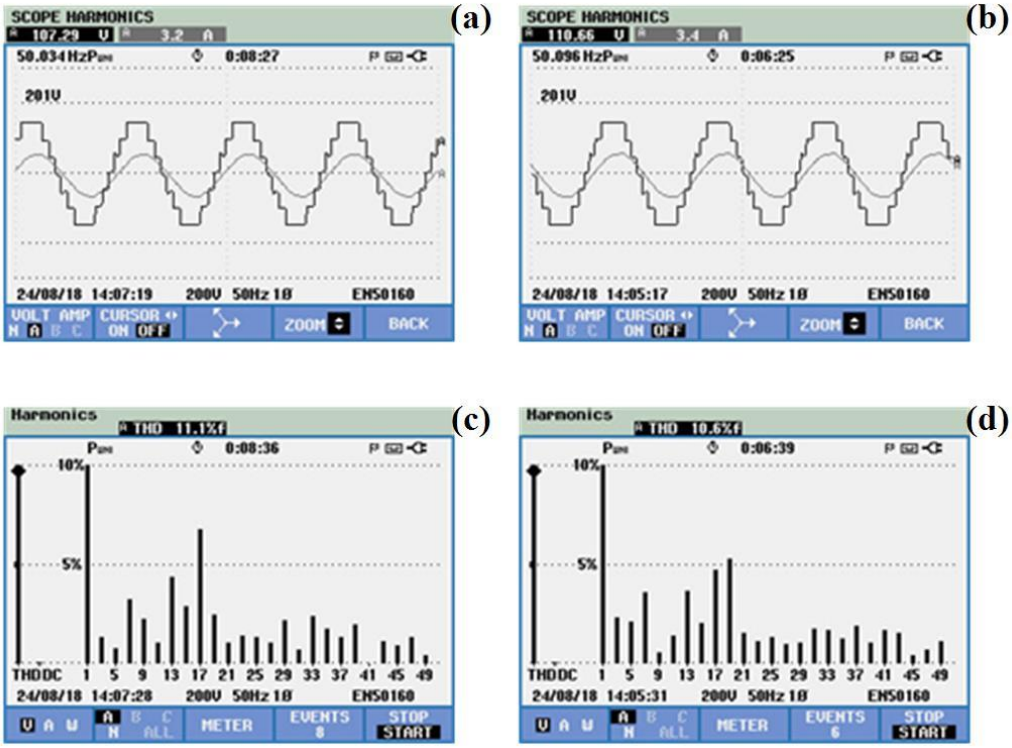

Figure 7. *Hardware results of CHBI with RL Load (a) Output voltage and output current waveforms using NLM (b) Output voltage and output current waveforms using mNLM (c) Voltage THD using NLM (d) Voltage THD using mNLM*

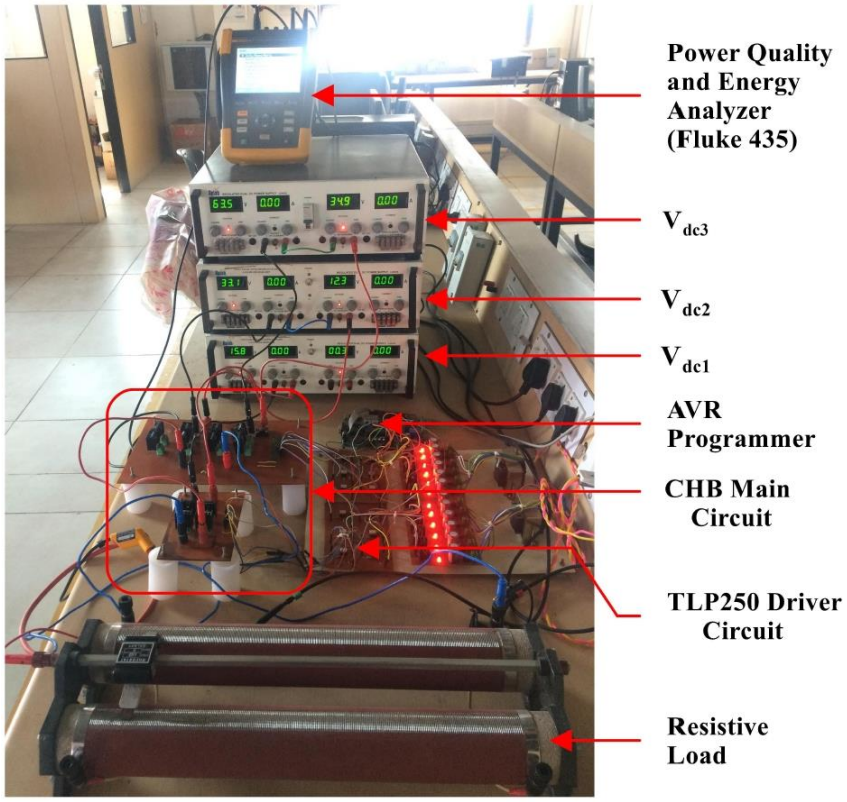

Figure 8. *Complete hardware setup for CHBI*

Table 2. *Performance parameters comparison of the inverter using NLM & mNLM scheme using R load*

MLI Parameters	Simulation Results		Hardware Results	
	NLM	mNLM	NLM	mNLM
Voltage THD (%)	11.05	10.45	10.80	10.20
Current THD (%)	11.05	10.45	10.59	10.06
RMS voltage (V)	107.23	110.52	106.43	110.28
RMS current (A)	3.26	3.43	3.3	3.4
Generated Power (W)	350	379	351	375

Table 3*. Performance parameters comparison of the inverter using NLM & mNLM scheme using RL load*

MLI Parameters	Simulation Results		Hardware Results	
	NLM	mNLM	NLM	mNLM
Voltage THD (%)	11.22	10.82	11.1	10.6
Current THD (%)	2.4	2.2	2.7	2.5
RMS voltage (V)	108.16	110.93	107.29	110.66
RMS current (A)	3.2	3.4	3.2	3.4
Generated Power (W)	336	365	332	364

5. CONCLUSION

The ac output of a MLI can be improved to a great extent by reducing the THD content. This paper provides a modified version of a conventional modulation scheme to achieve it. Using MATLAB/Simulink software, the simulation was carried out for the symmetric configuration of CHBI. The simulation results for R load show that the voltage and current THD had decreased by 5% while rms voltage and rms current has increased by 3% and 5% respectively. The power has increased from 350 W to 379 W. For a RL load, the voltage THD has decreased by 3.6%. The rms voltage, rms current and power has increased by 2.6%, 6% and 8.6% respectively. A hardware prototype is also presented in order to practically demonstrate the effectiveness of the proposed modulation scheme. For a R load, the MLI parameters have improved as per simulation results and generated power has increased by 6.8%. For the RL load, the increase in generated power is high as 9.6% while voltage THD has decreased by 4.5%. The proposed scheme can be extended to various asymmetrical configurations of CHBI.

CONFLICTS OF INTEREST

No conflict of interest was declared by the authors.

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