Cryogenic DC Characteristics of Low Threshold Voltage (V_{TH}) n-channel MOSFETs

M. B. YELTEN

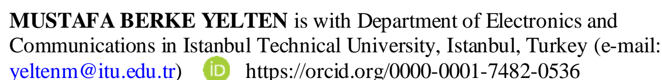
Abstract— **Cryogenic electronics has grown in its widespread use for various technological applications. Particularly, CMOS devices and circuits are more frequently used in such systems due to their dominance in the electronics industry. At cryogenic temperatures, characteristics of CMOS devices vary, which should be characterized with measurements. In this paper, the changes in the electronic behavior of a low threshold voltage (V_{TH}) n-channel MOSFET (nMOSFET) are captured experimentally. The results are then compared with the measurements of a regular nMOSFET having the same channel width and length. It is shown that although the V_{TH} increase of both transistors is at the same amount, this value corresponds to a more significant percentage of the nominal threshold voltage for the low V_{TH} nMOSFET.**

Index Terms— **Cryogenic electronics, threshold voltage, low threshold voltage transistors, cryogenic measurements.**

I. INTRODUCTION

CRYOGENIC systems, which can be defined as systems operating in the temperature regime below 100 K, have recently become prominent and widespread with increasingly more applications in the defense industry, space communications and research, novel computation architectures, and information storage systems. In the military, infrared cameras should have high precision detectors, for which the readout integrated circuits must have a very low noise figure. Such a performance is only possible when the operating temperatures are reduced down to the cryogenic range [1, 2].

Moreover, electronic equipment designed for space communications and research should accommodate the harsh conditions prevailing in space, where the ambient temperature can drop to −200 °C (80 K) [3-5]. As far as the novel computation architectures are concerned, quantum computing emerged as one of the most promising approaches, in which the probabilistic wave function of an electron defines the quantum state called qubit that replaces the bits in the traditional Boolean algebra. Qubits enable completely different algorithms with much higher computational efficiency to be. Nevertheless, qubits reach their operational state only when the temperature is cooled down to 15 – 20 mK [6]. Hence, peripheral electronic circuits that communicate with the qubits should be capable of operating at temperatures below 20K [7].



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Finally, the cryogenic regime has been shown to enhance the performance of memory systems where high-speed DRAM structures can be produced with better power efficiency [8, 9].

To design electronic circuits that will operate with high performance in cryogenic temperature range, devices, and components building such systems should be experimentally characterized. In this work, cryogenic characterization of low V_{TH} nMOSFETs, which are frequently used in low power circuit design, has been performed. The organization of the paper is arranged as follows. In Section II, the physical changes in the characteristics of a MOSFET at cryogenic temperatures are discussed. Subsequently, the test chip designed for the experimental analysis of the low V_{TH} MOSFETs will be described in Section III. In Section IV, measurement results encompassing I_D - V_{DS} and I_D - V_{GS} curves of both low and regular V_{TH} transistors are presented and discussed. Finally, conclusions will be drawn in Section V.

II. CHANGES IN MOSFET CHARACTERISTICS AT CRYOGENIC TEMPERATURES

As the temperature of a MOSFET is reduced, several of its physical properties are changed. The first of them is the charge carrier mobility. Scattering mechanisms determine how much the mobility is impaired at any temperature. Generally, at very low temperatures, the charge carriers have less kinetic energy; therefore, they stumble on the ionized impurities. Conversely, at high temperatures, due to increased energy of charge carriers and massive lattice vibration, more collisions occur, hence the mobility of the charge carriers comes down. The optimum temperature, at which the mobility is maximized, happens to be at much lower temperatures than the room temperature (300 K). Thus, the mobility of charge carriers increases significantly as the ambient temperature drops down to the cryogenic regime.

Another physical property that is being altered at cryogenic temperatures is the threshold voltage (V_{TH}). The typical equation for the MOSFET threshold voltage can be provided as follows [10]:

$$V_{TH} = V_{FB} - \frac{Q_I}{C_{ox}} - \frac{Q_D}{C_{ox}} + 2\phi_F, \quad (1)$$

In (1), the dominating term is the last one of the right side, which represents the Fermi potential of the substrate:

$$\phi_F = \frac{k_B T}{q_e} \ln \frac{N_A}{n_i} \quad (2)$$

Here, k_B is the Boltzmann constant, T is the temperature, q_e is the electronic charge, N_A is the substrate doping

concentration, and n_i is the intrinsic charge carrier concentration for the bulk material. n_i depends heavily on the temperature, and it severely drops at cryogenic temperatures. Therefore, the Fermi potential is increased significantly, and this leads to a rise in the nMOSFET V_{TH}.

The saturation velocity of charge carriers rises at cryogenic temperatures due to increasing mobility values. Furthermore, the drain-source resistance drops, since the conductivity of charge carriers grows, as long as complete ionization of dopant atoms can still be realized at that cryogenic temperature. However, impacts of these are minor in comparison to those of the changes in the charge carrier mobility and the device V_{TH}.

III. TEST CHIP FOR EXPERIMENTAL CHARACTERIZATION AND MEASUREMENT SETUP

In order to experimentally characterize the cryogenic properties of low V_{TH} nMOSFETs, a test chip has been fabricated that contains several types of transistors, including low V_{TH} nMOSFETs (Fig. 1) [11]. Here, four pads are assigned to every transistor corresponding each to one terminal of the transistor. In Fig. 2, the organization of the pads around the low V_{TH} MOSFET layout can be seen, which belongs to a commercial 180 nm device technology. The pads in Fig. 2 are used to apply DC voltages to the gate, source, bulk, and the drain, at which the drain current will be monitored.

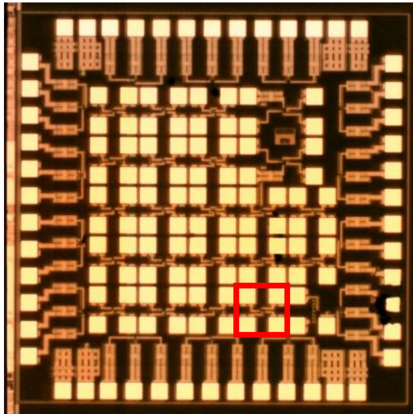


Fig.1. Chip micrograph of the fabricated test chip. The red rectangle shows the location of the low V_{TH} nMOSFET and the surrounding pads.

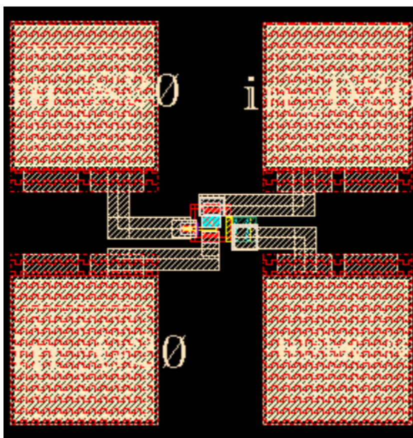
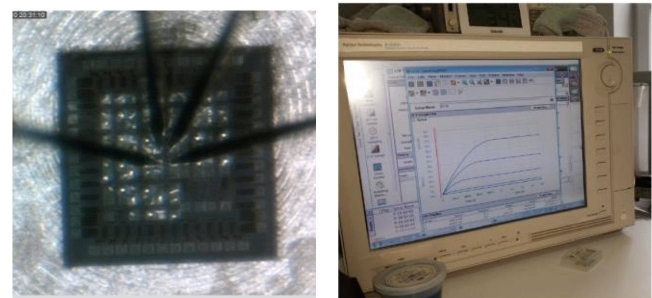


Fig.2. The layout of the low V_{TH} nMOSFET.

A low-cost cryogenic measurement setup has been developed to experimentally characterize the fabricated test chip (Fig. 3). For this purpose, an MDC 441 Cryogenic Probing System has been employed, where a dewar containing liquid nitrogen (LN2) is connected through flexible metal pipes to the actual probe station. LN2 is directly passed underneath of the chuck, on which the bare die lies in intimate contact. In that regard, the die comes easily in thermal equilibrium with the boiling LN2 at −196 °C (77 K). The vaporized nitrogen is then dumped to outside in gas form. A stereo microscope with a long working distance is used to view and touch the pads of the transistors (Fig. 4a). Along with the probing station, the Agilent B1500A Semiconductor Parametric Analyzer is utilized to capture the $I-V$ characteristics of the transistors under test (Fig. 4b).

Overall, the test set-up that has been established in this work is cheaper since it only cools down the chuck rather than the entire volume around the chip. Nevertheless, the intimate contact is sufficient to ensure the right measurement temperature for the device under test, thereby rendering the set-up a practical alternative in comparison to more expensive cryostats and cryogenic probe stations.

Fig.3. Cryogenic probe station and the measurement test setup.



(a) (b)

Fig.4. (Left) The test chip under stereo microscope, (right) Agilent B1500A used in the characterization of transistors under test.

IV. MEASUREMENT RESULTS AND DISCUSSION

The low V_{TH} nMOSFET characterized in this work has a channel length of 0.5 µm and a channel width of 35 µm with seven fingers. To better understand the $I - V$ characteristics of this device, a same-size regular nMOSFET is also experimentally analyzed, and the results acquired from both transistors are then compared.

First, the room temperature and cryogenic temperature characteristics of the low V_{TH} nMOSFET should be extracted. For this purpose, I_D - V_{DS} and I_D - V_{GS} curves have been captured at both 77 K and 300 K and depicted in Fig. 7 and Fig. 8, respectively. The changes in the I_D and V_{TH} of a regular and low V_{TH} NMOSFET have been analyzed numerically in Table I and Table II, respectively.

Fig. 7 clearly shows that at cryogenic temperatures, the I_D of low V_{TH} nMOSFETs sharply increases due to the rise in the mobility. In Table I, this change is noted to be by 50%. Through performing similar measurements on a regular nMOSFET, it is demonstrated that the rate of current increase is also around 50%. Thus, low V_{TH} nMOSFETs behave similarly to regular nMOSFETs as far as the drain current at cryogenic temperatures is concerned. Nevertheless, for the same gate and drain voltages applied, the drain current of low V_{TH} nMOSFETs is almost 50% higher due to the smaller device V_{TH}.

Fig. 8 shows that the threshold voltage is increased for a low V_{TH} nMOSFET at cryogenic temperatures in accordance with the theoretical expectations. V_{TH} is a key parameter and should remain low in order the circuit applications based on low V_{TH} characteristics of transistors can still be functional at cryogenic temperatures. Nevertheless, Table II indicates that the V_{TH} increase amounts are the same for both low V_{TH} and regular nMOSFETs, where the percentage change in the threshold voltage of low V_{TH} nMOSFETs reaches 75%. Therefore, circuit designers should be aware that the performance of designs based on low V_{TH} nMOSFETs would be significantly degraded at cryogenic temperatures due to this serious hike in the device V_{TH}. Even so, the threshold voltage of low V_{TH} nMOSFET is still around half of the regular transistors' V_{TH}.

Fig. 9 show the ensemble I_D - V_{DS} characteristics of low V_{TH} nMOSFETs extracted experimentally from 11 different devices at both room and cryogenic temperatures. Results demonstrate that in the cryogenic regime, the variability of the I_D - V_{DS} characteristics also goes up. Therefore, circuit designers should know that in addition to the changes in transistor parameters, the impact of variations would be more pronounced, as well. As a remedy, the designs should contain more room for random variations in the expense of performance cuts.

V. CONCLUSIONS

This paper describes the changes observed in the I_D - V_{DS} and I_D - V_{GS} characteristics of low V_{TH} nMOSFETs. In addition, the extracted characteristics have been interpreted with respect to the results acquired from the same-size regular nMOSFETs. Overall, it has been demonstrated that similar outcomes can be observed for both types of transistors, albeit low V_{TH} nMOSFETs have a more dramatic increase in their V_{TH} values. This is a potentially significant issue as the performance of relevant circuits can be substantially degraded at cryogenic temperatures based on this change. Furthermore, the variability of I_D - V_{DS} characteristics also increases in the cryogenic regime, which contributes to the burden of the previous problem. Hence, the designs should be generated such that the potential impact of such difficulties is properly accounted during circuit design (e.g., transistor sizing).

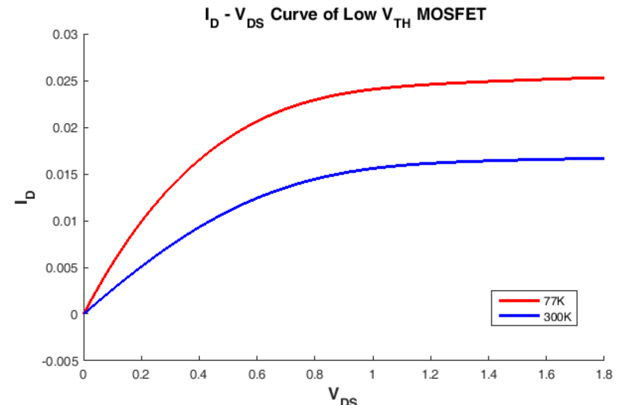


Fig.7. I_D - V_{DS} characteristics of the low V_{TH} nMOSFET at 77 K and 300 K (V_{GS} = 1.8 V).

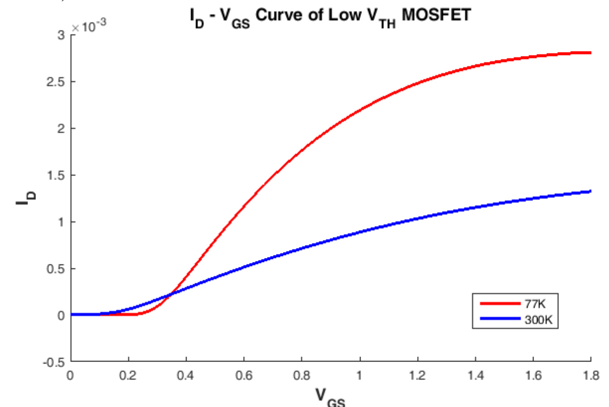


Fig.8. I_D - V_{GS} characteristics of the low V_{TH} nMOSFET at 77 K and 300 K (V_{DS} = 50 mV).

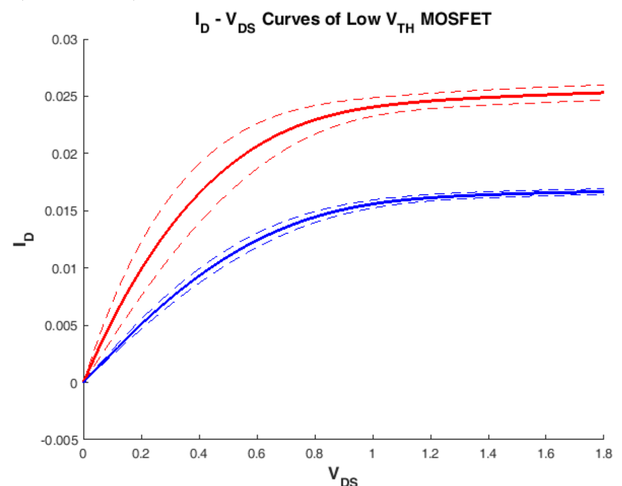


Fig.9. I_D – V_{DS} characteristics of an ensemble of low V_{TH} nMOSFETs at 77 K and 300 K (V_{GS} = 1.8 V).

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TABLE I.
Comparison of I_D values for regular and low V_{TH} nMOSFETs at room and cryogenic temperatures.

Transistor Type	Sizes (*W* x *L*)	I_D at room temperature	I_D at cryogenic temperature (LN2)	Difference	Increase
Low V_{TH} NMOS Transistor	35 µm x 0.5 µm	16.92 mA	25.31 mA	8.39 mA	%50
Regular V_{TH} NMOS Transistor	35 µm x 0.5 µm	11.2 mA	16.92 mA	5.72 mA	%51

TABLE II.
Comparison of V_{TH} values for regular and low V_{TH} nMOSFETs at room and cryogenic temperatures.

Transistor Type	Sizes (*W* x *L*)	V_{TH} at room temperature	V_{TH} at cryogenic temperature (LN2)	Difference	Increase
Low V_{TH} NMOS Transistor	35 µm x 0.5 µm	0.16 V	0.28 V	0.12 V	%75
Regular V_{TH} NMOS Transistor	35 µm x 0.5 µm	0.44 V	0.56 V	0.12 V	%27

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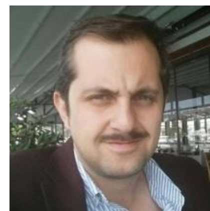
BIOGRAPHY



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