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Al/CdZnO/p-Si (MIS) Yapısının Voltaja Bağlı Arayüzey Durumlarının ve Bu Durumların Gevşeme Sürelerinin Admitans Metodu İle İncelenmesi

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ÖZET: Al/CdZnO/p-Si (MIS) yapısının voltaja bağlı arayüzey durumları / tuzakları (N_{ss}) ve bu durumların gevşeme süreleri (τ) 5 kHz-1 MHz frekans aralığındaki C-V-f ve G/ω-V-f ölçümleri kullanılarak admitans yöntemi ile incelenmiştir. Hem C hem de G/ω değerleri voltaj ve frekansın güçlü bir fonksiyonu olarak bulundu ve bu değerler hemen hemen her voltaj için azalan frekansla artar. Düşük frekanslarda elde edilen daha yüksek C ve G değerleri, CdZnO/p-Si arayüzeyi arasında yer alan N_{ss} varlığından kaynaklanmaktadır. Düşük frekanslarda, tuzaklardaki yüklerin gevşeme süresi uygulanan ac sinyalin periyodundan ($\tau \geq T$) daha büyüktür, bu nedenle ölçülen C ve G/ω değerlerine katkıda bulunabilirler. Ayrıca, N_{ss} varlığı yapının hesaplanan paralel iletkenlik (G_p/ω)-Lnf eğrilerinde bir pike neden olur. Böylece, hem N_{ss} hem de τ değerleri, sırasıyla pik değerinden ve pikin konumundan hesaplandı. N_{ss} ve τ değerleri, sırasıyla 1.7 V'da 1.65×10^{13} eV^{-1} cm^{-2}, 31.4μs ve 3 V'da 1.39×10^{13} eV^{-1} cm^{-2}, 9.18 μs arasında değişmiştir. Bu değerler oda sıcaklığında bu yapılar için çok uygundur.

Anahtar Kelimeler: Admitans metodu, Arayüzey durumları, Gevşeme süresi, Al/CdZnO/p-Si (MIS) tip yapılar

Investigation of the Voltage Dependent Surface States and Their Relaxation Time of the Al/CdZnO/p-Si (MIS) Structure Via Admittance Method

ABSTRACT: The voltage dependent surface states/traps (N_{ss}) and their relaxation time (τ) of the Al/CdZnO/p-Si (MIS) structure were investigated with admittance method using C-V-f and G/ω-V-f measurements in the frequency range of 5 kHz-1 MHz. Both the values of C and G/ω were found as strong function of voltage and frequency and they increase with decreasing frequency almost for each voltage. The obtained higher values of C and G at the low frequencies are due to the presence of N_{ss} located between CdZnO/p-Si interfaces. At low frequencies, the relaxation time of the charges at the traps is larger than the period ($\tau \geq T$) of the applied ac signal, so they can contribute to the measured C and G/ω values. In addition, the presence of N_{ss} causes a peak at the extracted parallel conductance (G_p/ω) versus Lnf curves of the structure. Thus, both the values of N_{ss} and τ were calculated from the peak value and its position, respectively. The values of N_{ss} and τ ranged from 1.65×10^{13} eV^{-1} cm^{-2}, 31.4 μs at 1.7 V and 1.39×10^{13} eV^{-1} cm^{-2}, 9.18 μs at 3 V, respectively. These values are very suitable for these structures at room temperature.

Keywords: Admittance method, Surface states, Relaxation time, Al/CdZnO/p-Si (MIS) type structures,

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INTRODUCTION

In order to separate the metal from the semiconductor, thereby preventing the interface diffusion and the chemical reaction between the metal and the semiconductor, a variety of insulator/oxide/organic interface layers are inserted at M/S interface. The existence of this interfacial layer quite changes and improves the properties of the metal-semiconductor (MS) type diodes (Nicollian and Brews, 1982; Demirezen et al., 2017; Durmuş and Altındal, 2017; Nikravan et al., 2017; Taşçıoğlu et al, 2018; Tanrıkulu et al., 2018; Güçlü et al, 2019). Usually the C-V characteristics of MIS or MOS structures are expected to be independent of frequency, but in reality situation is quite different; it becomes dependent of frequency and voltage due to the effects of N_{ss}, R_s, thickness and homogeneity of interlayer and barrier height at M/S interface, surface and fabrication processes. For example, the presence of N_{ss} and R_s causes a peak behavior in the C-V plots in depletion/inversion and accumulation region, respectively. While N_{ss} are more effective both in inversion and depletion regions at low frequencies, R_s is dominate at high frequency only at accumulation region.

The existence of N_{ss} and restructure and reordering of them under bias voltage give shifts the peak position, but R_s and interfacial layer lead to bending or concave curvature of the C-V at accumulation region. (Nicollian and Goetzberger, 1965; Card and Rhoderick, 1971; Kar and Dahlke, 1972; Chattopadhyay and Raychaundhuri, 1993; Reddy et al., 2013). In this case, the applied voltage will be shared between interfacial layer, R_s. and depletion layer. Therefore, it can be concluded that it is crucial to evaluate and extract the N_{ss} as a function of applied voltage and frequency. The sources of these N_{ss} are usually crystal defects such as dangling bonds, dislocations, and some organic impurities in the laboratory environment. They also depend on the chemical composition of the interfacial layer and they can trade charges with the semiconductor. At the low frequencies, the lifetime of the charges at the traps is smaller than the period of the alternating signal, so that these charges can yield an extra C and G to the measured values, but at high frequencies, this contribution is low so it can be ignored. There are several suggested methods in the literature to extract the N_{ss} values such as forward bias current-voltage (Card and Rhoderick, 1971; Akhlaghi et al., 2018; Büyükbaş Uluşan et al., 2018; Tanrıkulu, 2018), the high-low frequency capacitance (C_{HF}-C_{LF}) (Castagne and Vapaille, 1971; Nicollian and Brews, 1982; Nikravan et al., 2017), quasi-static capacitance (Kuhn, 1970), surface admittance (Karma and Varma, 1985), Hill-Coleman (Hill and Coleman, 1980) and admittance techniques (Nicollian and Goetzberger, 1967; Nicollian and Brews, 1982; Yakuphanoğlu, 2008; Yücedağ, 2009; Engel-Herbert et al., 2010;Altındal et al., 2012; Kaya et al., 2014; Padma et al., 2017; Demirezen et al., 2017; Tecimer et al., 2018). Among them, admittance method which is suggested by Nicollian and Goetzberger gives the most accurate and sensitive results rather than other and this method is based on the conductance loss resulting from the trade of charges between N_{ss} and semiconductors when an ac signal applied. This method also provides the determination of lifetime of the charges at the traps referred τ.

The intention of this study is to calculate the voltage dependent profile of N_{ss} and their τ of the prepared Al/CdZnO/p-Si (MIS) structure by evaluating the admittance measurements. For this purpose, the C-V and G/ω-V measurements were carried out between 5 kHz and1 MHz at room temperature and then G_p/ω vs Ln(f) plots were drawn for various bias voltage to calculate the values of N_{ss} and τ from the peak values of them for each bias voltage.

MATERIAL AND METHOD

Al/CdZnO/p-Si (MIS) structures were produced on p-type (B-doped) Si wafer with (100) surface orientation, 350 mm thickness and $1.36x10^{16}$ cm^{-3} doping acceptor atoms. The detailed preparation process of the Al/CdZnO/p-Si (MIS) structures can be found in our previous study (Taşçıoğlu et al., 2018). Admittance measurements included the C-V and G/ω-V measurements were performed between 5kHz-1MHz at room temperature by the HP 4192 A LF impedancemeter with 40 mV_{rms} test signal.

RESULTS AND DISCUSSION

The Fig. 1 reveals the observed C-Ln(f) characteristics of Al/CdZnO/p-Si (MIS) structure between 5 kHz and 1 MHz frequencies, 0.2 V and 1.7 V voltages by 100 mV steps. As shown in this figure that at low frequencies C values increase with increasing voltage while at high frequencies they become almost independent of voltage. In addition, for each voltage value, C values decrease with increasing frequency due to the presence of N_{ss} which are more effective at low frequencies, because the τ of the charges at the N_{ss} is smaller than the T so that these charges can contribute to the measured C and G/ω values. Contrarily, at high frequencies, the lifetime of the charges at the N_{ss} is greater than the period of the applied ac signal. In other words, these charges cannot follow the ac signal easily, so that it cannot contribute the measured values or this contribution is small to negligible.

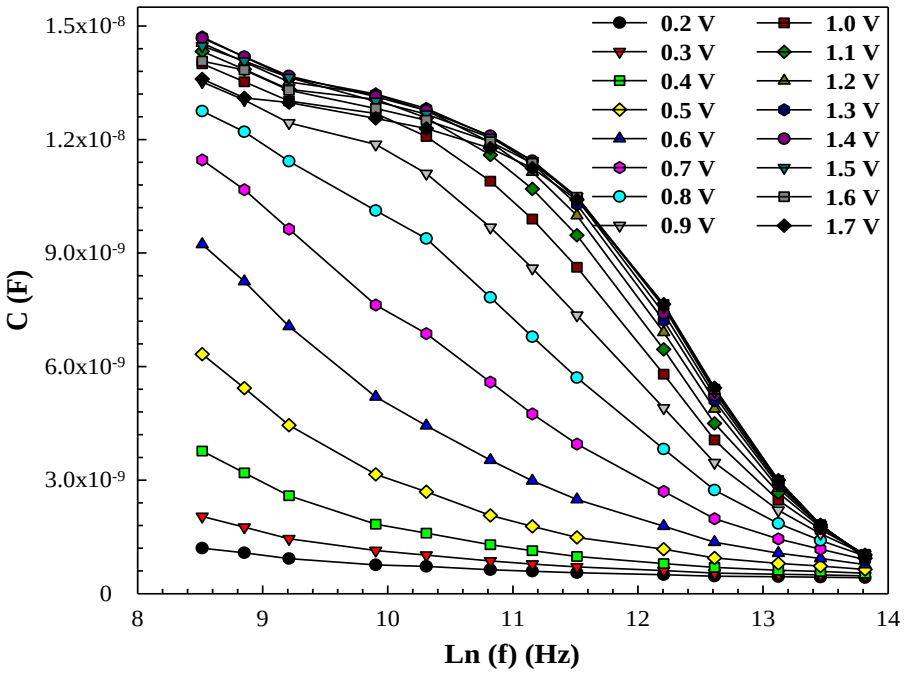

Figure 1: The C- Ln (f) curves of the Al/CdZnO/p-Si (MIS) structure for various applied bias voltages at room temperature.

Fig. 2 displays the G/ω- Ln (f) curves of Al/CdZnO/p-Si (MIS) structure in the voltage range of 0.2 to 1.7 V with 0.1 V steps. Similarly with C-Ln (f) curves, the G/ω values also decrease with increasing frequency almost exponentially due to the contribution of N_{ss} such as mentioned above. Also, it can be seen from the figure, while at low frequencies G/ω values have voltage dispersion, at high frequencies they are almost constant. The similar changes in C and G/ω values with frequency and applied bias voltage for different structures are reported in

the literature and usually were based upon the existence of N_{ss} and their a special distribution between interlayer and semiconductor in the forbidden bandgap of semiconductor at the junction (Tecimer et al., 2014; Kaya et al., 2014; Orak and Koçyiğit, 2016; Ejderha et al., 2018; Badali et al., 2018; Reddy et al., 2018; Karabulut, 2018; Tanrıkulu et al., 2018; Marıl et al., 2018;). It is explicit that the changes in the C and G become more pronounced at low frequency and higher forward bias voltages.

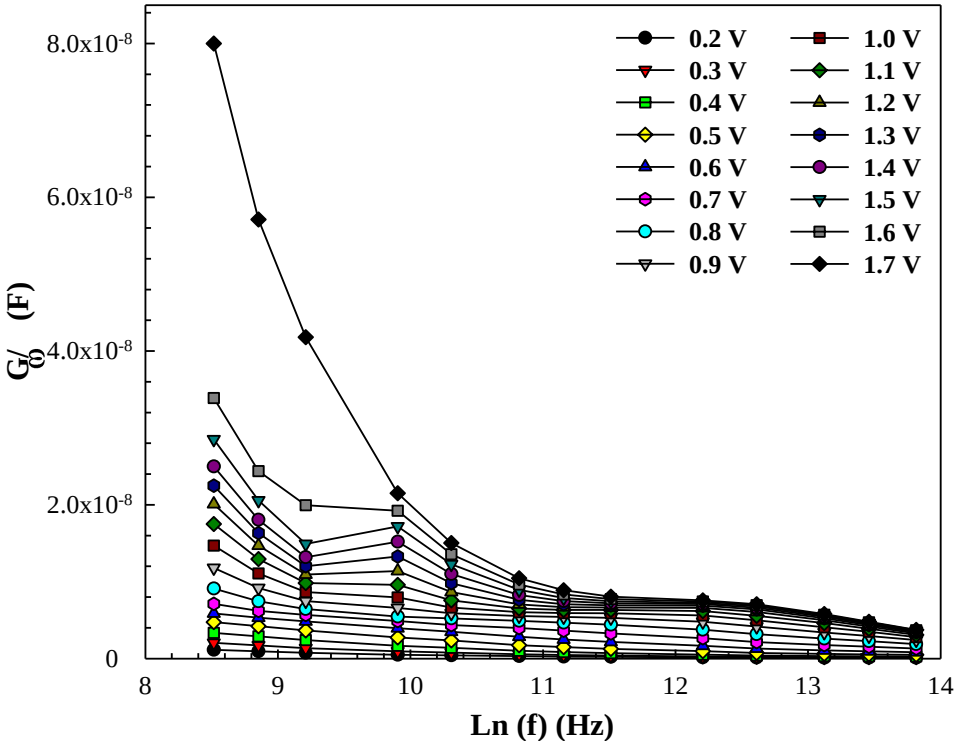

Figure 2: The G/ω- Ln (f) curves of the Al/CdZnO/p-Si (MIS) structure for various applied bias voltages at room temperature.

There are various suggested methods to determine the N_{ss} values at different voltage and frequency regions. In this study, the admittance method developed by Nicollian and Goetzberger is preferred due to its accuracy and sensitivity. Additionally, for MIS or MOS type structures, this method can also specify bulk and interface defects. When an ac signal is applied onto devices, Fermi energy oscillates about the medium positions governed by dc bias. According to this method, the voltage or energy density distribution of N_{ss} is identified by means of the loss resulting from alters in their occupancy caused by small variations of gate voltage. This energy loss is measured as an equivalent parallel conductivity given with the following equation;

$$\frac{G_p}{\omega} = \frac{\omega G_m C_i}{G_m^2 + \omega^2 (C_i - C_m)^2} = \frac{q N_{ss}}{2\omega\tau} \ln(1 + \omega^2 \tau^2) \quad (1)$$

In Eq.1, q is the electron charge, ω is the angular frequency (=2πf), τ is the relaxation time of the charges at the surface states, G_m and C_m are the measured conductance and capacitance at any given bias voltage, respectively. The parallel conductance values at various voltages were calculated using measurements results in Eq.1 and the G_p/ω –Ln (f) curves were drawn and given in Fig.3.

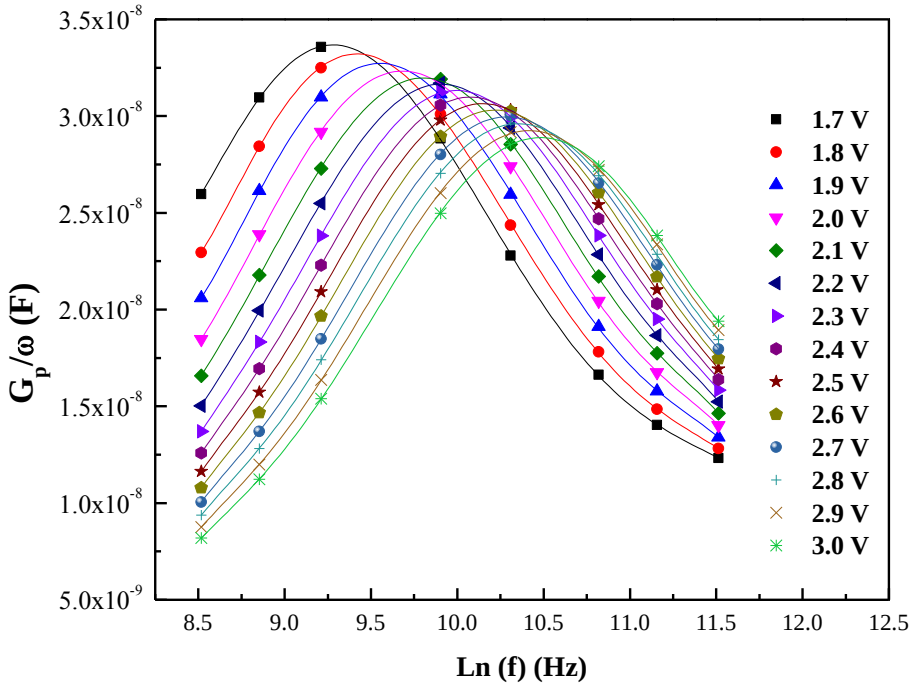

Figure 3: The G_p/ω- Ln (f) curves of the Al/CdZnO/p-Si (MIS) structure for various applied bias voltages at room temperature.

It is clear that the G_p/ω –Ln (f) curves have a peak only between 1.7 and 3.0 V, and peak position shifts to higher frequencies while its intensity decreases with increasing applied voltage due to restructure and reordering of charges at surface states or traps. These changes in the parallel conductance with frequency and applied bias voltage are expected behaviors according the surface states or trap model. The N_{ss} and τ were determined from the intensity and position of this peak with following relations, respectively (Nicollian and Goetzberger, 1965; Card and Rhoderick, 1971; Kar and Dahlke, 1972; Nicollian and Brews, 1982; Demirezen et al., 2017);

$$N_{ss} = \frac{\left(G_p/\omega\right)_{max}}{0.402\ qA} \qquad (2a)$$

$$\tau = \frac{1.98}{\omega_p} \qquad (2b)$$

In order to see the change of N_{ss} and τ with applied voltage, the N_{ss}-τ-V plots were drawn and shown in Fig. 4.

As can be seen in Fig.4, both N_{ss} and τ values decrease with increasing applied voltage. These results confirm that the N_{ss} is influential in the depletion region and at low frequencies. The N_{ss} and τ were determined as $1.65\text{x}10^{13}$ eV^{-1} cm^{-2} and 31.4 µs at 1.7 V and $1.39\text{x}10^{13}$ eV^{-1} cm^{-2}, 9.18 µs at 3 V, respectively. It can be said that the determining the voltage or energy dependent profile of N_{ss} and τ in the wide range of frequency and applied bias voltage is very substantial to take more accurate and reliable results on the performance of the MS structure with an interfacial layer. In addition, the orders of calculated values of N_{ss} and τ of the prepared Al/CdZnO/p-Si (MIS) type structure at room temperature are more suitable for MS, MIS, and similar electronic devices in the application.

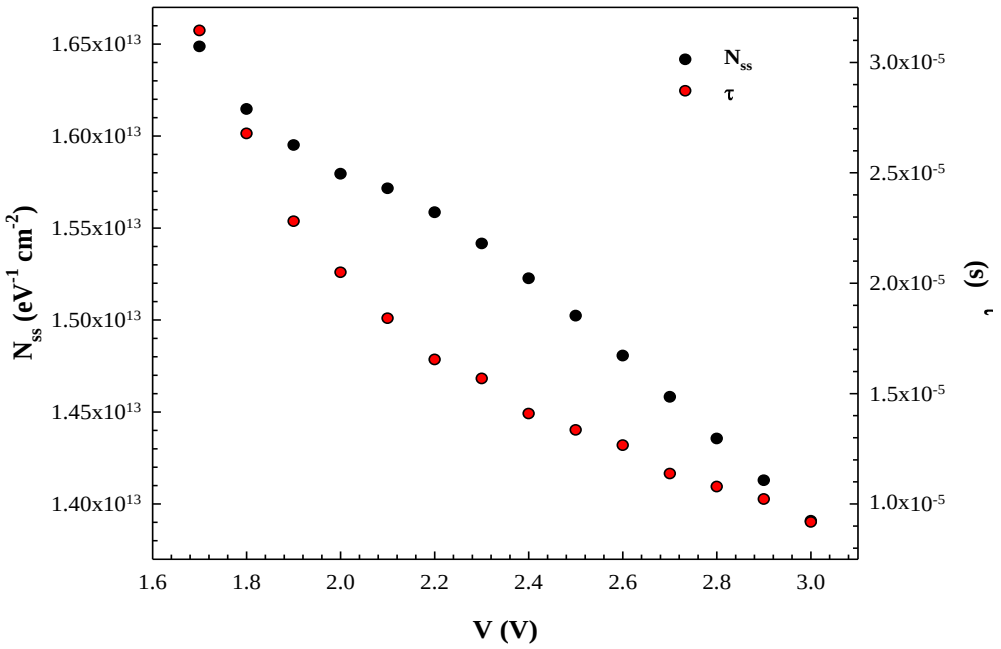

Figure 4: The voltage dependent profiles of N_{ss} and their relaxation time obtained from admittance method for the Al/CdZnO/p-Si (MIS) type structure at room temperature.

CONCLUSION

Voltage dependent profiles of the N_{ss} and τ are obtained with admittance method using C-Ln (f) and G/ω-Ln (f) plots for various voltages. Both the C and G/ω values were found strong function of voltage and frequency and they decrease with increasing frequency due to the presence of the N_{ss} depend on their relaxation time especially at low frequencies and higher forward bias voltages. But, this contribution at higher frequencies was found can be neglected. In addition, the obtained parallel conductance vs Ln(f) plots show a peak, but its position and intensity depend on frequency and voltage. Thus, both the values of N_{ss} and τ were calculated from these peak intensity and position with admittance method, respectively. According to experimental results, the N_{ss} and τ were determined as $1.65x10^{13}$ eV^{-1} cm^{-2} and 31.4 μs at 1.7 V and $1.39x10^{13}$ eV^{-1} cm^{-2}, 9.18 μs at 3 V, respectively. Experimental results confirmed that N_{ss} is dominant at the low frequency and depletion region. It is clear that the obtained orders of calculated the values of N_{ss} and τ of the prepared Al/CdZnO/p-Si (MIS) type structure are more suitable for MS, MIS, and similar electronic devices in the application.

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