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Research Article

A Hardware and Mobile-Health Based System for the Analysis of EEG Signals

Turgay KAYA[1,*], Seda ARSLAN TUNCER[2]

[1] Fırat University, Faculty of Engineering, Department of Electrical-Electronics Engineering, 23119, Elazig, Turkey, 0000-0002-7732-6194

[2] Fırat University, Faculty of Engineering, Department of Software Engineering, 23119, Elazig, Turkey, 0000-0001-6472-8306

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ABSTRACT

Instantaneous monitoring of EEG signals is very important for patient follow up. Independent follow-up systems are needed for the physician to monitor and diagnose the patient continuously. In this article, a real-time design for an FIR (Finite Impulse Response) filter was presented using a cosh window function implemented on an FPGA (Field Programmable Gate Array) environment. The reason for using the cosh window is that it has better ripple ratio and larger sidelobe roll-off ratio than other windows in literature. Since cosh window parameters can be changed in the developed design, they can be easily adapted to the new state change. After filtering the raw EEG signals, they were converted into a form that could be interpreted by a specialist physician. The filtered data was uploaded to a server on the internet so that the physician could access the EEG signals remotely via a mobile phone. The proposed system facilitated examination of the patient by the physician and made it possible to help instantly diagnose any illness.

Introduction

EEG signals are biological indicators of low amplitude taken from the brain's surface by means of electrodes. In general, the amplitudes of the EEG signals are at the microvolt level and classified into five sub-bands: delta = (0.5 to 4 Hz), theta = (4 to 8 Hz), alpha = (8 to 12 Hz), beta = (12 to 32 Hz) and gamma = (32 to 100+ Hz). The low amplitude of these signals makes it difficult to analyze the signals correctly. However, EEG signals are used in many areas, such as epilepsy, head trauma and sleep related disorders [1–3]. Raw EEG signals obtained from the patient include noise generated by the network frequency and various other causes in the environment. Noise should be removed from the raw signals so that the EEG signals from the patient can be diagnosed correctly.

The numerical filter types used in published literature for signal noise removal are either FIR (Finite Impulse Response) or IIR (Infinite Impulse Response). FIR filters are used in many applications due to their stable behavior. In the Fourier series method used in FIR filter design, window functions are used to eliminate Gibbs oscillations occurring due to the limited number of received terms [4]. These functions are preferred in many areas, such as the classification of cosmic data [5, 6], in weather forecasting models [7], in the biomedical field [8] and in speech processing [9].

* Corresponding author
Turgay KAYA
✉ tkaya@firat.edu.tr

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Window functions are divided into two groups: those with fixed and those with adjustable parameter windows [10]. Fixed windows control the width of the main lobe through window length N, while adjustable window functions can provide a more useful window amplitude spectrum with two or more independent variables. Among adjustable window functions, two-parameter windows include Dolph-Chebyshev [11], Kaiser [12, 13] and Saramaki [14]. The cosh window, which was developed from the Kaiser window equation, is widely used in published scientific literature [15]. This window function provides a better performance for adjusting the spectral parameters than other windows in literature, such as the width of the main lobe, the fluctuation rate and the side lobe reduction rate with the help of the αc variable parameter. More successful results are obtained when signal noise is eliminated with the help of FIR filter designs using window functions with good characteristics.

FPGA hardware is commonly used in processing real-time signals. FPGAs are used in many different areas, such as chaotic system applications [16], random number generators [17] and emotional robot control applications [18]. FPGAs are also used in digital filter design and applications because of their advantages, like hardware features, speed and ease of use [19, 20].

It is very important that noise can be removed from the EEG signals being processed, because this allows the doctor to interpret and diagnose the disease through signal analysis. There have been recent studies on obtaining bioelectrical signals in real time and presenting and interpreting them in the mobile environment [21–25].

To the best of our knowledge, no studies have been reported so far in literature on the hardware-based analysis of EEG signals and their presentation via the mobile environment. Therefore, this has motivated us to look at further studies and investigations.

The contribution of this article to literature includes:

– The processing of EEG signals, one of the biomedical signals, in an FPGA hardware environment

– The elimination of EEG signal interference in the FPGA environment by using an FIR filter design based on the cosh window function

– A design with IP cores utilizing the floating point number system

– The proposed use of an android-based mobile system for independent access by doctors to the filtered EEG signals.

For this purpose, we suggested a system to remove noise in the EEG signals and for the doctor to diagnose illnesses through analysis of these signals independent of their location. Firstly, noise was removed from the EEG signals with the help of the FIR filter designed using the cosh window function in the FPGA environment. Secondly, the filtered signal was recorded by a computer from the FPGA environment and then stored in a database on the internet. Consequently, it is then possible to access the data at any time with the developed android software, and doctors can access the EEG signal records in the database independent of their location. As a result, interpretation of the EEG signals for disease diagnosis was facilitated and an instantaneous follow-up on the patient was provided.

FIR Filter

The use of a Window Function in the FIR Filter Design

The most preferred method for FIR filter design is the Fourier series method. This presents less of a computational burden than other optimization methods. In the Fourier series method, Gibbs oscillations occur in response to the ideal prototype filter amplitude when using a limited number of series. Window functions are used to remove these oscillations. The non-causal filter impulse response is obtained using the window function in Equation 1:

$$h_{nc}(nT) = w(nT)h_{id}(nT) \quad (1)$$

where $h_{id}(nT)$ indicates the infinite impulse response of the ideal filter. The amplitude response of the ideal filter is shown in Equation 2:

$$h_{id}(nT) = \begin{cases} w_{ct}T/\pi & for\ n = 0 \\ \dfrac{sinw_{ct}nT}{n\pi} & for\ n \neq 0 \end{cases} \qquad (2)$$

The non-causal ideal filter response is made to be causal by shifting it $h_{nc}(nT)$ (N–1)/2 times. The causal filter equation can be obtained by using Equation 3:

$$h(nT) = h_{nc}[\left(n - \frac{N-1}{2}\right)T] \qquad (3)$$

The window function used in the filter design and the fluctuation in the pass and stop bands, will be approximately the same [12].

Cosh Window

The cosh window function is obtained by writing the cosh function in the Kaiser window function rather than the zero-order first type improved Bessel function ($I_0(x)$) [15].

$$\omega_c(n) = \begin{cases} \dfrac{cosh\left(\alpha_c\sqrt{1-\left(\frac{2n}{N-1}\right)^2}\right)}{cosh(\alpha_c)} & |n| \leq \dfrac{N-1}{2} \\ 0 & otherwise \end{cases} \qquad (4)$$

where α_c is the adjustable parameter and N is the length of the window.

Implementation of the FIR Filter and Cosh Window Function in FPGA

The first step in the FIR filter design was to design the window function to be used. In this section, the design of the cosh window, which is widely used in published literature, and has good spectrum parameters, was implemented step by step in the FPGA environment. The reason for using the cosh window is that it has better better ripple ratio and larger sidelobe roll-off ratio than other windows in literature.

For the cosh function, first the expression $\alpha_c\sqrt{1-\left(\frac{2n}{N-1}\right)^2}$ in Equation 4 was calculated with values of N=29 and α_c=4.5, followed by the calculation of a value for w_c(n). Since cosh window parameters can be changed in the developed design, they can be easily adapted to the new state change. Figure 1 shows the circuit designed to calculate $\alpha_c\sqrt{1-\left(\frac{2n}{N-1}\right)^2}$ in the Quartus environment.

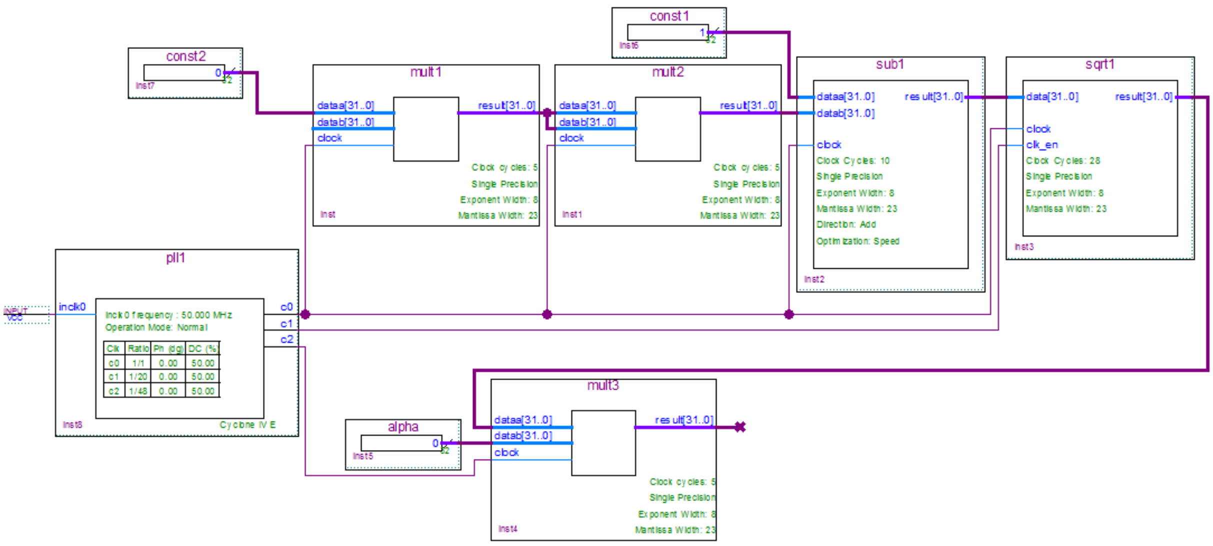


Figure 1: the realization of $\alpha_c\sqrt{1-\left(\frac{2n}{N-1}\right)^2}$

Available modules that can operate with floating point numbers were used to implement the circuit. Three multiplication modules, one subtraction module and one extraction module were used in the circuit. To calculate the result of applied values to the inputs of each multiplication, subtraction and extraction module, 5, 10 and 28 clock cycles were needed, respectively. A phase locked loop (PLL) circuit was also used to synchronously calculate w(n). The PLL has the ability to divide or multiply the clock signal applied to its input. The clock signal was converted to clock signals c0, c1 and c2 by utilizing this feature so that the circuit can operate synchronously. The clock signal used in the system was 400 MHz, while the signals c0, c1 and c2 were 400, 20 and 7.548 MHz, respectively. The values obtained from the input values were then used as inputs to the exponential modules in Figure 2 to calculate w_c (n). As already known, the cosh function can be written as shown in Equation 5:

$$cosh(x) = \frac{e^{x} + e^{-x}}{2} \qquad (5)$$

The circuit scheme used to obtain the result of Equation 4 by using Equation 5 is shown in Figure 2. In this circuit, exponential, summation and division modules were used. These modules gave clock cycle values of 17, 10 and 6, respectively. For n=0, 1, 2 ,… (N-1)/2, $w_c(n)$ is calculated at 228.7 kHz.

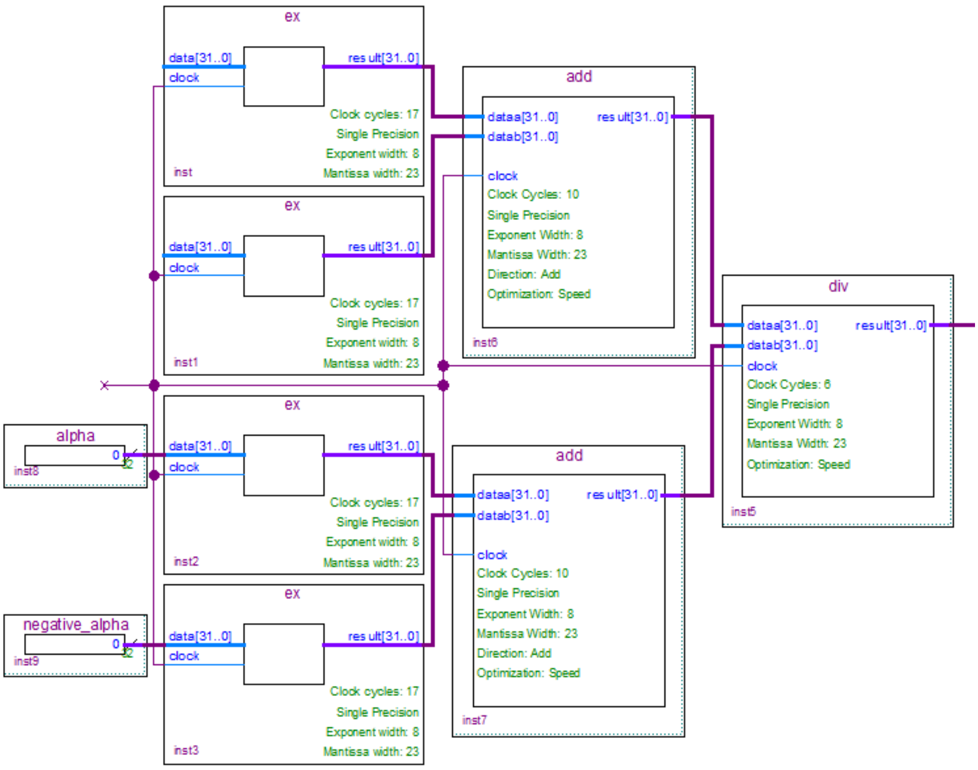


Figure 2. The implementation of Equation 4 in FPGA

To show the consistency of the results obtained with mathematical results, each result was recorded in a memory circuit at 228.7 kHz. Figure 3 shows the memory hardware required to write each value to memory. A 5-bit counter was used to write the results to the desired addresses in the memory. The counter frequency was the same as the memory clock frequency.

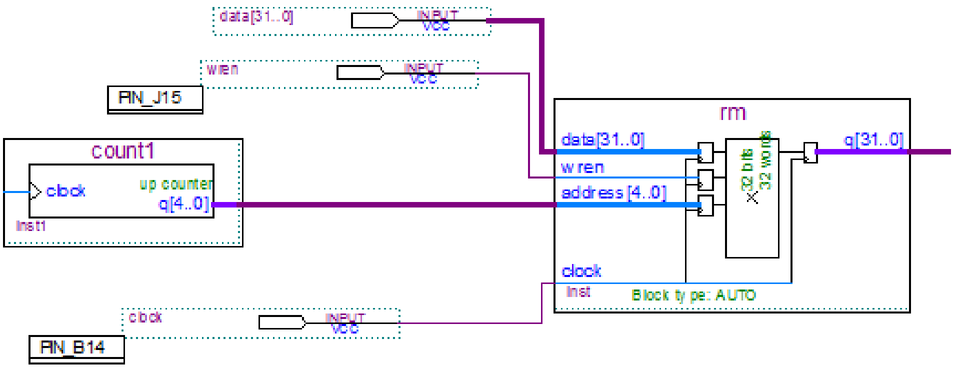


Figure 3. The design used to write the results into memory

In this application, the results were obtained using values of N=29 and α_c=4.5. Figure 4 shows the results written into each address of the memory in the hexadecimal number system.

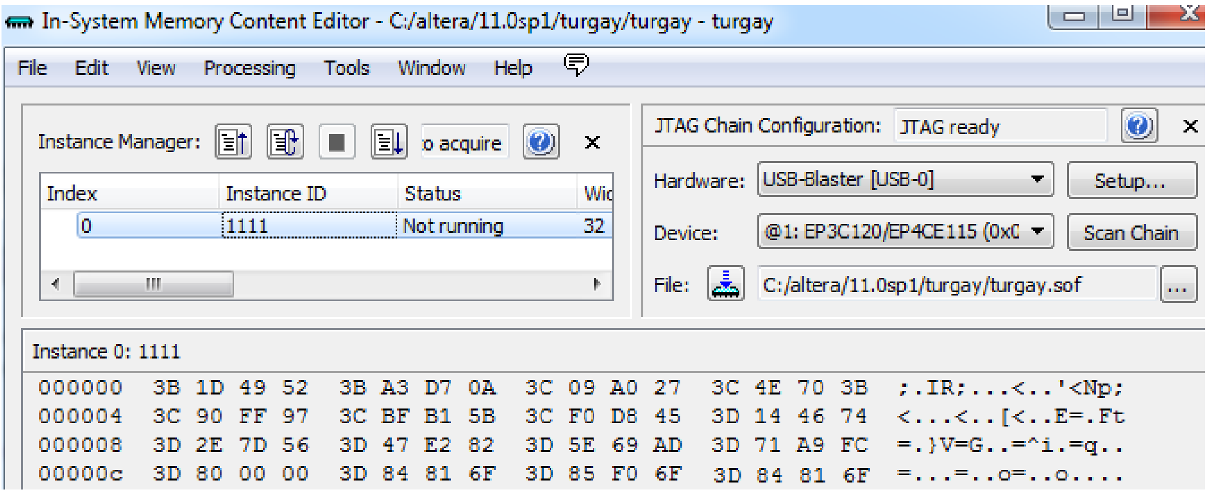


Figure 4. Hexadecimal results written into memory for values N=29 and α_c=4.5

The results obtained from the q output in Figure 3 are shown in Figure 5. First, eight values obtained at 228.7 kHz are seen. Because the q output is formed from a 32 byte bus structure, the corresponding hexadecimal values for each calculated value are given.

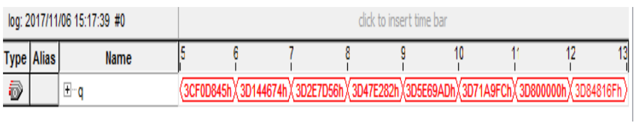


Figure 5. Real-time results calculated for values of N=29 and α_c=4.5

The Application Results

The first step in the method used by the physician to analyze the EEG signals is the design of the cosh window and the FIR filter using this window, as described in Section 3. Figure 6 shows the block diagram of the structure implemented in the FPGA environment and used for removal of noise from the raw EEG signal.

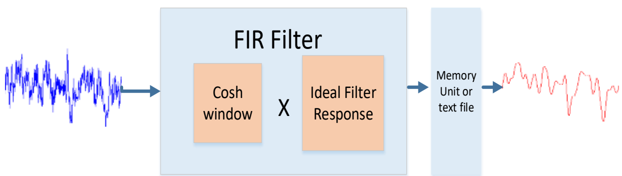
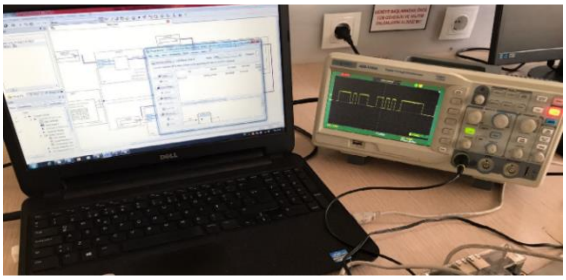


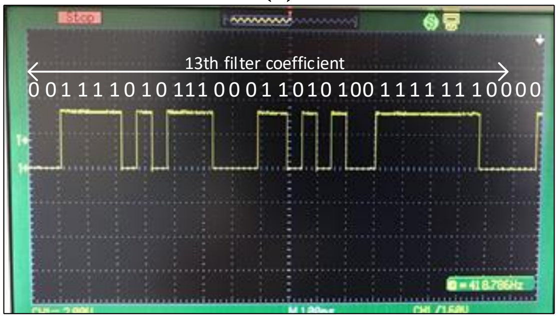
Figure 6. The block diagram representing the filtering of the EEG signal in the FPGA environment

The experimental environment for the system design is shown in Figure 7a, while the binary number system representation for the FIR filter coefficient example at the output of the storage unit where EEG signals are stored is shown in Figure 7b. This coefficient is $(3D71A9FC)_H$ –

based on the hexadecimal number system in the IEEE 754 format – and it is 0.059 according to the floating number system.



(a)



(b)

Figure 7. a) The experimental setup **b)** 13th filter coefficient

The second step of this system design is the remote access to the data by a doctor. For this step, an android-based system was developed so that the doctor can follow the patient remotely and diagnose any disease. In Figure 8, the system is shown to consist of an android application, a server where the data is stored, and an FPGA. The noise-free EEG signal (a file in txt format) is recorded in a database on the internet with the help of a user interface designed on a workstation. The sampled EEG signals in the file are in an array format. The samples obtained by splitting this sequence are stored in a table along with the patient ID. The doctor connects to the database with the android application, using his/her domain name. In this procedure, the doctor can obtain the patient ID and the EEG signals in the table in the Json data format. Json is a data format created for JavaScript applications that takes up less space than XML when transferring data. Thus, it is possible to display and interpret the EEG signals in the Json format using the android application using a mobile phone independent of location.

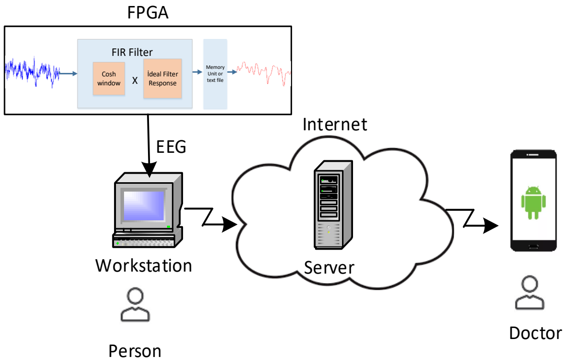
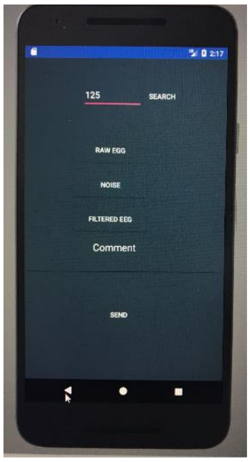


Figure 8. The block representation for the suggested system

The interface that allows the doctor to access the EEG signals using the android application is shown in Figure 9a). In Figures 9b–d, the patient's raw EEG signal, noise-free EEG signal and noise signal are shown using the patient's patient ID number, respectively.



(a)

(b)

(c)

(d)

Figure 9. a) The interface for the android application **b)** The raw EEG signal **c)** The unfiltered EEG signal and **d)** The noise signal

Conclusion

In this study, a system was proposed to remove the noise from the EEG signals taken from the patient and allow the doctor to follow and diagnose the patient independent of location. With this proposed system, the received EEG signal was processed using the window and FIR filter designed in the FPGA environment. The processed EEG signals were stored in a database so that the physician could access the online data with android software. The ability for the doctor to be able to follow up a patient's progress is of great importance in terms of monitoring any disease. This study makes it easy to instantly monitor, analyze and diagnose the EEG data.

The developed system has two important contributions to make to published literature. The first contribution is that the system is designed in hardware and allows the data to be processed in real time. The second contribution is that the physician can remotely access the patient's data independent of location to diagnose any disease.

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