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Multi Transformer Cell Inverter with Reduced DC sources

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ABSTRACT

This paper proposes a new isolated multi transformer cell inverter employing low-frequency single-phase transformers and two DC voltage sources. This inverter includes several transformer cells. Some of cells contain two unidirectional switches that generate two voltage levels and only one of cells has six switches that provide five voltage levels. Also, the multi transformer cell inverter provides a high number of output levels, symmetric and asymmetric states, reduction of DC sources and high modularity. The operation and performance of the suggested inverter has been proved by simulation and experimental results.

Keywords*: Multi transformer cell inverter, Cascaded transformer multilevel inverter, Reduction of DC sources and components*

1. INTRODUCTION

In recent years, there has been a growing interest in power electronic systems due to the increasing utilization of electrical and electronic equipment. This growing demand has favored the development of new power electronic devices, as well as novel power converter topologies. Multilevel inverters are one of the power electronic devices which can be considered as voltage synthesizers. The first multilevel inverter was introduced in 1981 by Nabae [1]. Since then, the multilevel voltage inverter has been receiving wide attention in research. Multilevel inverters include an array of power semiconductors and DC voltage sources (or capacitor), the output of which generate voltages with stepped waveforms [2-4]. There are several types of multilevel inverters. Three base topologies have been proposed for multilevel inverters: diode-clamped [5-8]; flying capacitors [8-10]; and cascaded multilevel with separate DC sources [11-14]. One of the important problems in multilevel inverters is the number of components. In other word, number of components in a multilevel inverter plays important roles on the cost and realization of the inverter. In the flying capacitor topology, an unacceptable amount of capacitors is required for high voltage levels. The cascaded multilevel with separate dc sources synthesizes a desired voltage from several independent sources of DC voltages and requires the least number of total main components even though the cascaded multilevel with separate dc sources needs more DC-link capacitors or DC sources as compared to those needed in the diode-clamped. In recent years, many topologies are suggested to multilevel converter with a low number of switches, gate driver circuits and DC voltage sources [15-18]. Recently cascaded transformer multilevel topology is proposed [19-21]. This has the advantage of having single storage capacitor or DC voltage source. This topology has transformers in its structure.

This paper presents a novel multi transformer cell topology with transformers in its cells that can be used to isolation and voltage transformation. This topology consists of two DC voltage sources, isolated single-phase low-frequency transformers and semiconductor switches. By the proposed circuit configuration, a number of switches and DC sources can be reduced, compared with traditional cascaded H-bridge multilevel inverters. Also, with respect to cascaded transformer

multilevel topology, number of semiconductor switches reduces. This paper includes simulation and experimental results based on a laboratory prototype to prove the feasibility of the proposed multilevel inverter.

There are several modulation strategies for multilevel inverters [22-24]. In this paper, the fundamental frequency switching technique has been used.

2.CONVENTIONAL MULTILEVEL INVERTER

Figure 1 shows the circuit structure of an inverter leg of a cascaded multilevel inverter. *n* identical inverter modules are connected in series (cascade) to form a single-phase multilevel inverter. All modules are fed by DC voltage sources of the same magnitude. This Multilevel inverter has been called symmetrical multilevel inverter.

Since this topology consist of series power conversion modules, the voltage and power level may be easily adjusted. An apparent disadvantage of this topology is the large number of isolated voltages required to supply each modules. Although this topology requires multiple dc sources, in some systems they may be available through renewable energy sources. When ac voltage is already available, multiple DC sources can be generated using isolated transformers and rectifiers. However, the modules can be supplied by phase-shifted transformers in medium-voltage systems in order to provide high power quality at the utility connection. Recently cascaded transformer multilevel topology is proposed [19-21]. Figure 2 shows a configuration of the cascaded transformer multilevel inverter. It consists of *n* full-bridge cells and their corresponding transformers. Each full-bridge cell is connected with a single input voltage source (V_{DC}) in parallel. Owing to the cascaded transformers, it has a galvanic isolation between an input DC source and output loads.

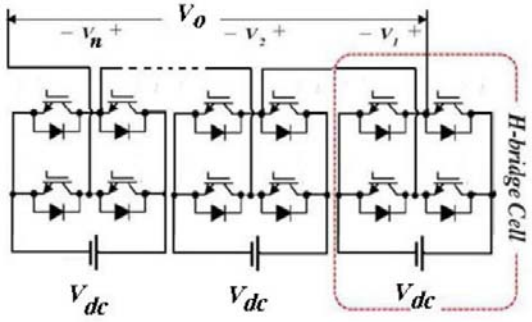


Figure1. Configuration of cascade inverter.

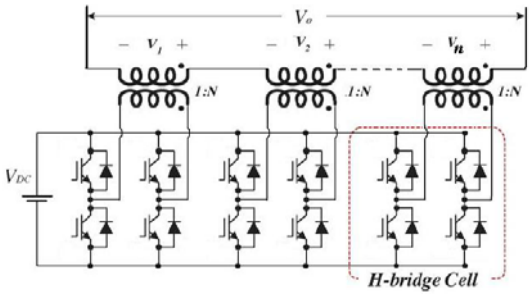


Figure 2. Configuration of cascaded transformer multilevel inverter

3. PROPOSED MULTILEVEL INVERTER

In recent years, multilevel inverters have received more and more attention because of their capability of high voltage operation, high efficiency and low electromagnetic interference (EMI) [1-4]. The desired output of a multilevel inverter is synthesized by several sources of DC voltages. With an increasing number of voltage steps, the inverter voltage output waveform approaches a nearly sinusoidal waveform while using a fundamental frequency switching scheme. These results in low switching losses and the switches experience lower voltage stresses. The required number of components depends on the output voltage level. For the high number of output voltage steps high numbers of components are needed. However, increasing the number of components also increase the inverter circuit size, cost and control complexity.

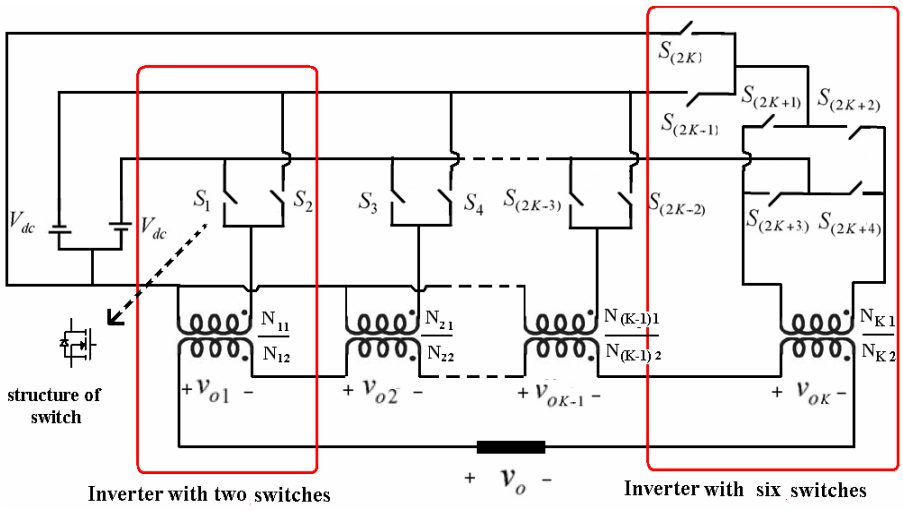


Figure 3. Proposed multilevelinverter.

To obtain a desired number of output levels without increasing the number of components, novel topology for multilevel inverters proposed in this paper. The main purpose of the new family of multilevel inverters is to reduce the number of switching devices used without changing the staircase nature of the output voltage.

Single phase topology of a proposedinverter is shown in Figure 3. This consists of two type cell: cells with two switches and one cell with six switches. These cells have single phase transformer in their structures. Whole of cells are supplied by two DC sources. Two values can be achieved for output voltage in cells with two switches. The cell with six switches can produce five values in its output. Each switch in the suggested topology can be composed of one IGBT or power MOSFET and one anti-parallel diode.

Table 1 indicates the values of v_{o1} for states of switches S_1 and S_2. Both switches S_1 and S_2 cannot be on simultaneously because a short circuit would be produced.

Table 2 shows the values of v_{oK} for cell with six switches.

Table 1. $v_{O1}$for states of switches S_1 and S_2.

on switches	v_{O1}
S_2	$\frac{N_{12}}{N_{11}}V_{dc}$
S_1	$-\frac{N_{12}}{N_{11}}V_{dc}$

An output phase voltage is achieved by summing the output voltages of transformers. Output phase voltage is obtained by:

$$v_O = v_{O1} + v_{O2} + \ldots + v_{Ok} \quad (1)$$

If all turns ratio of all transformers are the same, the maximum number of levels of phase voltage is given by:

Table 2.v_{oK} for cell with six switches

on switches	$v_{O\,K}$
S_{2K-1}, S_{2K+2}, S_{2K+3}	$2\frac{N_{K2}}{N_{K1}}V_{dc}$
S_{2K}, S_{2K+2}, S_{2K+3}	$\frac{N_{K2}}{N_{K1}}V_{dc}$
S_{2K+1}, S_{2K+2} or S_{2K+3}, S_{2K+4}	0
S_{2K}, S_{2K+1}, S_{2K+4}	$-\frac{N_{K2}}{N_{K1}}V_{dc}$
S_{2K-1}, S_{2K+1}, S_{2K+4}	$-2\frac{N_{K2}}{N_{K1}}V_{dc}$

$$m = 2K + 3 \quad (2)$$

k, *m* are the number of transformers and the maximum number of levels of phase voltage, respectively. These Multilevel inverters have been called symmetrical multilevel inverter. The maximum output voltage (V_{Omax}) is:

$$v_{o\,max} = (K+1)\frac{N_{K2}}{N_{K1}}V_{dc} \quad (3)$$

To provide a large number of output levels without increasing the number of components, asymmetric multilevel inverters can be used. The turn's ratio of transformers is proposed to be chosen according to a geometric progression with a factor of two.

For n cascaded transformers, the number of voltage levels is given as follows:

$$m = 2^{K+1} + 1 \qquad N_{i2}=2^{i}N_{k2}\ ,i=1,2,....,K\text{-}1 \quad (4)$$
and $N_{11}=N_{21}=\ldots\ldots=N_{K1}$

The maximum output voltages of these *K* cascaded multilevel inverters are:

$$v_{o\,max} = \left(\frac{N_{K2}}{N_{K1}} + \sum_{i=1}^{K}\frac{N_{i2}}{N_{i1}}\right)V_{dc} \quad (5)$$

The main purpose of this paper is reduction of the components of the cascaded multilevel inverters. The proposed converter can generate DC voltage levels the same as cascaded topology with less number of semiconductor switches. Proposed inverter employs two single DC input voltage source, isolated single-phase low-frequency transformers and unidirectional switches. By the proposed circuit configuration, a number of switches and DC sources can be reduced, compared with traditional cascaded H-bridge multilevel inverters. The number of switches in cascaded transformer H-bridge converter and proposed topology respectively are obtained by:

$$No.\ of\ \ switches\ \ = 4K \quad (6)$$

$$No.\ of\ \ switches\ \ = 2K + 4 \quad (7)$$

From comparison between (6) and (7), you can find that the suggested topology needs fewer switches for generating same levels of output voltages. Table 3 shows comparison between proposed structure and cascaded topology in some cases. For example if we want to generate the 17 levels with conventional cascaded transformer inverters, we can find that they need more switches compared with the proposed schemes as given in Table 3.

Figure 4 shows the circuit structure of an inverter leg of proposed topology with three transformers. Three identical cells and one cell with six switches are connected in series to form single-phase multilevel inverter.

By using single-phase transformer of the same turn ratio, 9-level multilevel inverter can be obtained. The output voltage has nine voltage levels from -4 V_{dc} to +4 V_{dc}. Table 4 illustrates the switching patterns of all nine discrete levels. Figure 5 shows a typical 9-level waveform which can be obtained with proposed symmetric converter with V_{dc}=10V.

Table 3. Comparison between proposed structure and cascaded H-bridge topology.

Cascade H-bridge				Proposed topology			
Symmetric		Asymmetric(Binary)		Symmetric		Asymmetric(Binary)	
Levels	Switches	Levels	Switches	Levels	Switches	Levels	Switches
9	16	7	8	9	10	9	8
17	32	15	12	17	18	17	10
33	64	31	16	33	34	33	12

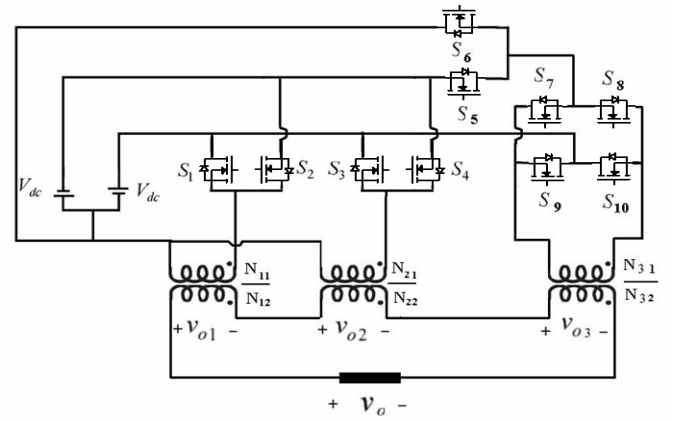


Figure 4. Circuit structure of an inverter with three single phase transformer

Table 4. Switching pattern for 9-level inverter.

Level	ON switches	Level	ON switches
$-4V_{dc}$	$S_1\ S_3\ S_7\ S_{10}\ S_5$	0	$S_2\ S_3\ S_9\ S_{10}$
$-3\ V_{dc}$	$S_1\ S_3\ S_7\ S_{10}\ S_6$	$+\ V_{dc}$	$S_2\ S_3\ S_8\ S_9\ S_6$
$-2\ V_{dc}$	$S_1\ S_4\ S_7\ S_{10}\ S_5$	$+2V_{dc}$	$S_2\ S_3\ S_8\ S_9\ S_5$
$-\ V_{dc}$	$S_1\ S_4\ S_7\ S_{10}\ S_6$	$+3V_{dc}$	$S_2\ S_4\ S_8\ S_9\ S_6$
0	$S_1\ S_4\ S_7\ S_8$	$+4V_{dc}$	$S_2\ S_4\ S_8\ S_9\ S_5$

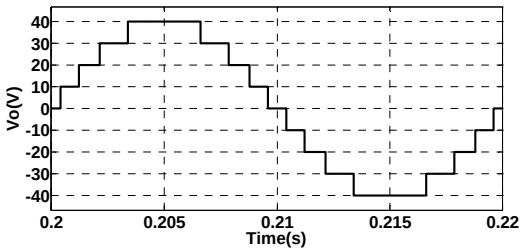


Figure 5. 9-level output voltage.

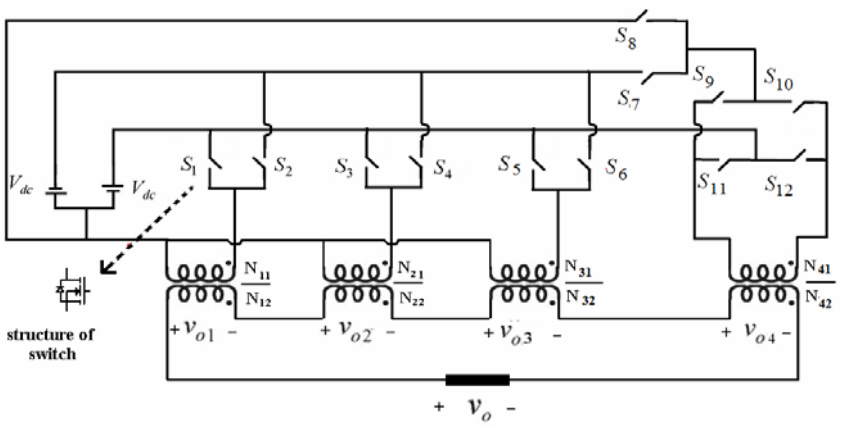


Figure 6. Circuit structure of an inverter with four single phase transformer

Table 5. Switching pattern for 33-level inverter.

Level	ON switches	Level	ON switches
0	S_1 S_3 S_6 S_7 S_9 S_{12}	-16 V_{dc}	S_1 S_3 S_5 S_7 S_9 S_{12}
+1V_{dc}	S_1 S_3 S_6 S_8 S_9 S_{12}	-15 V_{dc}	S_1 S_3 S_5 S_8 S_9 S_{12}
+2 V_{dc}	S_1 S_3 S_6 S_8 S_{11} S_{12}	-14 V_{dc}	S_1 S_3 S_5 S_8 S_9 S_{10}
+3 V_{dc}	S_1 S_3 S_6 S_8 S_{10} S_{11}	-13 V_{dc}	S_1 S_3 S_5 S_8 S_{10} S_{11}
+4 V_{dc}	S_1 S_3 S_6 S_7 S_{10} S_{11}	-12 V_{dc}	S_2 S_3 S_5 S_7 S_9 S_{12}
+5 V_{dc}	S_2 S_3 S_6 S_8 S_9 S_{12}	-11 V_{dc}	S_2 S_3 S_5 S_8 S_9 S_{12}
+6 V_{dc}	S_2 S_3 S_6 S_8 S_{11} S_{12}	-10 V_{dc}	S_2 S_3 S_5 S_8 S_9 S_{10}
+7 V_{dc}	S_2 S_3 S_6 S_8 S_{10} S_{11}	-9 V_{dc}	S_2 S_3 S_5 S_8 S_{10} S_{11}
+8 V_{dc}	S_2 S_3 S_6 S_7 S_{10} S_{11}	-8 V_{dc}	S_1 S_4 S_5 S_7 S_9 S_{12}
+9 V_{dc}	S_1 S_4 S_6 S_8 S_9 S_{12}	-7 V_{dc}	S_1 S_4 S_5 S_8 S_9 S_{12}
+10 V_{dc}	S_1 S_4 S_6 S_8 S_{11} S_{12}	-6 V_{dc}	S_1 S_4 S_5 S_8 S_9 S_{10}
+11 V_{dc}	S_1 S_4 S_6 S_8 S_{10} S_{11}	-5 V_{dc}	S_1 S_4 S_5 S_8 S_{10} S_{11}
+12 V_{dc}	S_1 S_4 S_6 S_7 S_{10} S_{11}	-4 V_{dc}	S_2 S_4 S_5 S_7 S_9 S_{12}
+13 V_{dc}	S_2 S_4 S_6 S_8 S_9 S_{12}	-3 V_{dc}	S_2 S_4 S_5 S_8 S_9 S_{12}
+14 V_{dc}	S_2 S_4 S_6 S_8 S_{11} S_{12}	-2 V_{dc}	S_2 S_4 S_5 S_8 S_9 S_{10}
+15 V_{dc}	S_2 S_4 S_6 S_8 S_{10} S_{11}	-1 V_{dc}	S_2 S_4 S_5 S_8 S_{10} S_{11}
+16 V_{dc}	S_2 S_4 S_6 S_7 S_{10} S_{11}	0	S_2 S_4 S_5 S_7 S_{10} S_{11}

Figure 6 shows circuit structure of an inverter with four single phase transformer. By using the single-phase transformers with the ratio of 2:4:8:1and by controlling the switching of the cells, 33 discrete voltage levels can be produced. Table 5 illustrates some switching patterns of 33-levels inverter.Figure7 shows output phase voltage in asymmetric state with V_{dc}=10V.

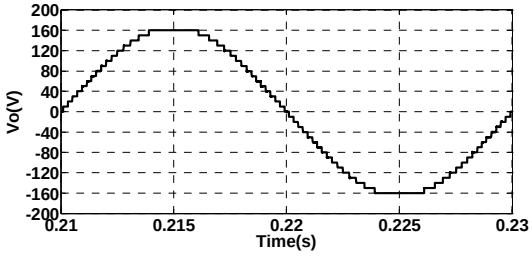


Figure7. 33-level output voltage

The proposed multilevel inverter can be used in some systems such as energy conversion of DC sources (renewable energy sources, batteries and DC link capacitor), dynamic voltage restorer (DVR) and etc.

A suitable power electronic converter is required between DC sources and load or grid in energy conversion [25-30]. Voltage regulation and galvanic isolation between sources and load or grid are needed in energy conversion. The voltage of renewable energy sources such as photovoltaic panels or full cells is low and step-up voltage transformers are needed to increase voltage level [29, 30]. The proposed multilevel inverter has transformers in its structure and voltage regulation achieve by proper switching and regulation turns ratio of transformers. The galvanic isolation between DC sources and load or grid obtains by transformers, too.

4. EXPERIMENTAL RESULTS

In order to verify the operation of the proposed inverter, single phase 9-level inverter was properly implemented with two 12 volt voltage sources. The load is a series R–L with magnitudes 72.8 Ω and 4.4 mH, respectively. The inverter utilizes MOSFET IRFP460 for main switches. The ATMEG 32-8PT microcontroller by ATMEL Company is used to implement inverter controller as PWM generator and the opto coupler TLP521-1 is used to drive switches.

Figure8 shows a prototype of the proposed multilevel inverter. It includes two single-phase transformers with 17:5 ratios and a single-phase transformer with 34:10 ratios for two switches cells and six switches cell respectively, ten switches, two DC sources and an ATMEGA based controller.

Figure 8 shows the transformer primary voltage of different cells. Cells 1 and 2 generate a square waveform. As shown in Figure9 (a) and (b), the transformer primary voltage of each cell for all times has negative or positive values. Cell 3 generates a 5-level waveform. As shown in Figure9 (c), the transformer primary voltage of this cell has negative, positive or zero values. Figure10 shows the measured output voltage. This is a nine levels 50 Hz voltage with amplitude 14.12 V. Figure 11 shows load current.

As it can be seen, the results verify the ability of proposed inverter in generation of desired output voltage. Consequently, we can say that the proposed topology is more advantageous in switch and DC voltage source cost compared with the conventional cascaded multilevel inverter because the proposed topology can reduce the number of switches and DC voltage sources.

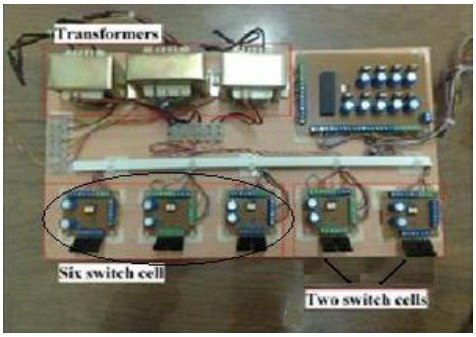
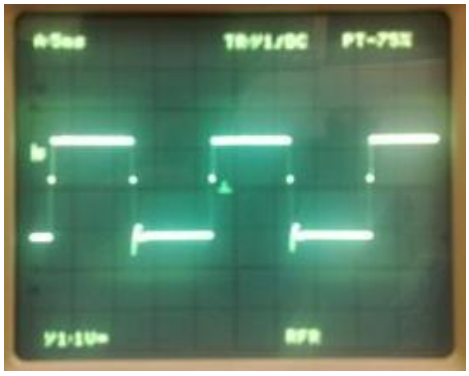
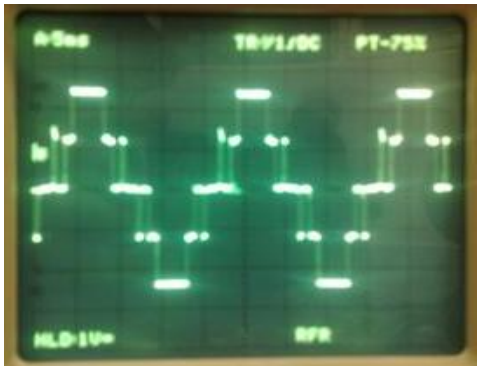


Figure8. The prototype



(a)

(b)



(c)

Figure 9. The transformer primary voltage of (a), (b) two switches cells (c) six switches cell, 1*10 volt/div

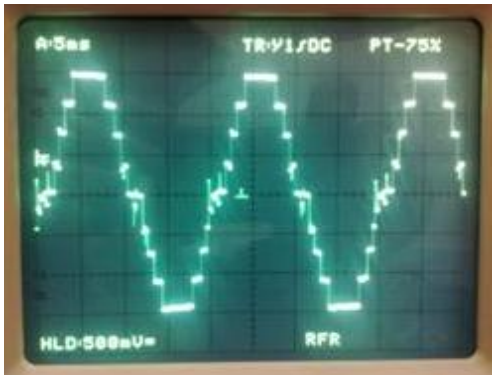


Figure 10. The output voltage, 0.5*10 volt/div

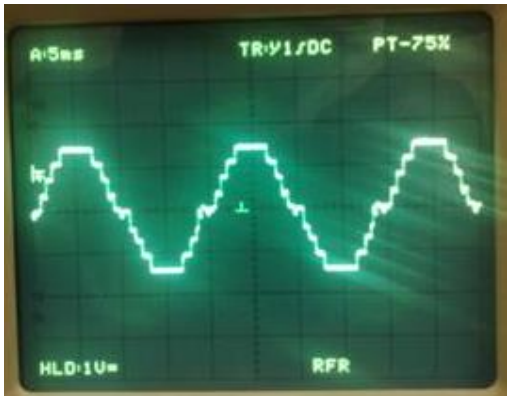


Figure 11. Measured load current, 1*10 volt/div (0.138 A/div)

5. CONCLUSION

This paper proposed a cascaded transformer multilevel inverter employing low-frequency single-phase transformers and two DC voltage source. The proposed configuration can reduce a number of switches compared with conventional cascaded transformer multilevel inverter or H-bridge multilevel inverters. Also, two algorithms have been presented for determination of the value of the turn ratio of transformers. The operation and performance of the proposed multilevel inverter has been verified on a single-phase 9-level multilevel inverter lab prototype. The proposed multilevel inverter may be available for energy conversion through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices such as capacitors or batteries.

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