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ORIGINAL ARTICLE

Two Flying Capacitors Cascaded Sub-Multilevel Inverter with Five Switches for DC–AC Conversion

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ABSTRACT

This paper presents a novel topology for cascaded multilevel inverters that only two flying capacitors apply single DC source voltage to all sub-multilevel inverters. The output voltages of each sub-multilevel inverters unit, which each unit can produce five voltage levels, are cascaded using low frequency transformers. Suggested topology have advantages of both original flying capacitor and cascaded H-bridge and in the same time reduces the amount of switching devices, DC sources, capacitors and natural self-balancing of the flying capacitors. Besides, it can operates in symmetric an asymmetric states and four algorithms for calculating of turn ratio of transformers have been presented. Simulation results of the proposed inverter are presented and carried out by MATLAB/SIMULINK to verify its voltage generating ability.

Keywords: *Asymmetric state, Two flying capacitors, Cascaded transformer*

1. INTRODUCTION

Multilevel converters are very interesting alternatives for medium and high-power applications. Multilevel inverter have shown an important development in the last years with increasing applications in different systems, such as high-power ac motor drives, active power filters, reactive power compensation, FACTS devices, medium voltage drives and energy conversion [1-5]**.** The capability of these topologies to obtain high voltage in the range of kV with medium voltage and low speed semiconductors is the main reason for this. Multilevel converters can sum small DC voltage sources together and create high AC voltage with high power quality waveforms, lower harmonic components, lower switching losses, and also reduction of dv/dt stresses on the load [6, 7]. Several circuit topologies of multilevel inverter have been researched and utilized. Three different famous topologies have been proposed for multilevel inverters: diode-clamped [8]; flying capacitors [9, 10]; and cascaded H-bridge with separate DC sources [11, 13]. The diode-clamped multilevel inverter uses capacitors in series to divide up the DC bus voltage into a set of voltage levels and flying-capacitor multilevel inverter uses a ladder structure of capacitors and one DC source. The cascaded H-bridge multilevel inverter uses cascaded inverters with separate DC sources. In this case, each inverter bridge is supplied by a separate and isolated dc power supply. Clamping diodes are not required in the flying capacitors and cascaded H-bridge, while balancing capacitors are not needed in the diode-clamped and cascaded H-bridge. The cascaded H-bridge needs more DC sources as compared to others.

The main disadvantage associated with the multilevel configurations is the great number of power semiconductor switches needed. Each switch requires a gate driver circuits and they require auxiliary DC voltage sources to switching. Another important problem in inverters is the ratings of switches. Current and Voltage ratings of the switches play important roles on the cost of the inverter. So, in practical implementation, reducing the number of switches and gate driver circuits is very important.

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The flying capacitor converter and stacked multicell converter [14-19], have many interesting properties, such as the advantage of transformer less operation and the ability to keep in good condition the flying capacitors voltages at their objective without any feedback control [16, 17]. In the flying-capacitor topology, an unacceptable amount of capacitance is required for high voltage levels. Not only these many capacitors make the system less cost-effective, but also they induce a severe voltage-imbalance problem in the transient period and at the steady state. Recently, several multilevel inverter topologies based on flying-capacitor have been developed that using a reduced number of switches and gate driver circuits [18, 19]. In [18] novel configuration of multilevel multicell has been proposed. This inverter is based on a new cell obtained from the mixture of the two most popular multilevel topologies, flying capacitor and cascaded H-bridge inverter. The new cell provide a high number of output levels, high modularity and low number of components [18] but they require multiple capacitors and some switches of suggested topologies have high peak inverse voltage. In [19] a new configuration of flying capacitor multicell converter is proposed. The main advantages of the proposed converter, in comparison with flying capacitor and stacked multicell converters, are doubling the rms and the number of output voltage levels. This progress is achieved by adding only two low-frequency switches to the conventional configuration of flying capacitor [19].

In the multilevel inverters, when the number of levels increases the difference between output voltage and sinusoidal voltage reduces. One clear disadvantage of multilevel inverter in high number of levels is the larger number of required components. Increasing the number of components such as semiconductor switches, diodes, capacitors and DC voltage sources cause increasing the losses, installation area, complexity control and cost. To provide a large number of output levels without increasing the number of components, asymmetric multilevel inverters can be used. The flying capacitor converter and stacked multicell can not operate as asymmetric converter. In asymmetric multilevel converters the DC voltage sources are proposed to be chosen as different value according to different methods [21-24].

This paper suggests a new topology for multilevel inverters with a high number of levels associated with a low number of components. The proposed converter employs one single DC input power source, two capacitors, isolated single-phase low-frequency transformers and semiconductor switches. The new topology is called stacked multicell cascaded transformer (SMCT). The SMCT not only gather advantages of both original flying capacitor and cascade H-bridge, but also reduces the amount of switching devices, DC sources, capacitors and natural self-balancing of the flying capacitors. DC/DC converter can be used in SMCT to charge flying capacitors and keep constant voltage of them. Single phase transformers can be used to increase the inverter output voltage and isolation. A simple modulation strategy based in the fundamental frequency modulation is also provided to switching. To verify the ability of the proposed multilevel inverter; we carried out computer-aided simulations using MATLAB / SIMULINK.

2. FLYING CAPACITOR MULTILEVEL CONVERTERS

Figure1 illustrates the fundamental building block of a phase-leg flying capacitor inverter. The flying capacitor, involves series connection of capacitor clamped switching cells [5]. The inverter in Figure 1 provides an m-level output across *a* and *n*. This topology has several attractive features such as clamping diodes are not needed and has switching redundancy within the phase which can be used to balance the flying capacitors so that only one dc source is needed. The flying capacitor requires a large number of bulk capacitors to clamp the voltage.

Stacked multicell converter derives from flying capacitor converter and uses a $m \times n$ cells array to increase the number of output voltage levels [19]. Figure 2 shows a $2 \times n$ stacked multicell converter. The number of combinations to obtain a desired voltage level is increased, and the voltage ratings of capacitors are reduced [19]. Stacked multicell requires the same number of capacitors and semiconductors in comparison with the equivalent flying capacitor converter for the same number of output voltage levels [18- 20].

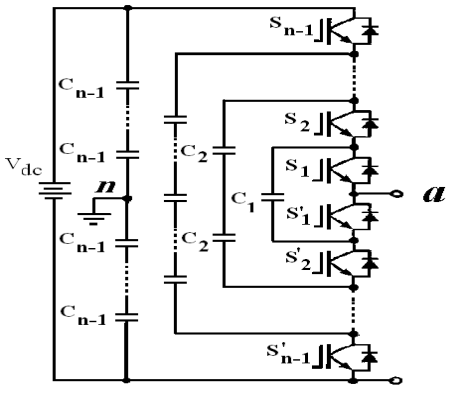


Figure 1. *n* level flying capacitor converter.

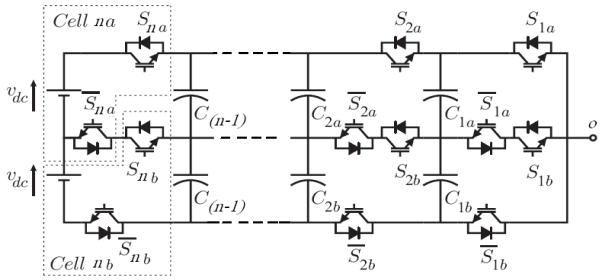


Figure 2. $2n + 1$ level stacked multicell converter with maximum output voltage value of v_{dc} .

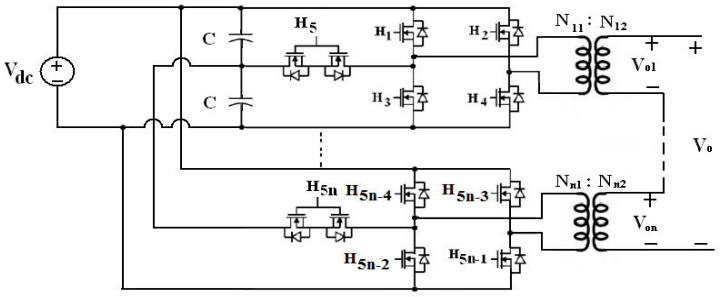


Figure 3. Circuit topology of the proposed inverter.

3. NOVEL MULTILEVEL INVERTER

Multilevel converters have some particular disadvantages. They need a large number of semiconductor switches and each switch requires a related gate driver and protection circuit. Some of them need multiple separate DC sources or capacitors. These conditions increase the cost and control complexity and tend to reduce the overall reliability. To overcome above mentioned disadvantages, SMCT topology with reduced number of switches, DC voltage sources and capacitors has been presented in this paper.

The circuit diagram of the proposed multilevel topology, SMCT, is shown in Figure 3. It consists of one DC voltage source, two level capacitor voltage divider, five switch bridge cells and their corresponding transformers. The five switch bridge cells are called FSBC. Each FSBC is connected with a single input voltage source (V_{dc}) and two capacitors in parallel. Input DC voltage charges capacitors. Each capacitor is charged to half of V_{dc} almost. The FSBC consists of H-bridge output stage with a bi-directional switch. It can be considered as voltage synthesizer and generates five voltage levels.

Single phase low frequency transformers are used in SMCT structure. The main functions of the Single phase low frequency transformers are voltage transformation and isolation. Isolation among different FSBCs is provided by transformers. In the other hands existence of transformers is caused that whole FSBCs are fed by single input DC voltage source. Owing to the cascaded transformers, it has a galvanic isolation between an input DC source and output loads. In some systems, where they need to supply with high voltage output from low voltage input, they require additional step-up transformers. The single phase transformers in SMCT structure can be used as step-up or step-down transformers. To obtain high quality output voltage with minimized number of switching devices asymmetric multilevel inverters can be used [22-24]. The SMCT multilevel inverter schemes efficiently increase the number of output voltage levels based on the different turn-ratio of the cascaded transformers. Several strategies can be used for determination of transformers turn-ratio in SMCT. The different output voltage levels can be determined by combinations of switching states of each SMCT. In fact, a proper choice of voltage asymmetry among output transformers can produce a different combination of voltage levels.

An output phase voltage is obtained by summing the output voltages of transformers:

$$V_O = V_{O1} + V_{O2} + \ldots + V_{On} \tag{1}$$

Where n is the number of cascaded transformers or FSBCs. If proper values for the turn-ratio of the cascaded transformers are selected, then the output voltage of the converter can be adjusted in desired value. If all turn-ratio of transformers in Figure 3 are equal to p then the converter is known as symmetric multilevel inverter. The effective number of output voltage levels (m) in symmetric multilevel converter may be related to the number of FSBCs (n) by:

$$m = 4n + 1 \tag{2}$$

and the maximum output voltage of this n cascaded FSBCs is:

$$V_{O\max} = n.p.V_{dc} \quad (3)$$

To provide a large number of output levels without increasing the number of components, asymmetric SMTC can be used. In order to have unequal values for transformers output and produce uniform steps, different methods for the determination of turn-ratio of transformers can be presented. In this paper, the turn-ratio of transformers are proposed to be chosen according to a geometric progression with a factor of 2, 3 and 5. The geometric progression with a factor of 5 is called Fifnary method in this paper. For n cascaded of transformers or FSBCs, one can achieve the following distinct voltage levels:

$$m = 2^{n+2} - 3 \qquad \frac{N_{i2}}{N_{i1}} = 2^{i-1} p \qquad i = 1,2,..,n \quad (4)$$

$$m = 2(3^n - \frac{1}{2}) \qquad \frac{N_{i2}}{N_{i1}} = 3^{i-1} p \qquad i = 1,2,..,n \quad (5)$$

$$m = 5^n \qquad \frac{N_{i2}}{N_{i1}} = 5^{i-1} p \qquad i = 1,2,..,n \quad (6)$$

Where p is the turn-ratio of first transformer or $\frac{N_{12}}{N_{11}} = p$:

The maximum output voltage is obtained, as follows:

$$V_{O\max} = V_{dc} \sum_{i=1}^{n} \frac{N_{i2}}{N_{i1}} = V_{dc} . p \sum_{i=1}^{n} f^{i-1} \quad (7)$$

where f is the geometric progression factor.

The SMCT has one DC voltage source and DC/DC buck, boost or buck boost converter can be used to changes the inverter's DC link voltage. Using DC/DC converter, the DC voltage across each capacitor can be adjusted to a desired voltage value, thereby the main problem associated with balancing the capacitors' voltages in flying capacitors or same converters is solved. Proposed topology has two capacitors in their structure and keeping of their voltage at desired value is simple. In multilevel inverters by decreasing modulation index total harmonic distortion (THD) increases, in other words, when multilevel inverters generate voltage that its value is less than rated value, harmonic distortion increases. By using DC/DC converter between input DC voltage source and SMCT inverter, almost output voltage can be adjusted between zero and maximum value while the staircase nature of voltage is kept and THD can't be increased.

In SMCT, two DC voltage sources can be used instead of one DC source and two capacitors. In some systems they may be available through renewable energy sources such as photovoltaic panels or fuel cells or with energy storage devices (batteries). When ac voltage is already available, two DC sources can be generated using isolated transformers and rectifiers.

Transformers are the fundamental components in SMCT inverter. For most transformers, core saturation is a very undesirable effect. Different condition can be caused core saturation in transformers [25-28]. These conditions are:

- A transformer's primary winding is overloaded from excessive applied voltage
- Operation at frequencies lower than normal frequency
- Presence of DC current in the primary winding
- Existence of DC voltage in input side of transformers
-

In the next section simulation results show that no problem exists about transformer saturation in SMCT structure. The leakage reactance of the transformers provides high-performance filtering effect of the harmonic components of the inverter output voltage [29, 30].

4. OPERATIONAL PRINCIPLE OF THE SMCT BASED ON SIMULATION

The SMCT of Figure 4 was chosen to show the behavior of the proposed topology by simulation results. As can be seen this converter uses two FSBCs cells in series per output phase, with two output transformers.

There are several modulation strategies for multilevel inverters and operation of them depends on modulation strategies. In this paper, the fundamental frequency switching technique has been used. It is important to note that the calculation of optimal switching angles for different goals such as elimination of the selected harmonics and minimizing total harmonic distortion (THD) are not the objective of this paper.

In the first, a nine-level symmetric converter topology is taken for example to introduce the SMCT topologies. If the suitable values for turn-ratio of transformers are selected and proper switching are used, then output voltage levels between+$2V_{dc}$ and -$2V_{dc}$ can be obtained. The operation of the proposed multilevel inverter in symmetric state is described by Figure 5. Here all turn-ratio of transformers are the same and the magnitude of DC voltage source is considered 200 V. The capacitance of DC-link is 3300 μF. The load capacity is 5 kVA (power factor is 0.8 lag). This structure generates nine levels in each output phase voltage. The output frequency is 60 Hz.

ON switches lookup table of nine-level multilevel inverter has been shown in Table 1. Table 1 shows the relationships between the output voltage and the different modes of switching states. Note that there are different switching patterns for producing the different level. Every mode corresponds to one kind of output voltage level. Figure 5(a) shows input DC voltage. Figures 5(b) and 5(c) depict the internal flying capacitors voltages for the case no feedback control is applied. Output voltage waveform is shown in Figure 5(d) that is a typical staircase nine-level waveform. Figure 6 shows output current.

The input voltages and currents of transformers are shown in Figure 7. This figure shows that the input voltage of each transformer has negative, positive or zero values and input current of transformers are sinusoidal. The DC value of input voltages and currents of transformers is very low (near to zero). In the SMCT, primary windings voltages is restricted and overloaded from excessive applied voltages don't occur. The frequencies of input voltages of transformer are the same as output frequency.

Several strategies can be used for determination of transformers turn-ratio in SMCT in asymmetric state. In the second simulation, among determination transformers turn-ratio strategies, Fifnary method is selected. Table 2 resumes the most important parameters of the proposed converter in simulation results.

If the turn-ratio of transformers is chosen as 20:20, and 20:100, this circuit can generate twenty five level voltages. Table 3 shows the ON switches lookup table of twenty five-level multilevel inverter. The output voltage waveform and harmonic spectrum of load voltage are shown in Figure 8(a) and 8(b), respectively.

The SMCT has twenty five-level voltages per phase with the fewest components. Total harmonic distortion (THD) of output voltage is as low as 5%. It can be observed from the harmonic spectrum of voltages that, presented topology is effective to meet low harmonic level. Figure 9 shows output current.

The input voltages of transformers and fourier analysis are shown in Figures 10(a) and 10(b). These figures show the DC value of input voltages of transformers is very low (near to zero) and the magnitude of frequencies that put on near the fundamental frequency (50 Hz) is very small (near to zero) and they can't create difficult in terms of core saturation. In the CTRSI, primary windings voltages is restricted and overloaded from excessive applied voltages don't occur. So no problem exists about transformer saturation in SMCT structure in this state, too.

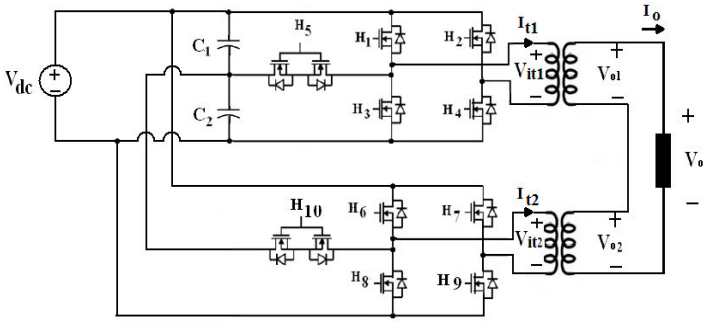


Figure 4. Novel multilevel inverter with two FSBCs.

Table 1. Relationships between the output voltage and the different modes of switching states.

On Switches	V_O(V)	On Switches	V_O(V)
H_4, H_5, H_6, H_7 (H_1, H_2, H_9, H_{10})	100	H_5, H_2, H_8, H_9 (H_3, H_4, H_7, H_{10})	-100
H_1, H_4, H_6, H_7 (H_4, H_5, H_9, H_{10})	200	H_2, H_3, H_8, H_9 (H_5, H_2, H_7, H_{10})	-200
H_1, H_4, H_9, H_{10} (H_4, H_5, H_6, H_9)	300	H_2, H_3, H_{10}, H_6(H_5, H_2, H_7, H_8)	-300
H_1, H_4, H_6, H_9	400	H_2, H_3, H_6, H_7	-400
H_1, H_2, H_6, H_7	0	H_3, H_4, H_7, H_8	0

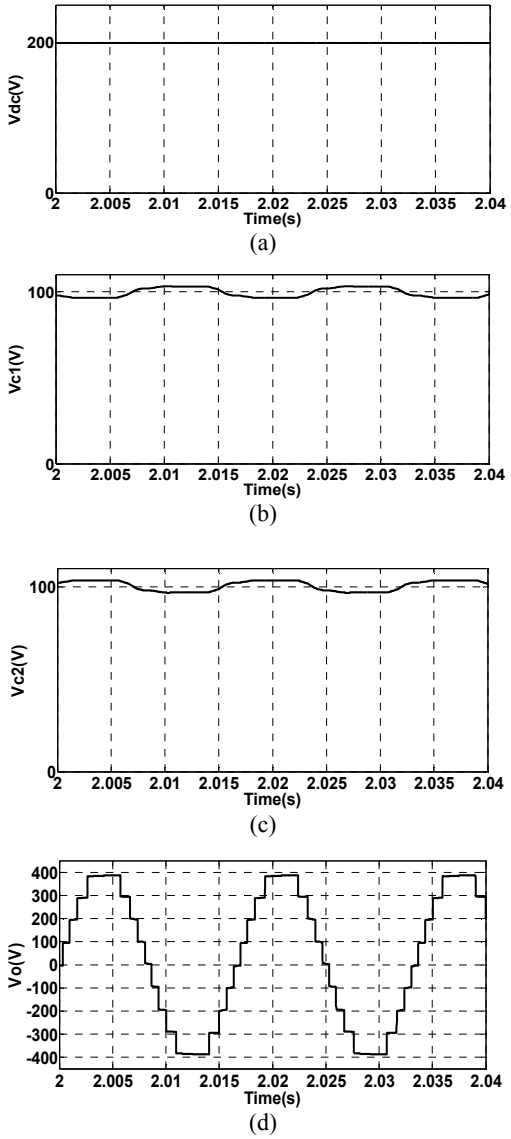


Figure 5. Nine-level multilevel inverter (a) input voltage (b) capacitor voltage, V_{c1}(c) capacitor voltage, $V_{c2}$and (d) output phase voltage.

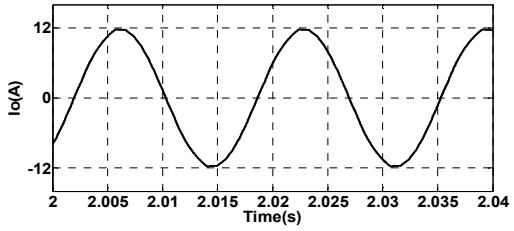


Figure 6. Output phase current.

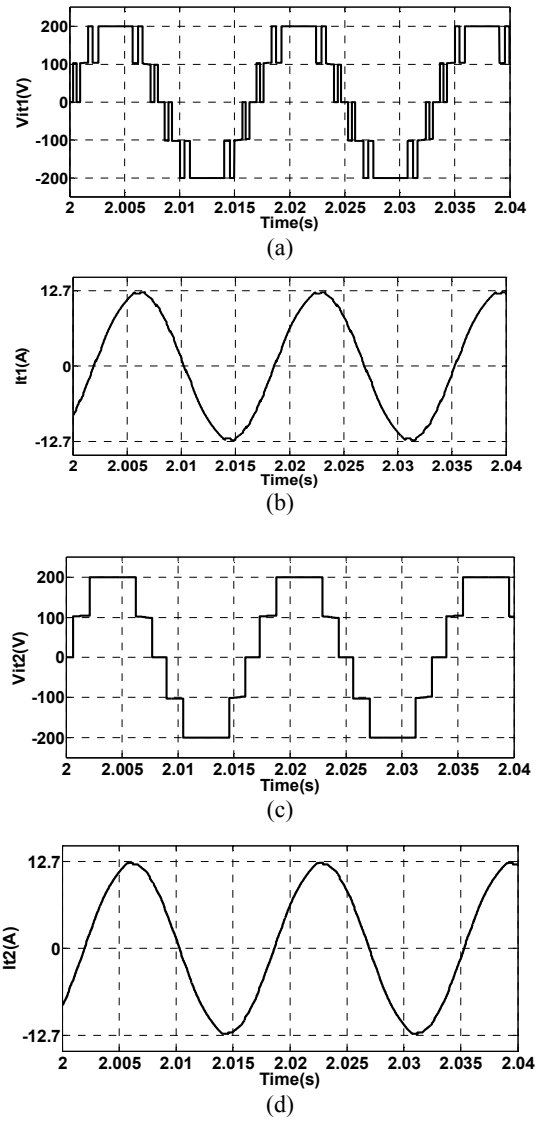


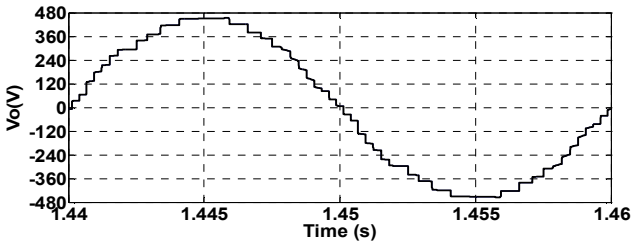
Figure 7. Nine-level multilevel inverter (a) input voltage of transformer, V_{it1} (b) input current of transformer, I_{t1} (c) input voltage of transformer, V_{it2} and (d) input current of transformer, I_{t2}.

Table 2. Simulation study parameters.

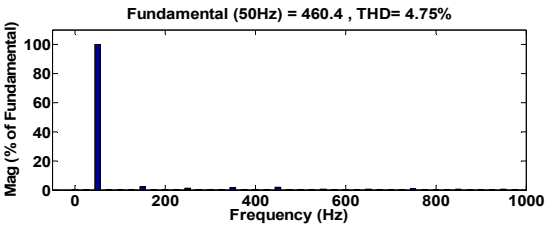
	Nominal frequency	R-L Load	capacitor	DC source
values	50HZ	5 kVA (power factor is 0.8 lag)	4700µF	80V

Table 3. Look-up table of a single-phase twenty five-level inverter.

On Switches	V_O(V)	On Switches	V_O(V)
H_5, H_4, H_6, H_7	40	H_5, H_2, H_8, H_9	-40
H_1, H_4, H_6, H_7	80	H_2, H_3, H_8, H_9	-80
H_2, H_3, H_{10}, H_9	120	H_1, H_4, H_{10}, H_7	-120
H_5, H_2, H_{10}, H_9	160	H_5, H_4, H_{10}, H_7	-160
H_1, H_2, H_{10}, H_9	200	H_3, H_4, H_{10}, H_7	-200
H_5, H_4, H_{10}, H_9	240	H_5, H_2, H_{10}, H_7	-240
H_1, H_4, H_{10}, H_9	280	H_2, H_3, H_{10}, H_7	-280
H_2, H_3, H_6, H_9	320	H_1, H_4, H_7, H_8	-320
H_5, H_2, H_6, H_9	360	H_5, H_4, H_7, H_8	-360
H_1, H_2, H_6, H_9	400	H_3, H_4, H_7, H_8	-400
H_5, H_4, H_6, H_9	440	H_5, H_2 ,H_7, H_8	-440
H_1, H_4, H_6, H_9	480	H_2, H_3, H_7, H_8	-480
H_1, H_2, H_6, H_7	0	H_3, H_4, H_8, H_9	0



(a)



(b)

Figure 8. Twenty five-level multilevel inverter (a) output phase voltage and (b) harmonic spectrum of load voltage.

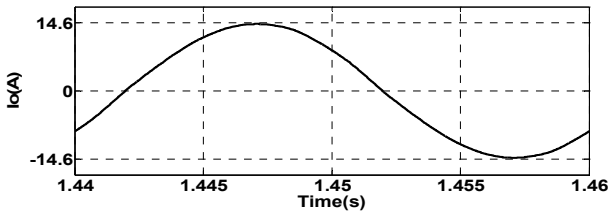
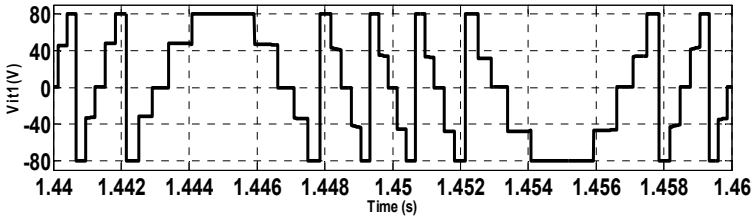
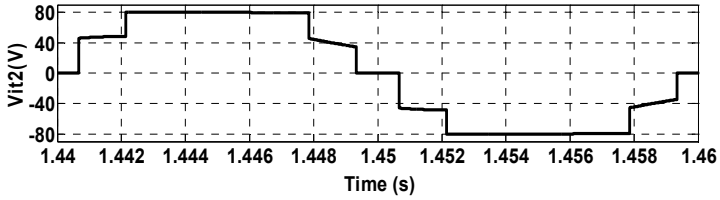


Figure 9. Output phase current.



0 Hz	(DC):	0.00%	90.0°
25 Hz		0.00%	181.9°
50 Hz	(Fnd):	100.00%	2.4°
75 Hz		0.00%	2.0°
100 Hz	(h2):	0.01%	180.5°
125 Hz		0.00%	0.6°

(a)



0 Hz	(DC):	0.00%	270.0°
25 Hz		0.00%	181.0°
50 Hz	(Fnd):	100.00%	1.3°
75 Hz		0.00%	1.5°
100 Hz	(h2):	0.00%	184.0°
125 Hz		0.00%	4.0°

(b)

Figure 10. Twenty five multilevel inverter (a) input voltage of transformer and fourier analysis, V_{it1} and (b) input voltage of transformer and fourier analysis, V_{it2}.

5. COMPARISON STUDY

The main disadvantage associated with the multilevel inverters is requiring a great number of components. Among the conventional multilevel inverters, diode-clamped, flying capacitor and cascaded H-bridge, the cascaded H-bridge multilevel inverter requires the least number of components to achieve the same number of output voltage levels and this topology can operate in symmetric and asymmetric states. To probe the reduction in component numbers achieved by new configuration; comparison between cascaded topology and new multilevel can be done but in this paper the main objective focused on topologies that use balancing capacitor in their structures.

In this section, the proposed topology is compared with flying capacitor and stacked multicell converters. The first comparison index is the number of switches. Each switch in the inverter requires an isolated driver circuit. The isolated driver circuits need separate isolated power supply for each semiconductor switch. Hence the reliability of a multilevel inverter is proportional to the number of its components. Tables 4 and 5 compare the power component requirements among the conventional flying capacitor, stacked multicell

and suggested multilevel inverters for the same number of the output voltage levels.

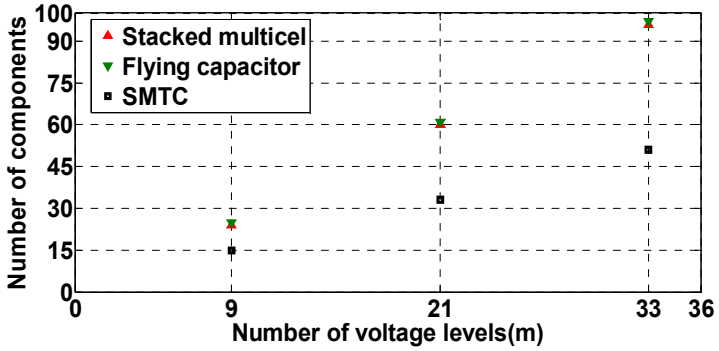
Table 4 compares the main power component requirements per phase leg among these three multilevel inverters in symmetric state, where m is the number of voltage levels. The SMCT nine-level inverter, for example, requires 10 main switches, while the other multilevel inverters need 16 switches. Table 5 compares the main power component requirements per phase leg among asymmetric multilevel inverters based on SMCT. The SMCT with 10 switches and two transformers, for example, produces 13-level in Binary state, 17-level in Trinary state and 25-level in Fifnary state. Figure 11 shows the total required components (single phase) in the multilevel inverters as a function of the number of voltage levels. As shown in Figure 11(a), flying capacitor, stacked multicell and symmetric SMCT are compared. Figure 11(b) shows compression required components between asymmetric SMCTs. These figures show capabilities of SMCT topology to production the same number of voltage levels with less number of components, clearly.

Table 4. Comparison of power component requirement.

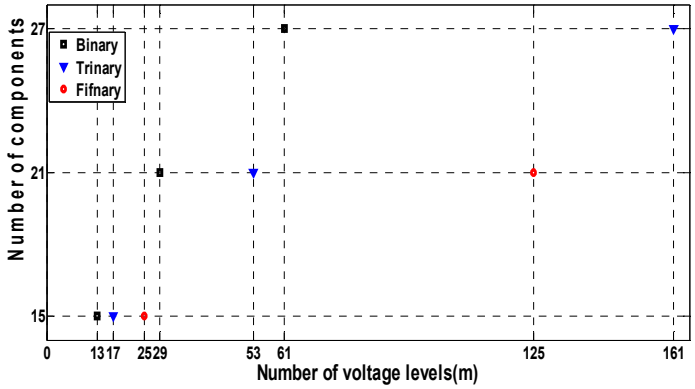
Inverter	Flying capacitor	Stacked multicell	Proposed
Main Switches	$2(m-1)$	$2(m-1)$	$\frac{5(m-1)}{4}$
DC Source	1	2	1
Capacitor	$(m-1)$	$(m-3)$	2
Transformer	-	-	$\frac{(m-1)}{4}$
Total component	$3m-2$	$3m-3$	$\frac{6(m+1)}{4}$

Table 5. Comparison of component requirement among asymmetric proposed topologies.

	Binary	Trinary	Fifnary
Main Switches	$5(\frac{Ln(m+3)}{Ln2}-2)$	$\frac{5Ln(\frac{m+1}{2})}{Ln3}$	$\frac{5Ln(m)}{Ln5}$
DC Source	1	1	1
Capacitor	2	2	2
Transformer	$(\frac{Ln(m+3)}{Ln2}-2)$	$\frac{Ln(\frac{m+1}{2})}{Ln3}$	$\frac{Ln(m)}{Ln5}$
Total component	$(6\frac{Ln(m+3)}{Ln2}-9)$	$\frac{6Ln(\frac{m+1}{2})}{Ln3}+3$	$\frac{6Ln(m)}{Ln5}+3$



(a)



(b)

Figure 11. Compression of components number (a) among flying capacitot, stacked multicell and symmetric SMCT (b) among asymmetric SMCTs.

6. CONCLUSIONS

This paper has proposed a new configuration that uses flying capacitor and called SMCT. In comparison with flying capacitor and stacked multicell converters, the main advantage of the proposed converter is increasing the number of output voltage levels with less number of components. Only two capacitors are used in SMCT converter while in flying capacitor and stacked multicell converters by increasing number of levels number of capacitors increases. SMCT converter can operate in symmetric an asymmetric states and different algorithms for calculating of transformers turn-ratio exist. In this paper four algorithms for calculating of transformers turn-ratio have been presented, too. These algorithms give freedom action to designer for design multilevel inverter. Comparison between the conventional flying capacitor and stacked multicell topologies and the proposed multilevel inverter is shown in this paper. The simulation results exhibit the good performance and feasibility of the proposed topology.

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