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FPGA Based, Low Cost Modulators of BPSK and BFSK, Design and Comparison of Bit Error Rate over AWGN Channel

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ABSTRACT

This paper presents the simulation results of binary frequency shift keying (BFSK) and binary phase shift keying (BPSK) modulation techniques in FPGA complier. Both modulation techniques are proposed in low power consumption systems. In addition, these modulation techniques are used high speed systems. Also, in this paper BPSK and BFSK modulations are compared to bit error rate (BER). BPSK modulation technique has BER low than BFSK modulation in AWGN channel. Thereby, as satellite communication for systems which need very high speed data transfer, BPSK modulation technique is preferred. For BPSK and BFSK modulation techniques, modulators were designed using FPGA complier (Quartus II 9.1). In Quartus II complier, results of simulation are observed using vector waveform file.

Key words: FBGA, BPSK, BFSK, Modulator, AWGN, BER.

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1. INTRODUCTION

FPGAs are integrated circuits that provide reconfiguration advantages for production of digital systems. [1] A common FPGA consists of a bidimensional array of Configurable Logic Blocks (CLBs) to support the logic and storage elements of circuits with input and output blocks [1]. BPSK (Binary Phase Shift Keying and BFSK (Binary Frequency Shift Keying) modulation techniques, which modulation types, are realized binary transfer. These modulation techniques are very efficient for power consumption in their areas of application. Thereby, BPSK and BFSK are proposed for these areas [2,3]. As satellite communication and medical systems, in important areas, many applications were realized using BPSK and BFSK modulation techniques [2-4].

For short-range wireless communications, power consumption of BPSK modulator was reduced using CMOS technology [2]. In that paper, two highly integrated ultra-low-power binary phase-shift keying (BPSK) receivers for short-range wireless communications was presented [2].

In applicable working of satellite communication systems, BPSK modulation technique was realized using FPGA. In that paper, A CMOS low-power transceiver for implantable and external health monitoring devices operating in the MICS band was presented [3]. Comparison of theoretical and simulation BER (Bit Error Rate) results were analyzed [3]. In other paper was presented the Binary Frequency Shift Keying (BFSK) modulator using the Frequency Hopping Spread Spectrum (FHSS) operating for the European band ISM 863-870 MHz. This modulator is intended for short range wireless applications, such as the wireless network sensors [5].

In a work about Y-00 direct encryption protocol, BPSK technique was used. In this paper for the security of the Y-00 direct encryption protocol under correlation attack, BPSK modulator and BPSK demodulator were used [6].

For wireless communication laboratory, design of PSK modulator was realized. In this paper, total cost is about USD $200. For different modulations and demodulations, number of used FPGA is 6. Total cost is about $1200 for laboratory and type of used FPGA is Xilinx Spartan-3A [7]. In other work, total cost is approximately $550 and realized modulation types are PSK, QAM, MSK e.g. Used FPGA device is Altera DE2-70 board in the paper [8].

In our work, we select Altera DE1 board (low cost FPGA kit) in Quartus II complier. This FPGA board supports same modulation techniques as Xilinx Spartan-3A and Altera DE2-70 board. Total cost of Altera DE1 board is approximately $200. In addition, we presented the BER comparison of BFSK and BPSK modulation techniques on AWGN (Additive White Gaussian Noise). Moreover, data rate of BPSK and BFSK were analyzed to using Quartus 9.2 FPGA complier.

BPSK MODULATOR

In Phase Shift Keying (PSK) modulation which least affected by noise among binary modulation, phase of the carrier signal varies with respect to the baseband signal. According to case of transmitted data bit (0 or 1 cases), two different phase of carrier signal is used [9].

$$m(t) = \begin{pmatrix} \sin(2\pi f_c t) & if\ symbol\ \ 1 \\ \sin(2\pi f_c t + \pi) & if\ symbol\ \ 0 \end{pmatrix} \quad (1)$$

It is shown that block diagram of BPSK modulator.

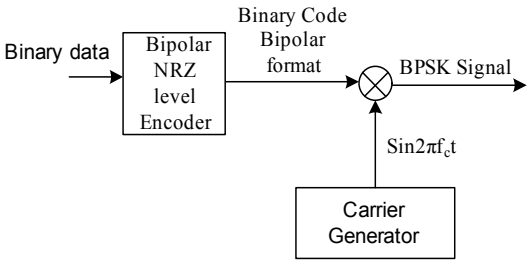

Figure 1. BPSK Modulator.

In Figure 2, it is shown that BPSK, message and carrier signal.

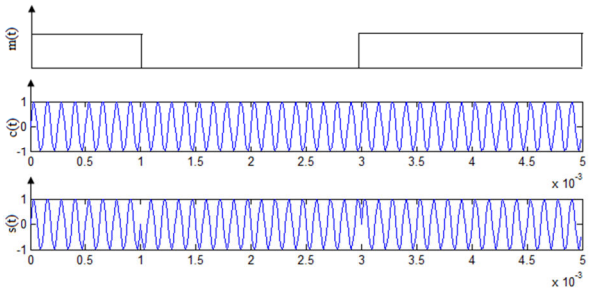

Figure 2. BPSK modulated signal.

In Figure 2, m(t), c(t) ve s(t) denote message signal, carrier signal and BPSK signal respectively.

BFSK MODULATOR

BFSK modulation can be achieved for two different frequency of carrier signal. In figure 3, it is shown that block scheme of BFSK modulator. Also, BFSK modulation is explained using equation (2).

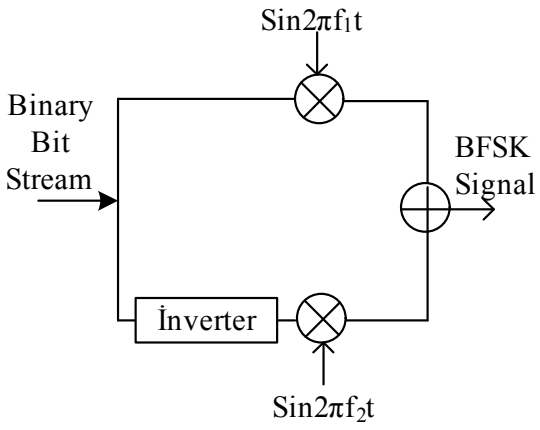

Figure 3. BFSK modulator.

$$m(t) = \begin{pmatrix} \sin(2\pi f_1 t) & if\ symbol 1 \\ \sin(2\pi f_2 t) & if\ symbol 0 \end{pmatrix} \quad (2)$$

In Figure 4 is illustrated that BFSK modulated signal, carrier signals and transmitting signal.

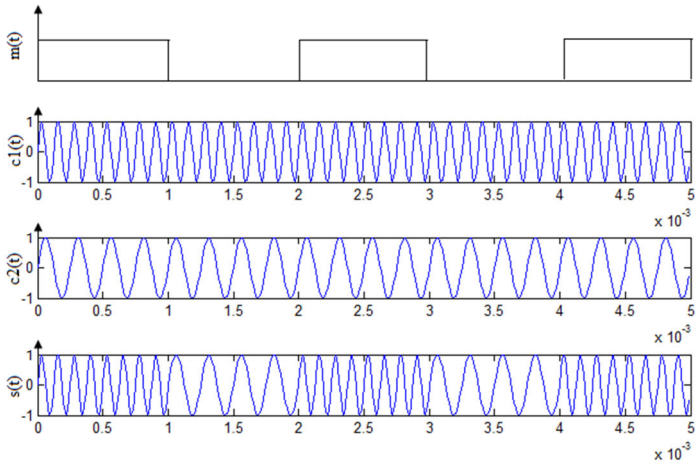

Figure 4. BFSK modulated signal.

Design of BPSK and BFSK based on FPGA

Real time logical circuits have high clock frequency, so FPGA operates very fast and received data are processed in real time. This advantage is very important for wireless communication systems because data transfer rate is virtual value in mobility. In Figure 5, İt is shown that block scheme of design for FPGA-based both BPSK and BFSK modulation.

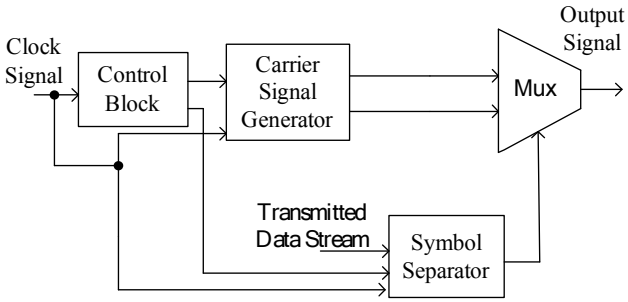

Figure 5. Scheme of FPGA based on BPSK and BFSK modulator.

If Figure 5 is considered as BPSK modulator, digital samples of carrier signal with 0° and 180° phase is saved on ROM1 and ROM2. According to output symbol case (1 or 0) of symbol separator, which was created using Very High Speed Integrated Circuits Hardware Description Language, BPSK signal (output signal) is created with digital samples in ROM1 or ROM2. Moreover, digital samples in ROM1 or ROM2 are selected using selective pin of Mux.

If block diagram in Figure 5 is considered as BFSK modulator, digital samples of two carrier signals with f_1 and f_2 frequencies are saved on ROM1 and ROM2. According to output of symbol separator, transmitted digital samples in ROM are converted to BFSK modulated signal using mux. In figure 6, it is illustrated that BFSK modulator block. BFSK modulator block consists of counter block, ROM block, Mux block, Bit separator and control block. These blocks were embedded on BFSK modulator block.

Figure 6 illustrates BFSK modulator, which consists of *bit_separator*, *control_block*, two *ROMs* and *MUX*.

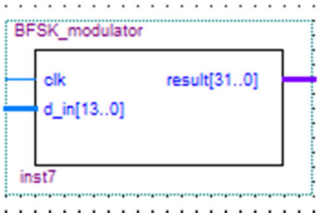

Figure 6. BFSK modulator in Quartus II .

Used control block was designed using Very High Speed Integrated Circuits Hardware Description Language. In addition to, this block products enabling signal for operating other blocks. In Figure 7, the control block is shown.

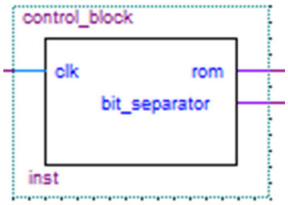

Figure 7. Control Block for BPSK and BFSK.

In Figure 8, it is illustrated that symbol separator using VHDL for BPSK and BFSK.

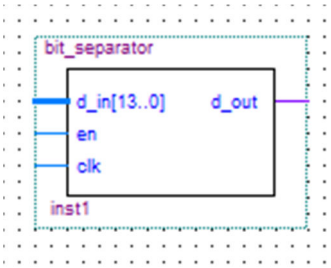

Figure 8. Symbol Separator for BPSK and BFSK.

As shown in figure 6, figure 9 is shown that embedded into one of the blocks too. This feature is created using VHDL and appropriate .inc and .cmp files.

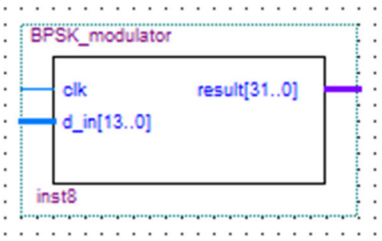

Figure 9. BPSK modulator in Quartus II.

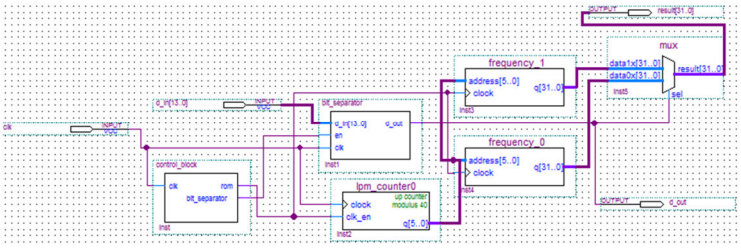

Figure 10. BPSK and BFSK modulator.

In Figure 10, according to saved samples in ROM, the modulator is determined as function that operates phase shifting or frequency shifting.

BER for BPSK and BFSK

In order to performance comparison of BPSK and BFSK, BER of these modulations must be explained. So, error of probability these modulations is evaluate the performance of the detector when the additive noise is white and Gaussian and BER of BPSK modulation is presented in equation (7) [10]. In these equations, $s_1(t)$, ε_b, N_0 are the transmitted signal, energy per bit and noise power respectively. There exists a phase difference of 180^0 in BPSK modulation technique. Namely, $s_1(t)$ and $s_2(t)$ are assumed carrier signals for BPSK. If a equation is wanted to generated between

these carrier, $s_1(t) = -s_2(t)$. Therefore $s_1(t)$ and $s_2(t)$ are antipodal signals and hence, probability error can be expressed as shown in equation (7) [10].

$$P(e|s_1) = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^{-\sqrt{2\varepsilon_b/N_0}} e^{-x^2/2} dx \quad (4)$$

$$= \frac{1}{\sqrt{2\pi}} \int_{\sqrt{2\varepsilon_b/N_0}}^{\infty} e^{-x^2/2} dx \quad (5)$$

$$= Q\left(\sqrt{\frac{2E_b}{N_0}}\right) \quad (6)$$

On the other hand, for BFSK, error probability is presented in equation (8).

$$P_b = Q\left(\sqrt{\frac{E_b}{N_0}}\right) \quad (7)$$

If these equations are analyzed, we note that the probability of error depends only on the ratio ε_b/N_0 [10]. In order to calculate bit error rate, function of Q (z) is achieved as presented in these equations. The matlab provides error functions (erfc(x)). This calculation is quite complex, so BER of BPSK and BFSK weren't calculated using simulator of FPGA. In addition to, result of simulation is plotted in figure 11 for bit error rate of BPSK and BFSK on matlab.

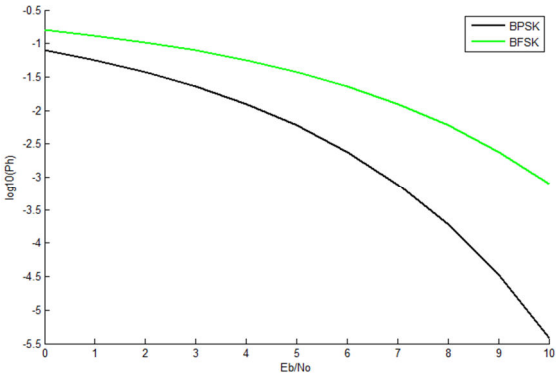

Figure 11. BER for BPSK and BFSK.

CONCLUSION

It was shown that BPSK and BFSK modulation techniques are relatively simple implemented on FPGA. Also, for designed modulators, the importance of VHDL codes was introduced. In addition, both block diagram in FPGA compiler (Quartus II) and designed blocks using VHDL are used in conjunction. So if only VHDL codes or only block diagram in FPGA complier (available blocks) are used, the designed modulators are created fairly difficult. Comparison of BER over AWGN for BPSK and BFSK was introduced. Besides, it is shown that BPSK modulation technique has BER low than BFSK modulation technique. In Figure 12 and Figure 13, it is shown that simulation results for BFSK modulations technique.

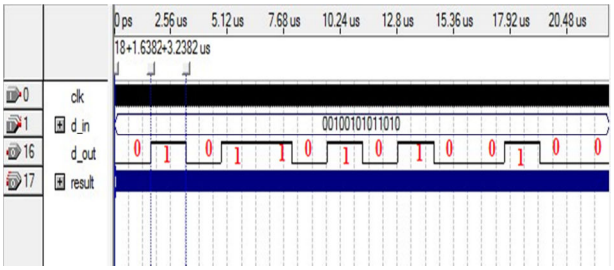

Figure 12. Data out for BFSK.

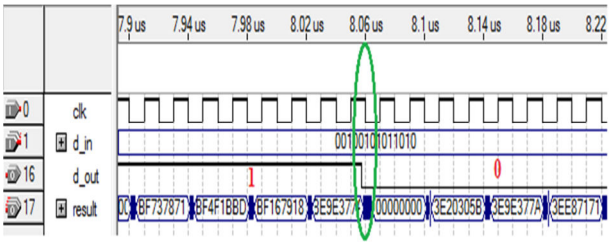

Figure 13. Symbol changing for BFSK .

In Figure 12 and 13, result, d_out, d_in and clk present BFSK modulated signal, both output of bit_separator and selective pin of mux, transmitted data and clock signal respectively. In figure 12, d_in is 00100101011010. d_out (output of bit separator) has also same bits. One bit transmits 3.2382us-1.6382us=1.6us. This result was obtained to using clock signal with 50 MHz frequency. Also, used sample number in ROM is 40. Namely, one bit represents 40 samples. If used sample number isn't take into account, this modulator has been operating quite efficiency. Because if figure 13 is scrutinized, it will be shown that one sample is transmitted during only 2 clock signals with 50 MHz frequency. If used samples are determined using maximum Nyquist frequency (for carrier signal), speed of modulator will increase. In this design, used first carrier signal frequency is 20 times second carrier signal for BFSK modulation. In addition to, any modulation multiplexing technique was used in this design.

In figure 14 and figure 15, as defined in results of BFSK, pin names are same tag. Figure 15 illustrates to changing of phase (0 to 1).

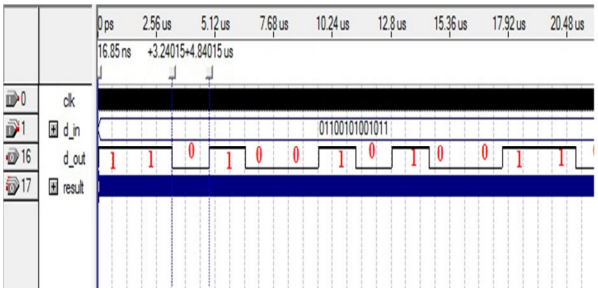

Figure 14. data out for BPSK.

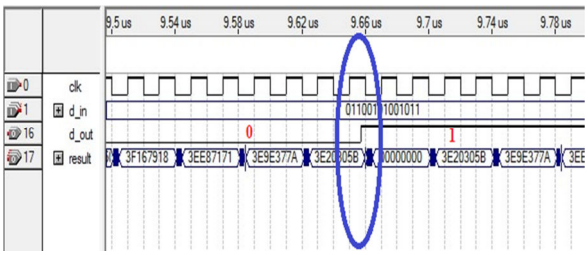

Figure 15. Symbol changing for BPSK .

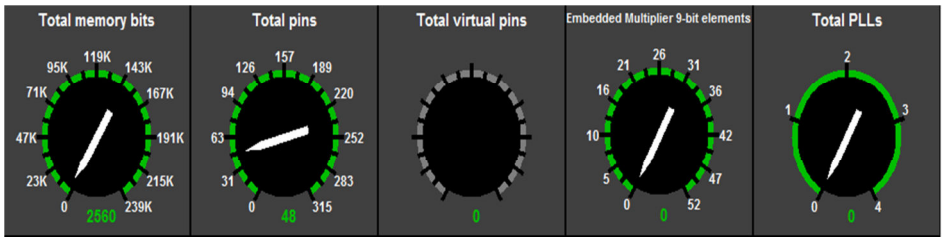

Figure 16. Resource utilization.

For BPSK and BFSK, it is shown that resource utilization in Figure 16. So FPGA based BPSK and BFSK modulators use same source on FPGA, BPSK modulator is only shown in Figure 16. Both BPSK modulation technique and BFSK modulation technique resource utilization, power on FPGA and these modulation techniques are same during data transfer time. For BPSK and BFSK modulator blocks, only difference is digital samples value in ROM. Because of frequency different between these modulators, sampled data is different in ROMs.

Total memory bits are 80 samples (for two ROM)*32 (Hexadecimal)= 2560. Total pins are d_out(1)+d_in(14)+clk(1)+result(32)=48.

In addition, BPSK has low BER than BFSK over AWGN channel. BPSK and BFSK bit rate are same in simulation results.

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