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Analysis of Barrier Height and Carrier Concentration of MOS Capacitor Using C-f and G/ω-f Measurements

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ABSTRACT

Capacitance (C) and conductance (G/ω) measurements of MOS capacitor with Si_3N_4 dielectric deposited on Si have been investigated in the frequency range of 1 kHz to 1 MHz at room temperature. The experimental results indicate that the values of the measured C and G/ω decrease with the increasing frequency. The $1/C^2$-V curves are linear in the wide voltage region for each frequency. This linearity of the curves is attributed to the uniformity of the donor concentration in the depletion region. Also, the barrier height (Φ_B) and carrier (donor) concentration (N_D) were obtained from C^{-2}-V characteristics. The values of the Φ_B and N_D decrease with the increasing frequency.

Keywords: MOS capacitor; C-f and G/ω-f characteristics; Barrier height; Donor concentration

1. INTRODUCTION

The metal-oxide-semiconductor (MOS) capacitors can be produced by coating an oxide layer upon the metal/semiconductor interface. With regard to the dielectric property of the oxide layer coated between the metal and the semiconductor, MOS capacitors are analogous to parallel-plate capacitors [1-8]. In studies conducted so far, the oxide layers of various types, such as SiO_2, Si_3N_4, SnO2, TiO_2, have been used between the metal and the semiconductor [6-8]. In real MOS capacitors, the localized interface states exist at the semiconductor-insulator interface and the device behavior is different from an ideal case due to the presence of these localized interface states. The localized electronic states associated with the surface region were called "surface states". The reason for their existence is the interruption of the periodic lattice structure at the surface, surface preparation, formation of insulating layer and impurity concentration of semiconductor [1,2,9,10]. The interface states usually cause a bias shift and frequency dispersion in the capacitance-voltage (C-V) and conductance-voltage (G/ω-V) curves [9-11]. The performance of MOS capacitors is greatly influenced by the interface state density (N_{ss}). Consequently, the N_{ss} is an important parameter for evaluating the quality of a MOS structures. [3,12]. In addition, series resistance (R_s) is an important parameter, which causes changes in the electrical characteristics of MOS capacitors [1,2,9,13].

The purpose of this paper is to determine the electrical parameters such as the diffusion potential (V_D), donor concentration (N_D), Fermi energy level (E_F) and barrier height (Φ_B) by using the capacitance-voltage (C-V) and conductance-voltage (G/ω-V) measurements.

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2. EXPERIMENTAL DETAIL

Au/Si_3N_4/n-Si (MOS) capacitor was fabricated on phosphorus doped (n-type) single crystal Si substrates each with a 2" diameter, 300µm thickness, (100) orientation, and 0.5 Ω.cm resistivity. For the fabrication process, the n-Si substrate was chemically cleaned using conventional method and then chemically etched and finally quenched in deionized water. Prior to each cleaning step, the Si substrate was rinsed thoroughly in deionized water of resistivity of 18 MΩ.cm using an ultrasonic bath. After cleaning and etching steps, the Si substrate was mounted on a stainless steel sputtering holder that was heated optically and loaded into a radio frequency (RF) magnetron sputtering system. The Si substrate was heated up to 400 ˚C in $1x10^{-8}$ mbar high vacuum and sputter cleaned in pure argon ambient to ensure the removal of any residual organic substance. Then, the silicon nitride (Si_3N_4) film was deposited on n-Si using high purity (99.999%) silicon nitride target. Also, the film was deposited at a constant pressure of $3x10^{-3}$ mbar and a constant substrate temperature of 200 ˚C.

The ohmic and rectifier contacts were formed using a thermal evaporation system. The ohmic back contacts were formed by the deposition of high-purity Au (99.999%) with a thickness of ~2000 Å at 450 ºC, under 10^{-7} mbar vacuum and the sample was annealed at 400 ºC to achieve good ohmic contact behaviour. After that, circular dot shaped rectifier front contacts with 1 mm diameter and ~2000 Å thickness were formed by the deposition of high - purity Au onto Si_3N_4 thin film at 50 ºC. Finally, Au/Si_3N_4/n-Si capacitor was fabricated for the electrical measurement.

The capacitance-voltage (C-V) and conductance-voltage (G/ω-V) measurements were carried out by using a HP 4192A LF impedance analyzer (5 Hz to 13 MHz). A low-distortion oscillator generated the ac signal with the amplitude attenuated to 50 mV_{rms} to meet the small signal requirement for the capacitor. All measurements were carried out with the help of a microcomputer through an IEEE-488 ac/dc converter card.

3. RESULTS AND DISCUSSION

The capacitance and conductance measurements were performed over a frequency range of 1 kHz-1 MHz at room temperature. Fig. 1(a) and (b) show the C-f and G/ω-f characteristics of the MOS capacitor. As shown in Figs. 1(a) and (b), the C and G/ω has displayed a decreasing trend with increasing frequency in the frequency range of 1 kHz-1 MHz.

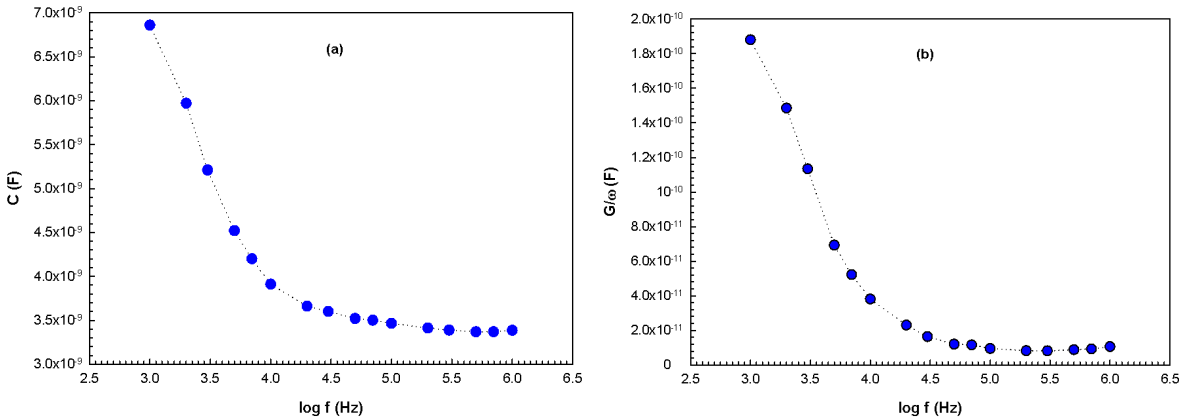

Fig. 1. Plot of (a) capacitance (C) and (b) conductance (G/ω) with log frequency of MOS capacitor.

As the frequency is increased, the capacitance decreases to the same limit, as the charges on the defects no longer have time to rearrange in response to the applied voltage [14-18]. The series resistance (R_s) seems to be the most important parameter that causes the electrical characteristics of MOS capacitors to be non-ideal [1]. There are several methods to extract the series resistance of MOS capacitors in literature [19-22]. In this study we have used the conductance method developed by Nicollian and Goetzberger [19,20]. The measured impedance (Z_{ma}) of MOS capacitor using the parallel RC circuit [1,2,23] is equivalent to the total circuit impedance as

$$Z_{ma} = \frac{1}{G_{ma} + j\omega C_{ma}} \qquad (1)$$

Comparing the real and imaginary part of the impedance, the series resistance is given by

$$R_s = \frac{G_{ma}}{G_{ma}^2 + (\omega C_{ma})^2} \qquad (2)$$

The series resistance of the MOS capacitor is calculated according to Eq. (2) and shown in Fig. 2. From Fig. 2, it is clearly seen that the R_s decreases with increase in frequency.

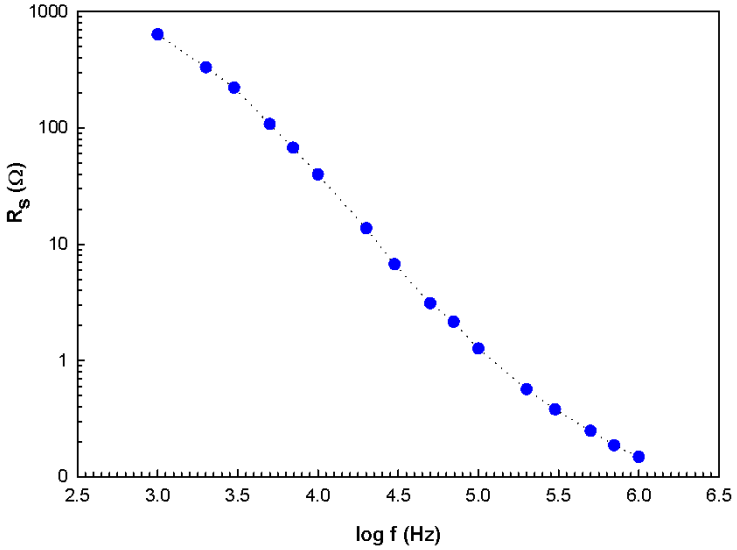

Fig. 2. Plot of the series resistance (R_s) with log frequency of MOS capacitor.

This frequency dependence of R_s is the result of frequency-dependent charges such as interface charge, fixed oxide charge, oxide-trapped charge and mobile oxide charge. Also, the trap charges have enough energy to escape from the traps located between metal and semiconductor interface in the Si band gap.

The analysis of the C-V characteristics has been achieved from the reverse bias C^{-2}-V characteristics of the MOS capacitor. In these structures the depletion layer capacitance is given as follows [1,2,6,24-26].

$$C^{-2} = \frac{2(V_o + V)}{\varepsilon_s \varepsilon_o q A^2 N_D} \quad (3)$$

$$\frac{d(C^{-2})}{dV} = \frac{2}{\varepsilon_s \varepsilon_o q A^2 N_D} \quad (4)$$

where A is the area of the structure (7.85×10^{-3} cm^{-2}), ε_s is the dielectric constant of semiconductor ($11.9\varepsilon_o$ for Si), ε_o is the dielectric constant of vacuum (8.85×10^{-14} F/cm), N_D is equivalent to the free electron concentration when all shallow donor levels are ionized, q is the electronic charge, V is the applied bias and V_o is the intercept of C^{-2}-V plot with the V axis and is given by

$$V_o = V_D - \frac{k_B T}{q} \quad (5)$$

where V_D is the diffusion potential, T is the absolute temperature and k_B is the Boltzmann's constant. The value of the barrier height (Φ_B) can be calculated by the following well-known equation, using the C-V measurements,

$$\Phi_B(C-V) = V_D + E_F - \Delta\Phi_B = V_D + \left(\frac{k_B T}{q}\right) \ln\left(\frac{N_C}{N_D}\right) - \Delta\Phi_B \quad (6)$$

where E_F is the energy difference between the bulk Fermi level and conductance band edge, N_C is the effective density of states in the conduction band, which is $N_c = 2.8 \times 10^{19}$ cm^{-3} for n-Si at room temperature and $\Delta\Phi_B$ is the image force barrier lowering and can be obtained from the well-known relationship in Refs. [2,6,18,24,27-32].

Fig. 3 shows the reverse bias C^{-2}-V characteristics of the MOS capacitor in the frequency range between 30 kHz and 1 MHz at room temperature. In Fig. 3, it is clear that the intercept of the C^{-2}-V characteristics changes with increasing frequency.

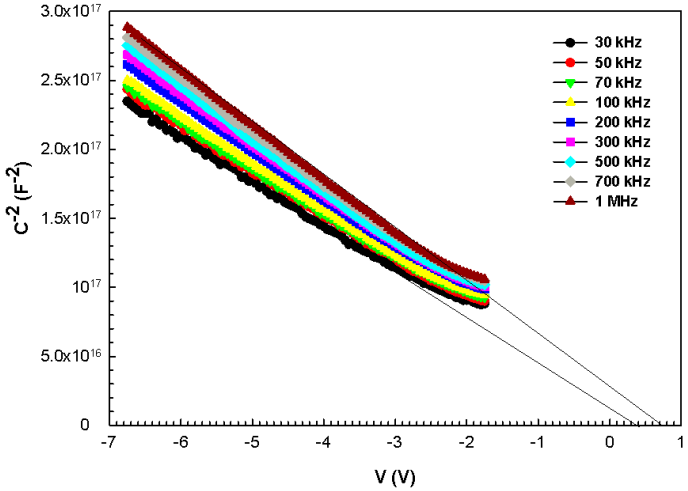

Fig. 3. The reverse bias C^{-2}-V characteristics of the MOS capacitor at different frequencies.

It is seen that the C^{-2}-V plots are linear in the wide voltage region for each frequency. This linearity of the curve is attributed to the uniformity of the donor concentration in the depletion region, indicating the interface states cannot follow ac signal at high frequencies [2]. At the high frequencies, the values of the capacitance are only space charge capacitance. However, at low frequencies the non-linearity of C^{-2}-V plots can be explained on the basis of assumption that some of interface states can easily follow the applied ac signal and yield an excess capacitance, which depends on frequency [1,2,16,24].

From the reverse bias C-V measurements, the barrier height (Φ_B) was calculated at different frequencies using the intercept voltage V_o of the C^{-2}-V plots and was given in Table 1. As shown in Table 1, in the frequency range of 30 kHz-1 MHz, the C-V measurements are revealed that the values of barrier height (Φ_B) change from 0.95 to 0.76 eV and the donor concentration from $3.93x10^{15}$ to $3.04x10^{15}$ cm^{-3}. The decrease in barrier height with increasing frequency is due to a decrease in V_o.

Table 1: Electrical parameters of MOS capacitor obtained from C^{-2}-V plot.

Frequency (kHz)	V_o (V)	V_D (eV)	N_D ($x10^{15}cm^{-3}$)	W_D ($x10^{-5}cm$)
30	0.71	0.74	3.93	4.98
50	0.68	0.71	3.71	5.02
70	0.65	0.68	3.66	4.94
100	0.64	0.67	3.57	4. 95
200	0.61	0.64	3.40	4.96
300	0.59	0.61	3.30	4.94
500	0.57	0.59	3.23	4.92
700	0.54	0.56	3.13	4.87
1000	0.52	0.54	3.04	4.84

Frequency (kHz)	E_F (eV)	$\Delta\Phi_B$ (meV)	Φ_B (eV)
30	0.230	18.95	0.95
50	0.231	18.50	0.92
70	0.231	18.23	0.89
100	0.232	18.03	0.88
200	0.233	17.61	0.85
300	0.234	17.31	0.83
500	0.235	17.10	0.81
700	0.235	16.74	0.78
1000	0.236	16.45	0.76

The depletion layer width (W_D) being deduced from the experimental C-V measurements is given by [1,2]

$$W_D = \sqrt{\frac{2\varepsilon_s}{qN_D}\psi_s} \qquad (7)$$

where ψ_s is the surface potential.

Fig. 4(a) and (b) shows plots of donor concentration (N_D) and the surface potential (ψ_s) versus frequency obtained from the slope of the linear plot of C^{-2}-V curves. As shown in Fig. 4(b), the ψ_s decreases with increasing frequency. As shown in Fig. 4(a), the N_D values decrease with increasing frequency. This behavior of N_D can be explained by whether the interface state charges contribute to the capacitor capacitance or the charge at the interface states can follow an ac signal due to various kinds of states with different lifetimes [33-38]. If the capacitance measurements are made at sufficiently high frequencies, the interface state charges cannot contribute to the MOS capacitance. This will occur when the time constant is too long to permit the charge to move in and out of the interface states in response to an applied signal.

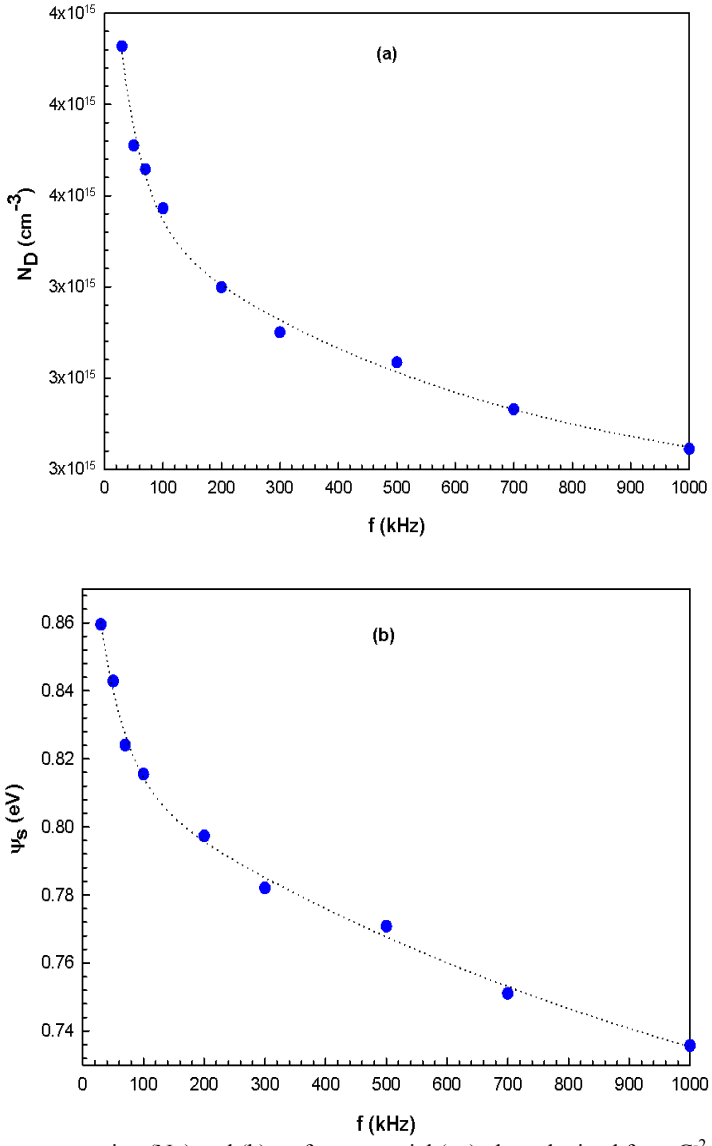

Fig. 4. (a) Donor concentration (N_D) and (b) surface potential (ψ_s) plots obtained from C^{-2}-V curves.

4. CONCLUSION

In this study, the electrical parameters of Au/Si_3N_4/n-Si (MOS) capacitor such as N_D, E_F, Φ_B, V_D and ψ_s have been calculated from frequency dependent C^{-2}-V characteristics. The C^{-2}-V curves are linear for each frequency. Experimental results show that the Φ_B and N_D decrease with the increasing frequency. In conclusion, the C-V and G/ω-V characteristics of MOS capacitor have been controlled by the interfacial oxide layer, interface states and series resistance which are responsible for the non-ideal behavior of electrical characteristics.

CONFLICT OF INTEREST

No conflict of interest is declared by the authors.

REFERENCES

[1] E. H. Nicollian, J. R. Brews, MOS Physics and Technology, ***Wiley***, New York, 1982).

[2] S. M. Sze, Physics of Semiconductor Devices, 2nd Ed. ***Wiley***, New York, 1981).

[3] D. K. Schroder, Semiconductor Material and Device Characterization, 2nd Ed. ***Wiley***, New York, (1998).

[4] M. K. Hudait, S. B. Krupanidhi, ***Solid State Electron.*** 44, 1089 (2000).

[5] A. Singh, K. C. Reinhardt, W. A. Anderson, J. ***Appl. Phys***. 68, 3475 (1990).

[6] A. Tataroğlu, Ş. Altındal, ***Vacuum*** 82, 1203 (2008).

[7] O. Pakma, N. Serin, T. Serin, Ş. Altındal, ***J. Phys. D: Appl. Phys***. 41, 215103 (2008).

[8] S. Kaya, R. Lok, A. Aktag, J. Seidel, E. Yilmaz, ***J. Alloys Compd***. 583, 476 (2014).

[9] H. C. Card, E. H. Rhoderick, ***J. Phys. D Appl. Phys***. 4, 1589 (1971).

[10] C. R. Crowell, S. M. Sze, ***J. Appl. Phys.*** 36, 3212 (1965).

[11] S. Kar, W. E. Dahlke, ***Solid State Electron***. 15, 221 (1972).

[12] S. Jeon, S. Park, ***Microelectron. Eng***. 88, 872 (2011).

[13] U. Kelberlau, R. Kassing, ***Solid State Electron***. 22, 37 (1979).

[14] P. Matheswaran, R. Sathyamoorthy, R. Saravanakumar, S. Velumani, ***Mater. Sci. Eng. B*** 174, 269 (2010).

[15] A. Tataroğlu, ***G.U. J. Sci***. 26, 501 (2013).

[16] M. Soylu, F. Yakuphanoglu, ***Mater. Chem. Phys***.143, 495 (2014).

[17] T. Ataseven, A. Tataroğlu, T. Memmedli, S. Özçelik, ***J. Optoelectron. and Adv. Mater.*** 14, 640 (2012).

[18] Ş. Karataş, F. Yakuphanoğlu, F. M. Amanullah, ***J. Phys. and Chem. Solids*** 73, 46 (2012).

[19] E. H. Nicollian, A. Goetzberger, ***Appl. Phys. Let.*** 7, 216 (1965).

[20] E. H. Nicollian, A. Goetzberger, ***Bell Syst. Tech. J***. 46, 1055 (1967).

[21] K. Sato, Y. Yasamura, ***J. Appl. Phys.*** 58, 3656 (1985).

[22] M. S. P. Reddy, J.-H. Lee, J.-S. Janga, ***Synth. Metals*** 185-186, 167 (2013).

[23] P. Chattopadhyay, A. N. Daw, ***Solid State Electron***. 29, 555 (1986).

[24] E. H. Rhoderick, R. H. Williams, ***Metal-Semiconductor Contacts***, 2nd Ed. (Clarendon Press, Oxford, 1978).

[25] S.S. Fouad, G.B. Sakr, I.S. Yahia, D.M. Abdel-Basset, F. Yakuphanoglu, ***Mater. Res. Bulletin*** 49, 369 (2014).

[26] D. S. Reddy, M. S. P. Reddy, V. R. Reddy, ***Optoelectron. Adv. Mater. Rapid Comm.*** 5, 448 (2011).

[27] C. Sah, Fundamental of Solid-State Electronics (World Scientific Publishing, Singapore, 1991).

[28] A. A. M. Farag, A. Ashery, F. S. Terra, ***Microelectron. J.*** 39, 253 (2008).

[29] Ş. Karataş, Ş. Altındal, A. Türüt, M. Çakar, ***Physica B,*** 392, 43 (2007).

[30] S.J. Moloi, M. McPherson, ***Rad. Phys. Chem***. 85, 73 (2013).

[31] K. K. Hung, Y. C. Cheng, ***J. Appl. Phys***. 62, 4204 (1987).

[32] B. Akkal, Z. Benamara, B. Gruzza, L. Bideux, ***Vacuum*** 57, 219 (2000).

[33] A. Tataroğlu, Ş. Altındal, ***Microelectron. Eng.*** 83, 582 (2006).

[34] R. T. Tung, ***Mater. Sci. Eng.*** R 35, 1 (2001).

[35] S. Chand, J. Kumar, ***J. Appl. Phys. A*** 63, 171 (1996).

[36] W. M. R. Divigalpitiya, ***Solar Energ. Mater.*** 18, 253 (1989).

[37] J. W. Kim, J. W. Lee, ***Appl. Sur. Sci.*** 250, 247 (2005).

[38] N. Kavasoğlu, C. Tozlu, O. Pakma, A. S. Kavasoğlu, S. Özden, B. Metin, Ö. Birgi, Ş. Oktik, ***Synthetic Met.*** 59, 1880 (2009).