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A New Topology for UPQC Based on Reduced-Switch-Count Converter

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ABSTRACT

Recently, reduced switch count converter switch numerous advantages such as low cost and weight, small size and high reliability have been introduced to be used in unified power quality conditioner (UPQC). In this paper a novel topologyfor UPQC based on back-to-backB4 converter and its control system are proposed. The conventional UPQC consists of twelve switches while the proposed topology for UPQC has 8 switches. By reducing the number of switches, the price of the whole system and losses are decreased. In addition, the proposed control system can be used in conventional UPQC when one of converter legs has a faulty condition. This increases reliability of the system. Special control and modulation schemes have been offered to compensate oscillations in load and utility currents and voltages and also input power factor of UPQC. The experimental and simulation results verify the efficiency of proposed control and modulation schemes of proposed topology.

Keyword: Unified Power Quality Conditioner (UPQC), Reduced Switches Count Converter, B4 Inverter

1. INTRODUCTION

Nowadays, increasing interest for efficient non-linear loads like rectifiers, inverters, adjustable speed drives and etc, has increased harmonic current injection to the utility that hascaused great concernsabout other customers and grid.In recent years, usage of sensitive deviceshas been increased that need high quality power supply. Temporary interrupts, voltage distortions and other power quality issues has destructive effects for the modern and sensitive loads. Recently,power quality issues havebecome a major problem for utilities and customers [1-4]. The unified power quality conditioner (UPQC) is one of the most important and effective custom power devices which has a wide ability to solve most of power quality problems [5-11]. UPQC consists of a shunt and a series converters withcommon DC-link. Therefore, this device can compensate all of voltage and current distortions, such as voltage sag and swell, poor power factor, current and voltage harmonicsand etc. The role of series converteris to inject a series voltage into the line in order to compensate the harmonic,unbalance and other voltage distortion at source side. Therole of shunt converter is to compensate the currents unbalance and harmonicsof the load current and power factor and to regulate DC-linkvoltage. Reduction of the number of switches is one of the ways to reduce UPQC' cost. In order to reach this purpose, a UPQC topology based on nine-switch converter has been presented in [12]. The nine-switches-double-output converter can operate in differentfrequency (DF)and constant frequency (CF) modes.In DF mode, the sum of modulation indexes of two outputs equals toone. Since in

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the UPQC applications, the injected voltage by series converter is small, about 0-0.3 p.u., though the modulation index for series converter will be small. But the output voltage of shunt converter should be greater than the grid voltage.Therefore, for proper operation of UPQC based on nine-switch converter, the DC-link voltage should be considerably increased. An alternative concept is proposed in this paper, where the four switch converter is chosen to replace a shunt and a series converter found in conventional twelve switch power conditioner. The B4 converter uses four switches to form two phase legs with its third phase drawn from the midpoint of a split dc capacitive link. For tying two ac systems together, two B4 converters as a proposed converter are needed with their split dc link shared. The total number of switches in the proposed converter is eight, which probably is the minimum achievable for interfacing two ac systems. Two sets of control schemes are designed for the proposed topology. The first control schemes are proposed to compensate for harmonic currents, reactive power flow and three-phase unbalance caused by nonlinear loads is proposed to proposed converter. With the proposed method, the grid currents drawn from the utility are then sinusoidal, having only fundamental component. Also, the second control scheme which is the series inverter control, are designed to compensate for any detected grid voltage harmonics and unbalance, so that only a set of balanced three-phase voltages appears across the loads under normal operating conditions . During voltage sags, the series inverter control scheme also has the ability to continuously keep the load voltages within tolerable range.

This paper is composed of seven sections. In second section, the proposed topology and its modulation method is presented in details. In third section, proposed control methods for series and shunt converters are presented. After introducing theproposed topology and control methods, in fourth section, the switching losses are calculated. In nextsection, the simulationresults for different operation conditions are presentedsixth sectionpresents the experimental results. These results confirm the proper operation of proposed topology, modulation method, control system and verify simulation results. Finally, the last section is dedicated to conclusion.

2. PROPOSED TOPOLOGY AND MODULATION METHOD

UPQC based on the conventional back-to-backconverter, inwhich one of the legs in series and shunt converters is eliminated, is shown in Fig. 1. In proposed topology for UPQC, instead of using B6 inverter, B4 inverter is used.

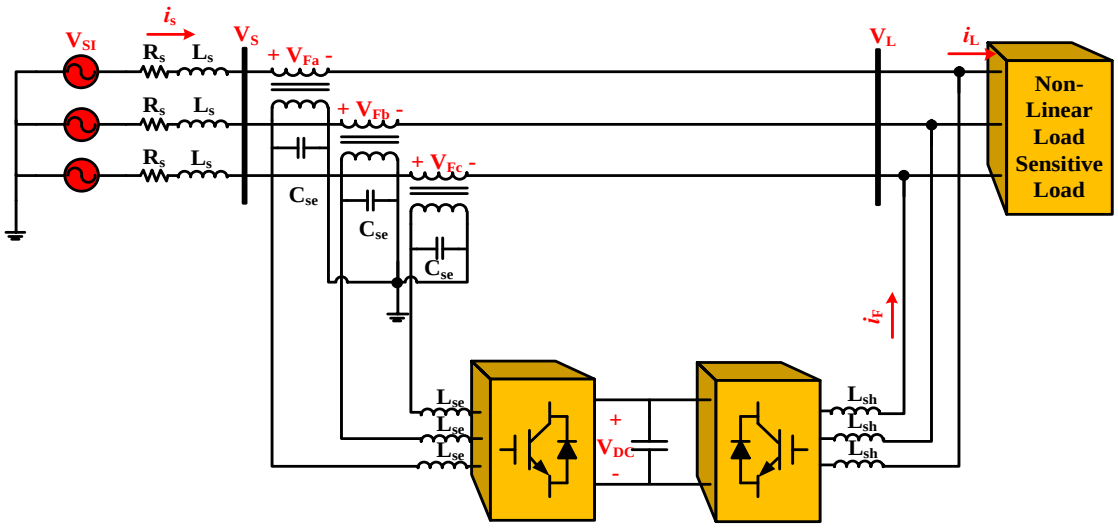

Fig. 1: UPQC based onconventional back-to-back structure

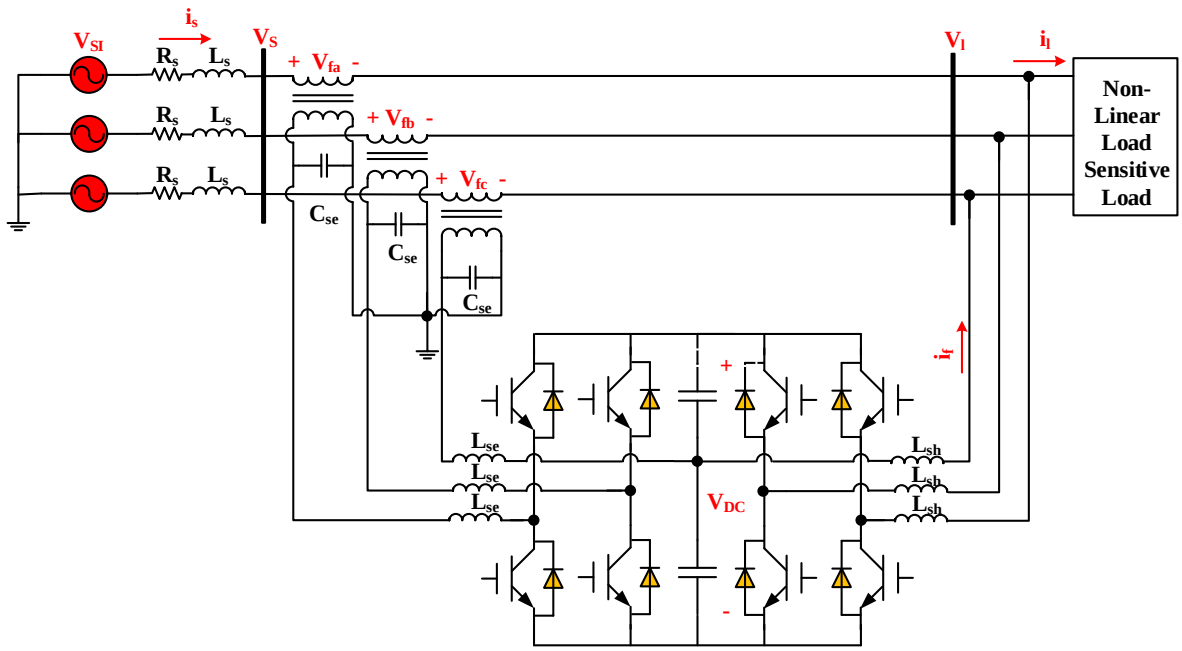

Fig. 2: Schematic circuit of UPQC based on back-to-backB4 structure

Fig. 2 shows the circuit diagram of proposed topology of UPQC based on back-to-back B4 converters. The number of switches in proposed topology is eight while it is twelve in the conventional topology. Therefore, due to less number of switches in proposed topology, the cost of UPQC for low voltage applications (low voltage distribution system) and switching losses will be lower in comparison with conventional topology.

2.1. B4 InverterStructure

Inlowvoltage application, the reduced switch count topologies have attracted a great attention in industry. The most well-known reduced switch count topology is B4 converter which was introduced by Van Der Broeck[13]. Fig. 3 shows so-called B4 inverter with four switches and three output phases. In this structure, one leg of conventionalthree-phase inverter have been eliminated and replaced with two series capacitors. In this case the third phase of inverter is connected to the mid-point of series capacitors.

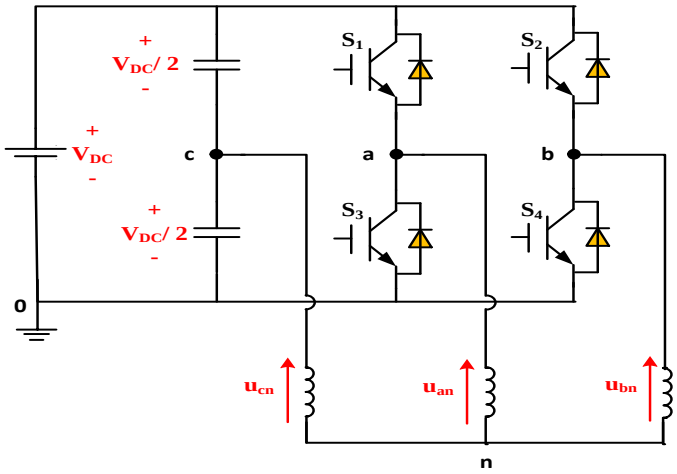

Fig. 3: Four-switch B4converter

There are two methods for B4 inverter's switching [13, 14-17]:

1. Carrier Based Pulse WidthModulation (CBPWM)
2. Space Vector Modulation (SVM)

2.1.1. Carrier Based Pulse Width Modulation (CBPWM)

This inverter has two legs. Consequently in this modulation method, two reference signal is required. The reference signal of B4 inverter in the UPQC structure, are generated using shunt and series controllers.Since, line voltage of converter is controllable, these references which are defined as follows and are shown in Fig. 4:

$$V_{ref,ba} = m\sin(\omega t) \quad (1)$$

$$V_{ref,ca} = m\sin(\omega t + \frac{\pi}{3}) \quad (2)$$

Where m is modulation index and ω is the output voltage angularfrequency. As it can be seen in Fig. 5, these signals are compared with carrier signal and the logical results of the comparison define the gate pulses.If the reference signal is greater than carrier signal, the upper switch of each leg is turned on. If not, the lower switch of each leg is turned on.

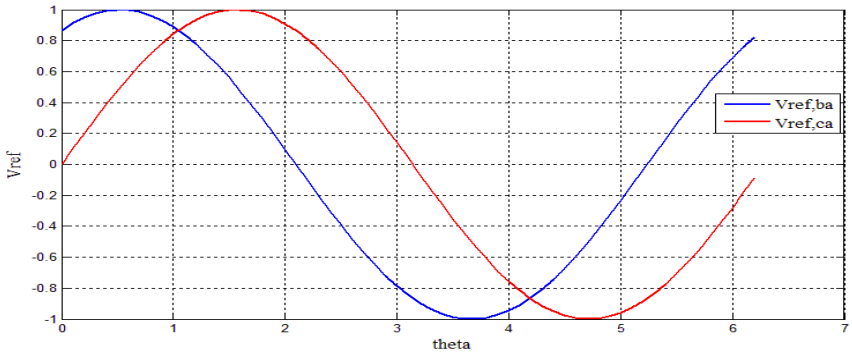

Fig. 4: Reference signal for B4 inverter

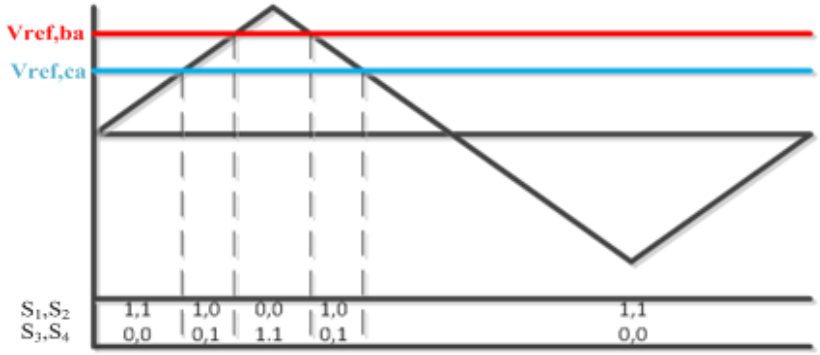

Fig. 5: CBPWM switching method for B4 inverter

Consequently, the maximum phase output voltage (u_m)by SVM method is the same as CBPWM and can be calculated as [16]:

$$U_{\mathrm{m}} = \frac{1}{\sqrt{3}}\frac{V_{dc}}{2} \quad (3)$$

This value is equal to phase voltage amplitude where the modulation index of PWM method is consideredto be one. Likeas conventional B6 inverter, the B4 inverter operates as a step-down converter butin comparison with B6 inverter, it can be seen that the output voltage of B4 inverter has decreased by a factor of $\sqrt{3}$.With assuming the same load for both converters, a comparison between B6 and B4 converters isderived as follows:

1. Less number of switches in B4 structure causes the lower costin low voltage applications than B6 inverter.
2. Withsame output voltage, the maximum peak inverse voltage (PIV) for switches in B4 converter will be more than B6 converter.
3. Due to less number of switches inB4 converter,the conduction losses of B4 converter

will be lower than conduction losses for B6 converter.

The most important characteristic for a converter is the peak inverse voltage (PIV) of on switches.The PIV and number of switches performa great role in the cost of converters. The PIV of switches in UPQC, based on traditional back-to-back structure, nine-switch topologyand proposed topology based on B4 inverterare given in Table 1.

According to (3), the maximumamplitudeof phase voltage in the proposed topology has been increased by a factor of $\sqrt{3}$ in comparison with conventional back-to-back structure. Therefore, in the proposed topology the DC-link voltage should be regulated as $\sqrt{3}$ times greater than the DC-link voltage in conventional topology based on back-to-back structure.

Table 1: The PIV of switches for different topologies of UPQC

	Conventional back-to-back structure	*Nine-switch converter*	*Proposed structure*
PIV	$12V_{dc}$	$9*2V_{dc}$	$8*\sqrt{3}V_{dc}$

3. B4 INVERTER'S CONTROL SCHEME IN THE PROPOSED UPQC

In this paper, the synchronous reference frame theory isappliedas control system of proposed UPQC. The CBPWM and hysteresis methods are used asmodulation methodsof series and shunt B4 converters, respectively. Different types of carrier based modulation methods are introduced in [18].

UPQC control system consists of two subsystems [19]:

- Shunt inverter control system.
- Series inverter control system.

Shunt inverter's control system, based onsynchronous reference frame theory is shown in Fig. 6(a). i_{la}, i_{lb} and i_{lc} are load currents and v_{sa}, v_{sb} and v_{sc} are source voltages. The synchronous reference frametransformation (Park's transformation) isused to transform the measured load currents into dq0 frame. Direct and quadrature components of load current can be decomposed into AC and DC components.Thesecomponents are separated by a low-pass filter.

$$i_{ld} = \bar{i}_{ld} + \tilde{i}_{ld}, \quad i_{lq} = \bar{i}_{lq} + \tilde{i}_{lq} \quad (4)$$

For factor correction and load current harmonicscompensation, the reference currents of shunt converter are calculated as follows:

$$i^*_{fd} = \tilde{i}_{ld}, \quad i^*_{fq} = i_{lq} \quad (5)$$

After injecting the reference currents by shunt converter, the utility side currents will be as follows.

$$i_{sd} = \bar{i}_{lq}, \quad i_{sq} = 0 \quad (6)$$

Due to power losses and series inverter's real power injection, DC-link voltage fluctuates. Thus, a PI controller is used to regulate the DC-link voltage (Fig. 6(a)).

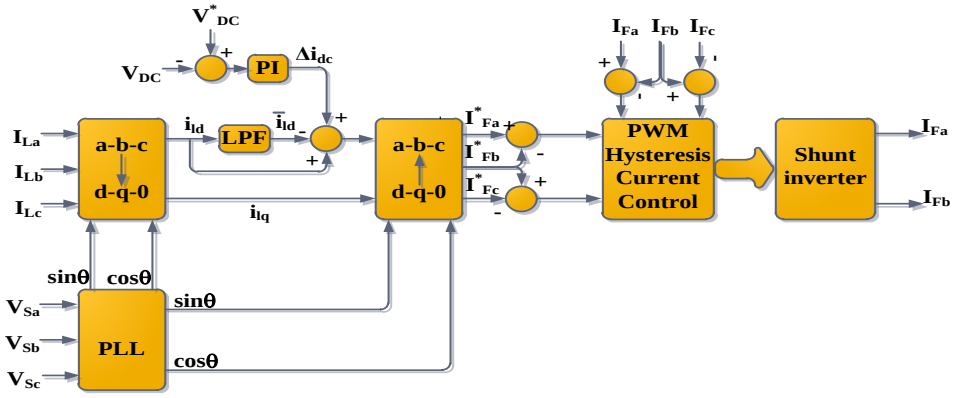

Fig. 6(a). Shunt B4 inverter's control system

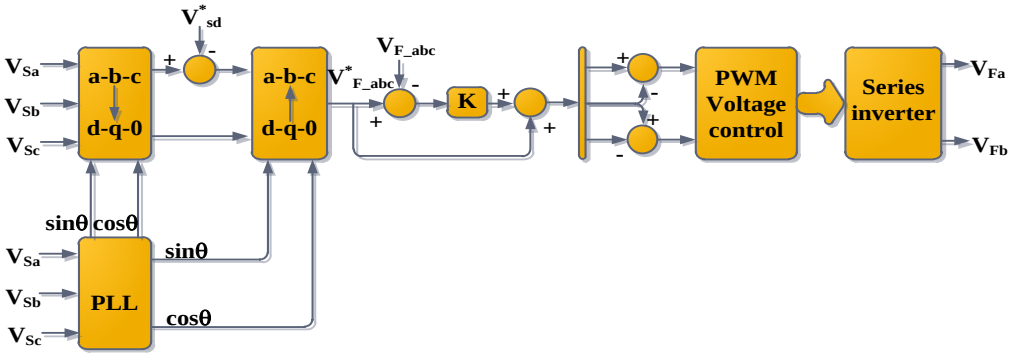

Fig. 6(b). Series B4 inverter's control system
Fig. 6: Control system of proposed UPQC

By injecting or absorbing active power through the utility, the shunt converter regulates theDC-link voltage. The PI controller output, Δi_{dc}, is added to d component of reference current. Finally, the dq components of reference current can be stated as follows:

$$i_{cd}^{*} = \tilde{i}_{ld} + \Delta i_{dc}, \quad i_{cq}^{*} = i_{lq} \quad (7)$$

As seen in Fig.6(a), the reference currents in synchronous reference frame are transformed to abc components using the inverse park's transformation. Difference between the reference currents ($i_{fa}^{*}, i_{fb}^{*}, i_{fc}^{*}$) and output currents of shunt inverter (i_{fa}, i_{fb}, i_{fc}) are fed to hysteresis current control block that produces gate signals for shunt inverter's switches.

Load side voltage control is done through the series B4 inverter of UPQC. The control system of series B4 inverter is used to calculate reference signals in order to compensate the voltage unbalance and distortions. The control system for Series inverter is illustrated in Fig. 6(b).In order to preserve the load voltage at its constant value, reference voltage is compared with direct component of load voltage. Regarding, error is defined as the difference between the injected reference voltage and the measured voltage.

It is obvious that the controllability of the system can be enhanced, if the error value decreases. In this regards, the obtained error is multiplied by k and then is added to injected reference voltage. The series connected converter is controlled as a two phase system, because it composed by two legs. The required switching pulses for each switch are produced by using PWM method. The values of decrease in are listed in table (2).

Table 2: values parameters control

Shunt converter		Series converter
k_p	k_i	k
0.5	0.04	5

4. LOSS CALCULATION FOR PROPOSED TOPOLOGY

In the proposed topologyfor UPQC the number of switches is reduced. It should be noticed that PIV of the switches in is increased, in return. Converter's losses (P_L) can be divided to conduction loss (P_{cond}) and switching loss (P_{sw}). Conduction loss is due to the non-ideal current–voltage characteristic of semiconductors (diodes and IGBTs) and switching loss is due to drastic changes of current and voltage in switching intervals [20, 21].

4.1. Conduction Losses

Conduction loss of IGBT can be calculated using the equivalent circuit of IGBT in the state of being on. This circuit consists of a DC voltage source (u_{CE0}) which representsthe IGBT on-state zero-current collector-emitter voltage and a collector-emitter on-state resistance (r_C)

$$u_{CE}(i_C) = u_{CE0} + r_C.i_C \quad (8)$$

The same definition can be used for the anti-parallel diode:

$$u_D(i_D) = u_{D0} + r_D.i_D \quad (9)$$

The instantaneous value for IGBT conduction loss can be written as:

$$p_{CT}(t) = u_{CE}(t).i_C(t) = u_{CE0}.i_C(t) + r_C.i_C^2(t) \quad (10)$$

Defining the average current of IGBT as I_{cav}, and its rms value as I_{crms}, the average conduction loss of IGBT can be expressed as follows:

$$P_{CT} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_T(t)dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} (u_{CE0}.i_C(t) + r_C.i_C^2(t))dt = u_{CE0}.i_{cav} + r_C.i_{crms}^2 \quad (11)$$

And instantaneous value of the diode conduction losses is:

$$p_{CD}(t) = u_D(t).i_D(t) = u_{D0}.i_F(t) + r_D.i_D^2(t) \quad (12)$$

If the average and rms values of diode current are considered as I_{Dav} and I_{Drms} then conduction loss for diode during the switching period ($T_{sw}=1/f_{sw}$) will be calculated as follows:

$$P_{CD} = \frac{1}{T_{sw}} \int_0^{T_{sw}} p_{CD}(t)dt = \frac{1}{T_{sw}} \int_0^{T_{sw}} (u_{D0}.i_D(t) + r_D.i_D^2(t))dt = u_{D0}.i_{Dav} + r_D.i_{Drms}^2 \quad (13)$$

4.2. Switching Losses

The turn-on energy losses in IGBT (E_{onT}) can be calculated as the sum of the switch-on energy without taking the reverse recovery process into account (E_{onTi}) and the switch-on energy caused by the reverse-recovery of the free-wheeling diode (E_{onTrr}):

$$E_{onT} = \int_0^{t_{ri}+t_{fu}} (u_{ce}.i_c(t)dt = E_{onTi} + E_{onTrr} \quad (14)$$

The peak value of the reverse-recovery current can be calculated as:

$$I_{Drrpeak} = \frac{2.Q_{rr}}{t_{rr}} \quad (15)$$

Great portion of turn-on energy in the diode consists of the reverse-recovery energy (E_{onD}):

$$E_{onD} = \int_0^{t_{ri}+t_{fu}} (u_D(t).i_F(t)dt \approx E_{onDrr} = \frac{1}{4}.Q_{rr}.U_{Drr} \quad (16)$$

Where, U_{Drr} is the diode voltage during reverse recovery interval. For the worst case calculation this voltage can be approximated with DC-link voltage ($U_{Drr}= U_{DD}$). The turn-off energy loss for IGBT can be calculated in the similar manner which is mentioned in calculating the turn on energy losses. The turn-off losses for the diode is normally neglected ($E_{offD}\approx 0$). Therefore:

$$E_{offT} = \int_0^{t_{ru}+t_{fi}} u_{ce}(t).i_c(t)dt \quad (17)$$

The switching loss for IGBT and diode can be calculatedas product of switching energies and the switching frequency (f_{sw})like:

$$P_{swM} = (E_{onM} + E_{offM}).f_{sw}$$
$$P_{swD} = (E_{onD} + E_{offD}).f_{sw} \approx P_{swM} = E_{onD}.f_{sw} \quad (18)$$

Power losses in IGBT and free-wheeling diode can be expressed as sum of the conduction and switching losses which results in:

$$P_T = P_{cT} + P_{swT} = u_{CE0}.i_{cav} + r_C.i_{crms}^2 + (E_{onT} + E_{offT}).f_{sw}$$

$$P_D = P_{cD} + P_{swD} = u_{D0}.i_{Dav} + r_D.i_{Drms}^2 + E_{onD}.f_{sw} \quad (19)$$

5. SIMULATION RESULTS

In this study, powercircuitconsists of a 3-phase 3-wire system witha non-linear load which is composed of a three phase diode rectifier with RL load. The parameters of the system and load are presented in Table 3.

Table 3: Characteristics of test system

Value	Parameter
$220v / 50Hz$	Source Phase Voltage (V_s)
11.5Ω	Load Resistance (R_l)
$12mH$	Load Inductance (L_l)
$1100v$	DC-link voltage (V_{DC})
$3mH$	Shunt inverter Inductance (l_{sh})
$10\mu F$	Shunt inverter Capacitance (C_{sh})
$3mH$	Series inverter Inductance (l_{se})
$15\mu F$	Series inverter Capacitance (C_{se})
$20kHz$	Switching Frequency

In the proposed topology, the third phase of both shunt and series converter isconnected to DC-link mid-point.In this study, the capacitance of both capacitors has been considered to be 2000µf. Increasing the capacity of capacitorscauses to slow dynamic response and a decrease in capacitor voltage ripple.Some disturbances such as sag, swell, harmonic(i.e. 5, 7 and 11) and flickerare considered to evaluate the operation of the suggested UPQC topology. The detailed propertiesof these disturbances are given in Table 4. The source side voltage, load side voltage and injected voltage through the series inverter of UPQC for four types of above mentioned disturbances are shown in Figs. 7. (a)-(d). As it can be seen from these figuresUPQC's series inverter compensatesthe load side voltage properly and turns it into balanced sinusoidal three-phase voltages. The presented simulation results show that the utility side disturbances are not observed at load side voltage.

Table 4: Characteristics of utility side disturbance

Disturbances utility side	Occurred time	Amplitude voltage	Frequency
Sag	0.5-0.6 s	62v	50Hz
Swell	0.7-0.8 s	62v	50Hz
Flicker	0.9-1 s	70v	20Hz
harmonic	1.1-1.2 s	30,50,70v	550,350,250Hz

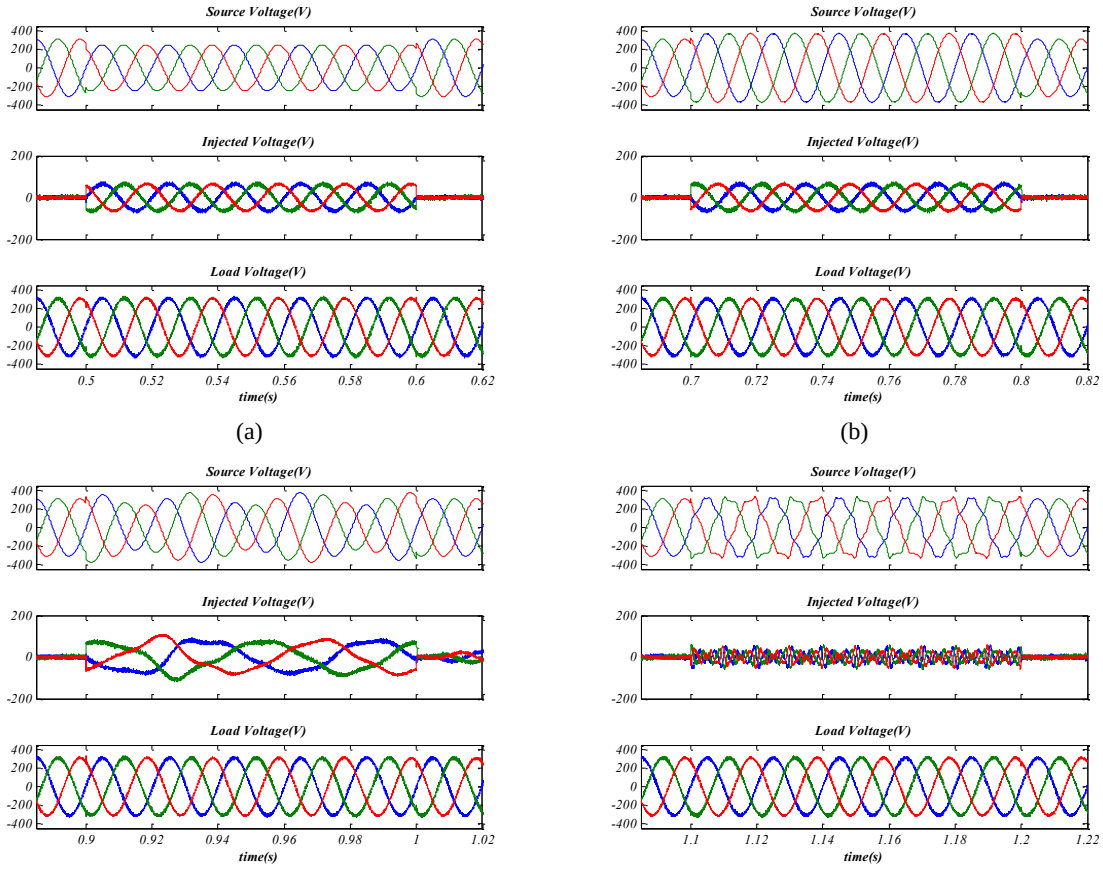

Fig. 7: Source side voltage, Injected voltage by series inverter of proposed UPQC, load side voltage for different disturbances in the utility side
(a) sag(b) swell (c) flicker (d) harmonic

In order to show the proper operation of UPQC's shunt inverter, a non-linear load which consistsof a diode rectifier with RL load, connected to the utility is considered. In this case the THD of non-linear load'scurrents is more than 17%.The source side current, load sidecurrentand injected current by UPQC's shunt inverter arepresented in Figs. 8(a)-(d) forfour types of disturbances in source side voltages. The presented results show that with good performance of UPQC's shunt converter, thesource sidecurrent are almost free of harmonics and in phase with source side voltages (Fig. 9(a)) and the reactive power which is required by load is provided by UPQC. Fig. 9(b) shows the utility side and load side reactive powers.

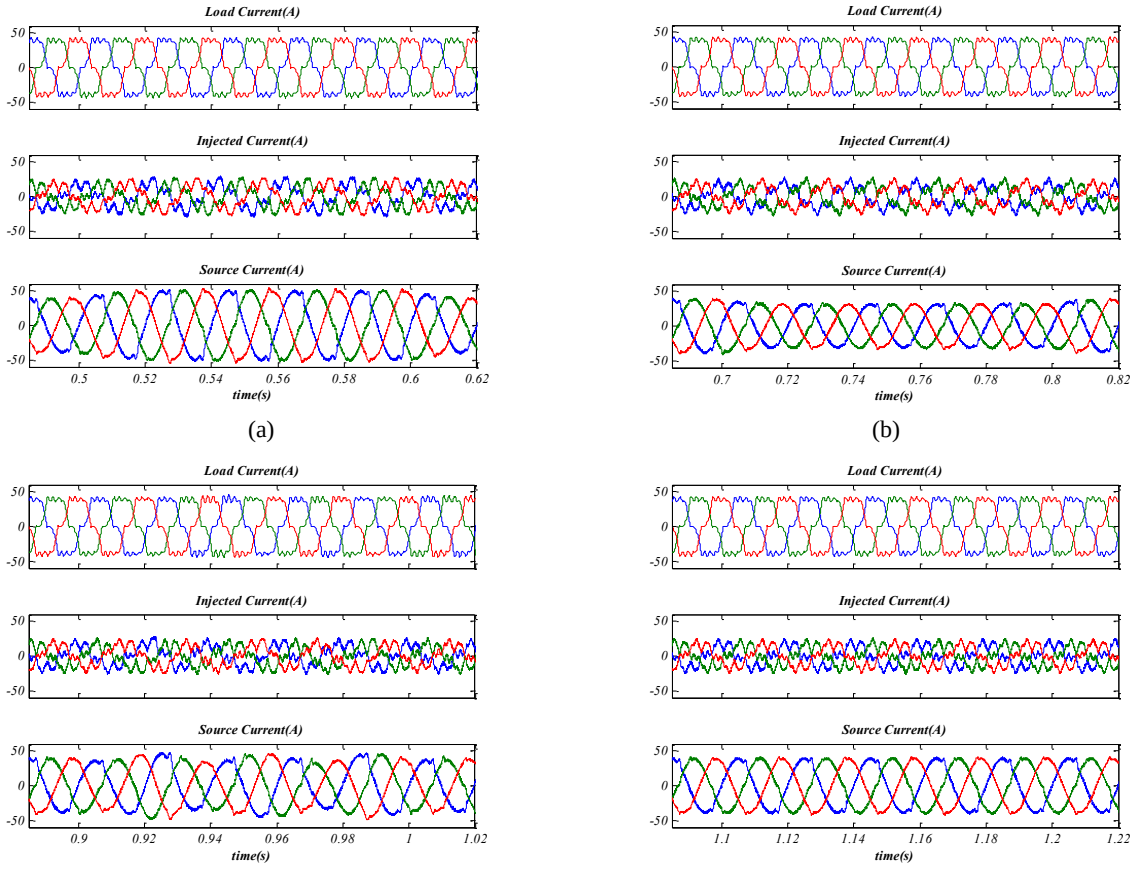

Fig. 8:Loadside current, Injected current by UPQC's shunt inverter, load side currentfor different disturbances (a) sag (b) swell (c) flicker (d) harmonic

According to (7), voltage gain of B4 converter is $1/\sqrt{3}$ times of conventional back-to-back converter. Therefore, to generate a voltage with same amplitude in two topologies, the DC-link voltage in B4 structureshould be increased up to $\sqrt{3}$ times. The DC-link voltageunder differentdisturbances is shown in Fig. 9(c).It can be seenfrom this figure that the DC-link voltage is properly regulated at its reference value 1100v due to proper operation of presented DC-link voltage controller.

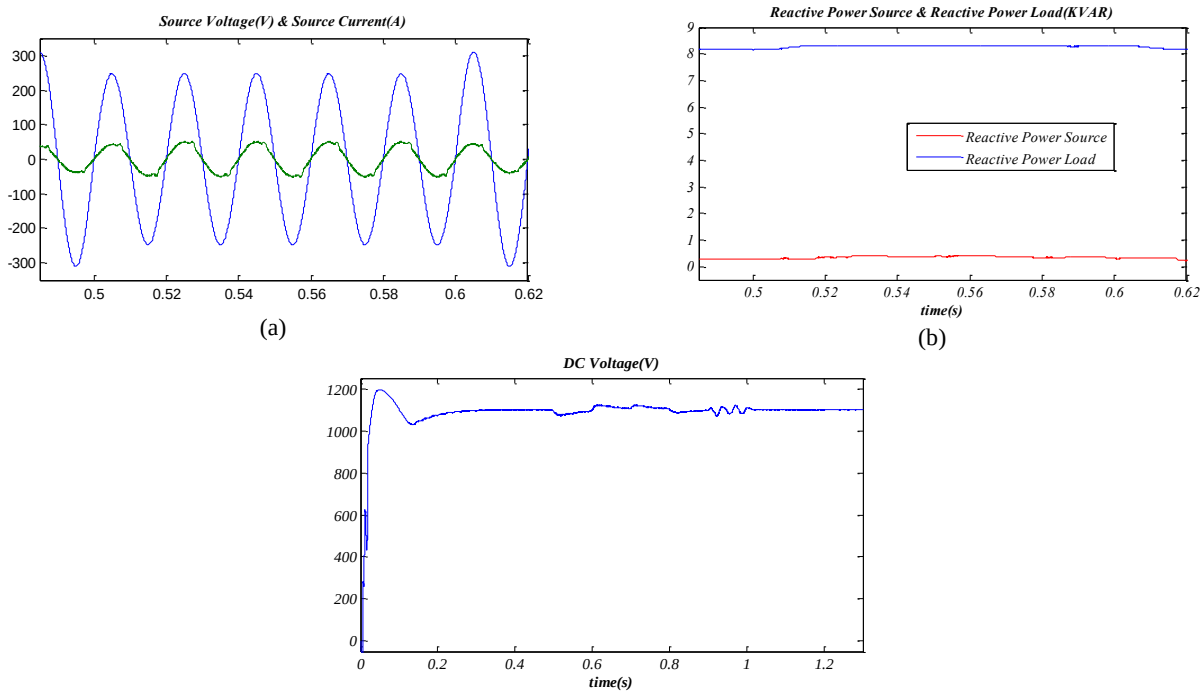

Fig. 9:(a) source voltage and current(b) source and load reactive powers, (c) DC-link voltage

One of the important parameters in power qualityissues is THD of load voltages and source currents.The THD and amplitude of fundamental component of load voltage and source current under different disturbances such as sag, swell, flicker and distorted source voltage are given in Table 5 when the suggested UPQC is installed.

The results of Fourier analysis (FFT) indicate that THD of source side current, depending on the type of disturbance, reaches a value within 6.25-11.35%.It should be noted that this value has been improved respect to the THD of pre-compensated load current (17%). The data presented in this table shows that the value of THD for load side voltage and utility side current meet power quality standards [1].

Table5: THD and amplitude of fundamental componentof load voltage and source current in different disturbances

INDEX		*Sag*	*Swell*	*Flicker*	*Harmonic*
Load Voltage	*THD*	*2.71%*	*2.57%*	*3.49%*	*2.55%*
	Fundamental	*313.5 (V)*	*308.2 (V)*	*311.1 (V)*	*311 (V)*
Source Current	*THD*	*5.34%*	*4.25%*	*7.35%*	*4.56%*
	Fundamental	*50.96 (A)*	*31.71 (A)*	*40.68 (A)*	*39.73 (A)*

To calculate the switching losses in UPQC based on the back-to-back converter, nine-switchconverter and proposed topology, the equation (23) is used. The required parameters forloss calculationare given in [22]. The results for power losses calculationfor back-to-back,nine-switch and proposed topology are presented in Table 6.The load and source parameters are considered to be same for three topologies.

Table 6: Calculated losses for back-to-back, nine-switch and proposed topology

	Back-to-back	*Nine-switch*	*Proposed topology*
Losses	*485W*	*550W*	*310W*

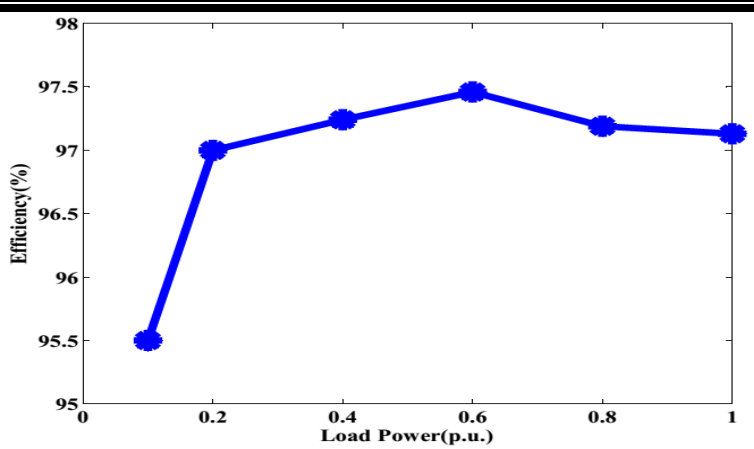

Fig. 10: Simulation efficiency of the proposed converter as a function of different Load power

Fig. 10 shows the converter proposed efficiency curves obtained for load different. The nominal power of load is considered as 14kw for activepower and 7kvar for reactive power. The maximum efficiency 97.5% is achieved at 0.6 p.u. load condition.

6. EXPERIMENTAL RESULTS

For implementing a prototype of proposed UPQC, based on back-to-back B4converter, the BUP400D [23]and HCPL316j[24] are used as power IGBT and IGBT drivers, respectively and the control system is implemented on aTMS320F2812 DSP.

In the test case, a Thyristor based rectifier as nonlinear load and a voltage source with sag depth of 0.2 p.u. are considered. The parameters of test system are given in Table 7. Fig. 11 shows thesource voltage, injected voltage and load voltage inabovementioned conditions. It can be seen from this figure that the load side voltage is not been affectedby utility side voltage sag. This confirms the proper operation of series converter in proposed UPQC and its control system.

Table 7: Characteristics of test system

Utility side disturbance	**time**	**Injected voltage**	**Source Phase Voltage**	**DC-link voltage**
Sag	0.1 s	30v	150v (peak)/50Hz	500v

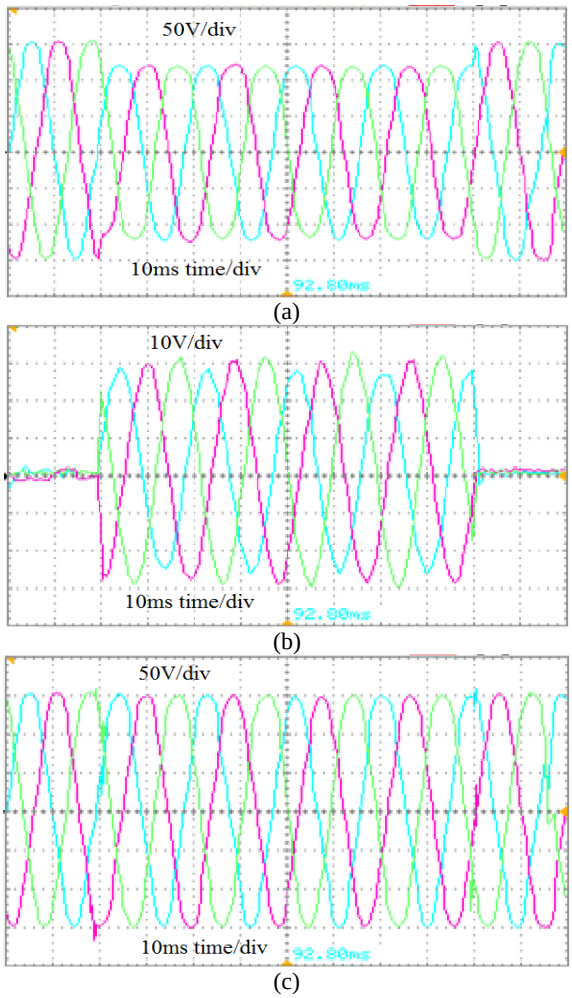

Fig. 11: (a) Source voltage (b) Injected voltage (c) load voltage during voltage sag

To show the proper operation of shunt converter of proposed UPQC and its control system, the load currents, injected currents by shunt converter and utility side currents of same test case are presented in Figs 12 (a)-(c), respectively. It can be seen from these figures that after compensation the utility side currents are nearly sinusoidal while the load currents are non-sinusoidal. These results confirm proper operation of shunt converter in proposed topology for UPQC and its control system.

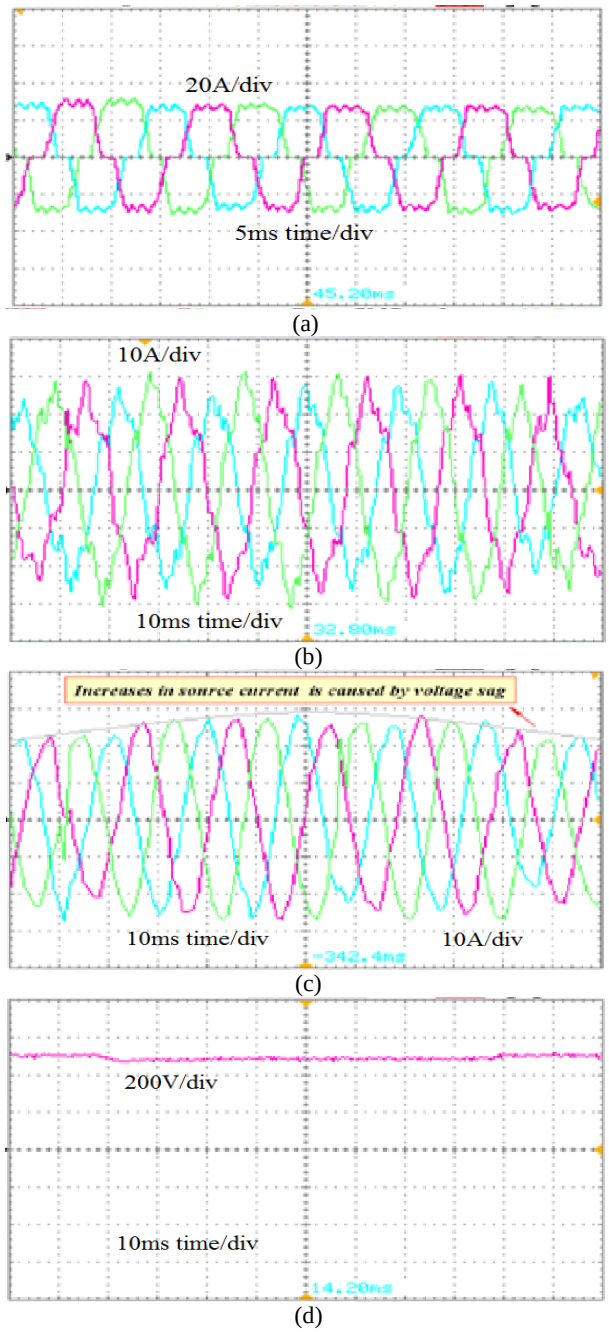

Fig. 12: (a) Load current (b) Injected current (c) Source current (d) DC-link voltage duringvoltage sag

The measured DC-link voltage is presented in Fig. 12(d). This figure shows that the DC-link voltage regulator have properly regulates the DC-link voltage at its reference value.

7. CONCLUSION

In this paper design, simulation and implementation of aunified power quality conditioner (UPQC) based on back-to-backB4 converter ispresented applying synchronous reference frame theory. The number of switches in the proposed topology for UPQC is decreased in comparison with previouslyproposed topologies. ThePIV of the switches in the proposed topology is greaterin comparison with topology based on conventional back-to-back converter but lower than the PIV of the switches in the nine-switch converter. Also the proposed topology as four and one less switches in comparison with

above mentioned topologies, respectively. The proposed UPQC topology can lead to a decrease in whole system cost, power lossesand an increasein efficiency and reliability ofthe system because of less number of circuit elements. Simulation results show the ability of proposed UPQC topologyin the voltage distortion, reactive power and harmonic current compensation. The PI controller stabilizes DC-link voltage by balancing the power between series and shunt inverters.Experimentalresults confirm the results achieved from simulation by MATLAB/SIMULINK.

CONFLICT OF INTERESTS

The authors declared that there is no conflict of interests.

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