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A Majority Gate Based RAM Cell Design With Least Feature Size In QCA

Amanpreet SANDHU[1,*], Sheifali GUPTA[1]

[1] *Chitkara University, Department of Electronics and Communication Engineering, 140401, Rajura, India.*

Highlights

- This paper first proposes a design of a new five input majority gate.
- The proposed gate occupies 44.4% less area than the best-reported designs.
- The correctness of the proposed gate is proved by designing a new RAM cell.
- The proposed RAM cell is efficient in terms of area with lower energy dissipation.
- The proposed designs can be used for both single and multilayer architecture.

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Abstract

Designing and fabricating complementary metal-oxide semiconductor (CMOS) based logic devices at nanoscale faces serious issues like oxide thickness, thermal reliability, and energy dissipation. Hence the industries are in search of new technologies which could substitute the scaling down of CMOS circuits. Quantum-dot-cellular-automata (QCA) is an imminent technology considered at nano-level with the high speed of operation and lower power dissipation features. As the memory is used in most of the electronic equipment for data storage purpose, designing a RAM cell with a reduced number of QCA cells, and lower energy dissipation finds wide applications in the electronics industry. This paper first proposes a five input majority gate which may be utilized efficiently for designing single layer QCA circuits. Then by using the invented gate, a coplanar RAM cell structure with Set and Reset capability is devised. The structural and energy dissipation analysis of presented structures are estimated using QCADesigner and QCAPro tools. The results prove that the disclosed RAM cell architecture achieves 12.5% lower area, 18.26% lower total energy dissipation, and 16.6% lower input to output delay than the best-reported design.

1. INTRODUCTION

In the past few decades shrinkage in VLSI design based logic circuit dimension has faced some serious challenges like high power consumption, short channel effects, leakage currents, oxide thickness, and thermal reliability [1]. QCA is one of the potential candidate technology for the replacement of VLSI circuits at the nanoscale in the coming days [2]. It is recognized as one of the innovative phenomena for enumerating logic circuits at nano-scale [3]. Among various nanotechnologies, QCA overcomes the disadvantages of CMOS technology and offers a faster speed of operation, higher device density, and lower power consumption [4]. Since memory is one of the powerful element in the digital system the design of highly optimized RAM cell in nanotechnology leads to substantial improvement in performance parameters of QCA designs. Reconfigurability of a memory cell with QCA will add a new dimension [5] for the improvement in parameters like the number of cells, Input to output delay, occupation area, and total energy dissipation. Many logic gate designs such as flip flops [6-7], multilayer structures [8], and counters [9] have been implemented using QCA during recent years. These logic designs are modeled and verified by an open source simulator named as QCADesigner tool [10]. The objective of the paper is to design a five input majority gate and construct a RAM cell based on a new majority gate. The working of presented structures is inspected using QCADesigner tool [11].

*Corresponding author, e-mail: amanpreet.sandhu@chitkara.edu.in

The new coplanar majority gate schematic is utilizing 17 QCA cells with 0.01μm^2 area, and having energy dissipation of 41.97 meV. It has a smaller area, less QCA cells and less power in comparison to the existing designs. The presented gate design can be used for both single as well as multilayer structures because its input and output cells are reachable for the single layer as well as multilayer with no interference. For the same reason, it can be extendible for any type of QCA logic circuit design.

The new RAM cell design is utilizing 85 QCA cells having an area of 0.07 μm^2 with total delay is 1.25 clock cycles. It has a smaller area, lower QCA cells, lower energy dissipation, and lower latency as compared to the existing designs in the literature. The disclosed RAM cell design can be used for both single and multilayer structures because it's input and output cells are reachable from a single layer as well as a multilayer.

The remaining part of this article is arranged as follows: In Section 2, the basics of QCA fundamentals and its clocking scheme has depicted. The literature review of existing majority gates is detailed in section 3. The structural analysis, energy dissipation analysis, and the simulations of a newly designed majority gate are investigated in section 4. In section 5, firstly showcase a glance of existing RAM cell structures, and then a new RAM cell based on newly designed majority gate is presented along with its energy dissipation analysis. Section 6 presents the conclusion of the paper.

2. BASIC QCA FUNDAMENTALS

QCA is one of the latest upcoming nanotechnologies which replaces the CMOS structures at the nanoscale level. The QCA cell is the fundamental structure which can create all elements of a circuit (wiring and computing). The QCA cell consists of four quantum dots which are located at the extreme edges of a quantum cell. Out of which, two quantum dots contain free electrons in a diagonal direction. These two electrons can exchange their positions by lowering the barrier potential between them to achieve P = +1 or P = -1 polarization state [12] is illustrated in Figure 1. The electrons always confine within a QCA cell and never tunnel between the adjacent QCA cells. When an array of QCA cells placed adjacent to one another to form a wire only a polarization state (columbic charge) will travel along the wire.

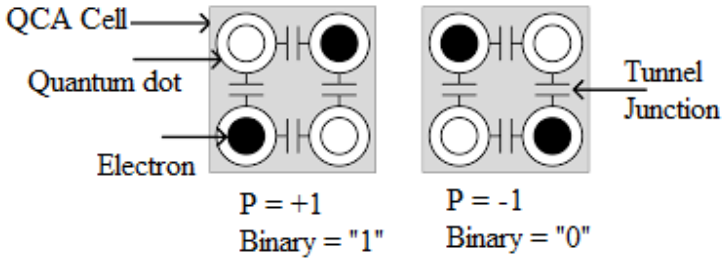
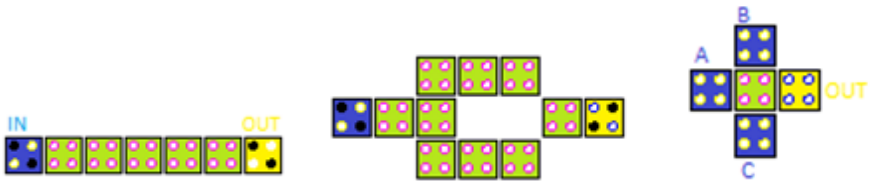


Figure 1. *QCA Cells with Two Polarization States [12]*

Such a pattern of QCA cells is used to construct wire or any logic structure. As a result, there is less power dissipation because of the absence of the flow of electrons. The QCA wire is created by cascading the cells as depicted in Figure 2(a). Other QCA structures like the inverter and majority gate of three inputs can also be constructed using these quantum cells [13]. An inverter circuit of Figure 2(b) inverts its state because the output cell is in the diagonal orientation (interaction) with respect to the adjacent QCA cell. The QCA based 3-input majority structure is illustrated in Figure 2(c). Its function is exhibited by the equation given in (1):

$$M(A, B, C) = AB + BC + AC \quad (1)$$



(a) (b) (c)

Figure 2. *(a)Connecting Wire (b) Inverter (c) 3-Input Majority Gate [13]*

A QCA cell is polarized by an external supply called clock signal [14] for control of power and data flow is depicted in Figure 3. The potential barrier within a QCA cell determines its logic level i.e. either logic '0' or logic '1'. These logic levels are determined by four clock phases such as a switch, hold, release, and relaxed phase. There exists a phase difference of π/2 within each clocking phase. In the switch phase, the barrier potential of a QCA cell starts increasing, hence moving from unpolarized state to polarized state. In Hold phase, the barrier potential will remain constant and the QCA cell is completely polarized. Now it becomes independent of its neighboring cells. In the release phase, the barrier potential of QCA cell starts reducing, hence moving from polarized state to unpolarized state. In the relax phase, the barrier potential becomes zero and the cell gets unpolarized [15].

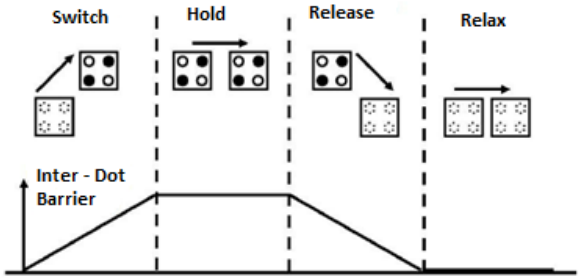


Figure 3*.QCA Clocking with Four Phases [14]*

3. PROPOSED FIVE-INPUT MAJORITY GATE

3.1. Review of Existing 5-Input Majority Gates

In addition to the 3-input gate, many researchers have implemented the digital circuits using a 5-input majority gate. The purpose of designing digital circuits using such gate is to reduce area, and latency, faster speed of operation than the traditional ones [16]. The functionality of the gate is based upon the Boolean expression in Eq. (2)

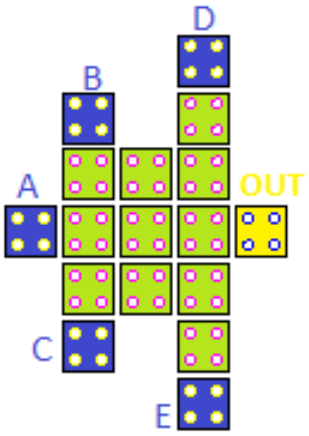
$$\mathrm{MG(A,B,C,D,E)} = \mathrm{ABC} + \mathrm{ABD} + \mathrm{ABE} + \mathrm{ACD} + \mathrm{ACE} + \mathrm{ADE} + \mathrm{BCD} + \mathrm{BCE} + \mathrm{BDE} + \mathrm{CDE}. \quad (2)$$

Important majority gates exist in the literature are described in this section. The majority gate design [17] is utilizing 10 QCA cells and occupying an area of $0.01\mu m^2$ having a drawback that its output QCA cell is trapped by the input cells, hence it is not possible to connect its output cell in a single layer. The majority gate design [18] is also utilizing 10 QCA cells having an area of $0.01\mu m^2$ with a drawback that the input cells are positioned too near to each other which causes interference of QCA cells with each other. The designs in [19-20] tried to overcome the previous drawbacks but at the cost of the enlarged area from $0.01\mu m^2$ to $0.02\mu m^2$. The designs in [21-22] consums more area as compared to the proposed design. The majority gate design in [23] has an area of $0.01\mu m^2$but with a drawback that the input QCA cell 'A' has a double effect due to two neighboring cells due to which, it may produce incorrect output. The majority design in [24] with an area of $0.01\mu m^2$ has a drawback that the structure is nonsymmetrical and the input cells are positioned very close to each other which causes interference between the cells. The majority design in [25] is also having an area of $0.01\mu m^2$ but with rotated input and output cells. This design also has a disadvantage of reduced efficiency and high fabrication cost due to the presence of two types of QCA cells. The majority design in [26] also has an interference problem because the input QCA cells cannot be extended further for implementing other circuits.

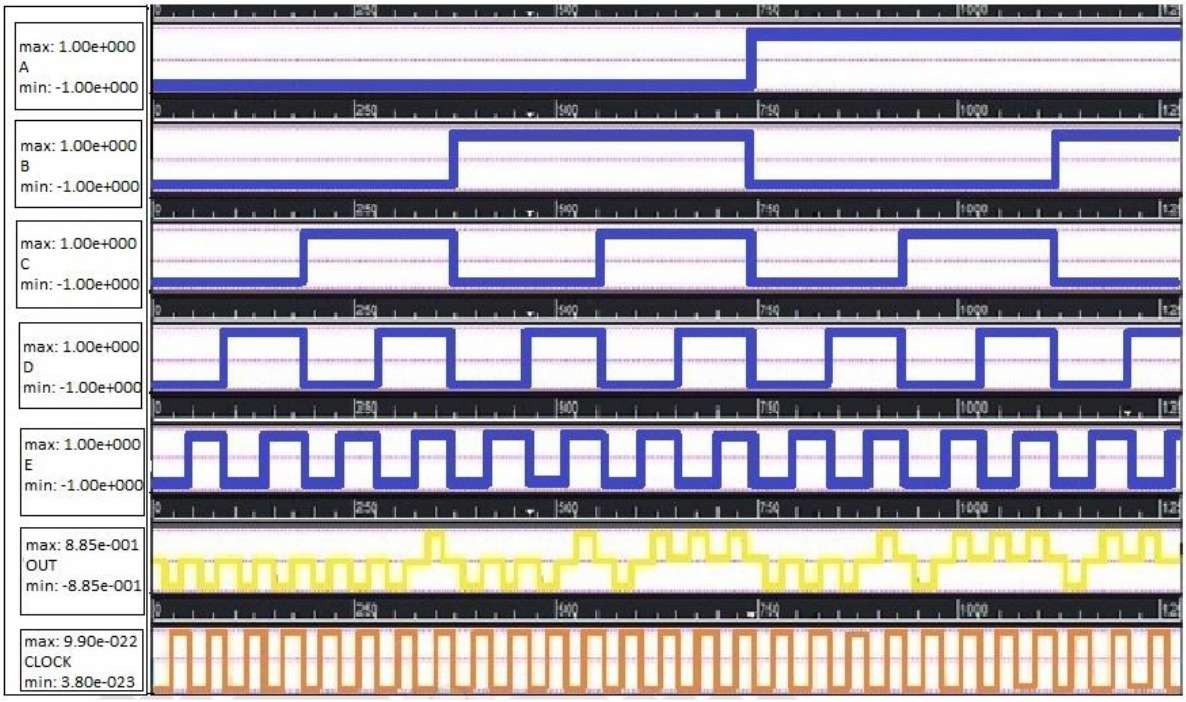
3.2. Design of Proposed 5-Input Majority Gate (PMG)

The majority Gate is designed using 17 QCA cells having an occupational area of $0.01\ \mu m^2$ is shown in Figure 4(a). It is clearly visible from the figure that its output can further be connected with any QCA logic design on the same layer, which means that one can connect as many QCA cells as desired with the output QCA cell without using another layer. Hence design can be utilized for both single as well as multilayer structures. Moreover, its configuration is robust due to the absence of rotated QCA cells, which further

reduces its implementation cost. It also has less power dissipation due to lesser occupational area. Figure 4(b) shows the simulated waveform for the PMG.



(a)



(b)

Figure 4. *The Proposed Majority Gate Design (a) QCA Structure (b) Simulation Output*

The majority gates in [17-18, 22, and 26] have the problem of unreachability of output cell and Input cells in a single layer. So these designs can be used only for multilayer structure. The designs in [19-21], this problem is overcome but it has increased QCA cells and the occupational area causing more power dissipation. However, the majority gates in [23-25] have overcome previous disadvantages with the reduced area but at the cost of more interference and high implementation cost. Therefore, it can be concluded from the above that in spite of all the efforts made, the solutions previously present and known in the prior art do not meet all the essential requirements [26] which have to be taken into consideration while designing a new majority gate. The structural analysis of PMG with the existing designs is compared in Table 1. Various parameters considered for comparison are an area, interference, and a total number of QCA cells. It is illustrated that the PMG structure occupies an area of 0.01 μm^2 which is 50 % less than the design reported

in literature. The designs presented in [27-28] presents majority gate based memory cell, which are discussed in section 4.

Table 1. *Comparison of the designed gate with the prior structures*

QCA Layout Design	Total QCA cells	Area (μm^2)	Interference	Single Layer Structure	Multi-Layer Structure
[17]	10	0.01	Yes	No	Yes
[18]	10	0.01	Yes	No	Yes
[19]	20	0.02	Yes	Yes	Yes
[20]	22	0.02	No	Yes	Yes
[21]	42	0.034	No	Yes	Yes
[22]	51	0.038	No	No	Yes
Proposed	17	0.01	No	Yes	Yes

3.3. Energy Dissipation Analysis of Proposed Majority Gate

Low power dissipation, even below traditional *KT*, is one of the main features of QCA nanotechnology. QCAPro is one of the accurate power estimation tools, which uses a non-adiabatic power dissipation model [29] to measure the switching power loss. The basic concept of this model is taken from the quasi-adiabatic model [30]. According to this model, the expectation energy value of the cell for every clock cycle is described as:

$$E = \frac{\hbar}{2}.\vec{\Gamma}.\vec{\lambda}, \tag{3}$$

Where, $\vec{\lambda} = \text{coherence vector}$,

$\vec{\Gamma} = 3\text{D energy vector}$.

Now, QCA cell power at any instant is:

$$P_{total} = \frac{dE}{dt} = \frac{d}{dt}\left[\frac{\hbar}{2}.\vec{\Gamma}.\vec{\lambda}\right] = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}\right] + \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\right] = P_1 + P_2. \tag{4}$$

The first term i.e. $P_1 = \frac{\hbar}{2}\left[\frac{d\vec{\Gamma}}{dt}.\vec{\lambda}\right]$indicates two components, first term is the transfer of power generated from clock to QCA cell and the second is power gain difference due to input and output power.

The second term $P_2 = \frac{\hbar}{2}\left[\vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\right]$indicates instantaneous power dissipation.

The energy dissipated by a cell in a single clock is calculated as:

$$E_{diss} = \int_{-T}^{T} P_2\, dt = \frac{\hbar}{2}\int_{-T}^{T} \vec{\Gamma}.\frac{d\vec{\lambda}}{dt}\, dt. \tag{5}$$

The value of energy dissipation is maximum for the maximum changing rate of $\vec{\Gamma}$.So the upper bound power dissipation is given by:

$$P_{diss} = \frac{E_{diss}}{T_{cc}}\langle\frac{\hbar}{2T_{cc}}\vec{\Gamma}_+ \times \left[-\frac{\vec{\Gamma}_+}{|\vec{\Gamma}_+|}\tan h\left(\frac{\hbar|\vec{\Gamma}_+|}{k_B T}\right) + \frac{\vec{\Gamma}_-}{|\vec{\Gamma}_-|}\tan h\left(\frac{\hbar|\vec{\Gamma}_-|}{k_B T}\right)\right]\rangle. \tag{6}$$

Here, k_B represents Boltzmann Constant, T represents temperature. The author of [31] has presented a power dissipation model. Here the leakage power is due to the loss for clock transitions at the leading edge or trailing edge of the pulse and switching power loss is due to the switching state of the cell. The sum of

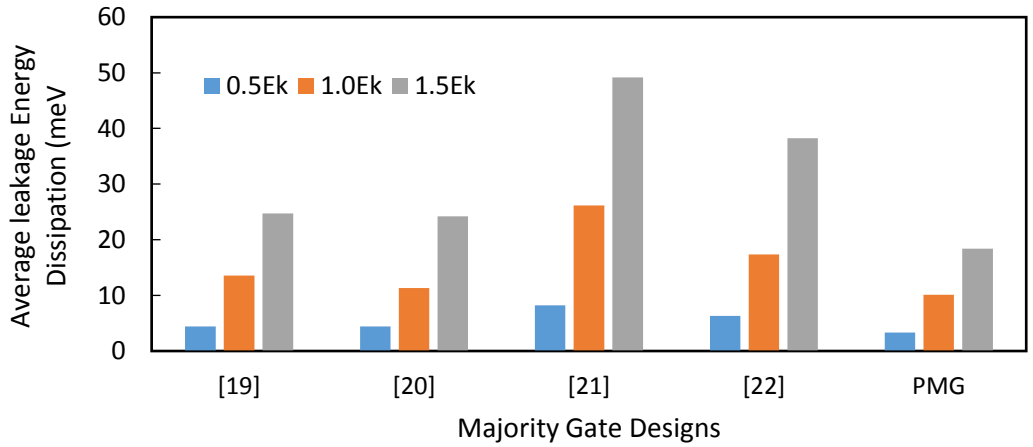
both the powers represents total power. All the above mentioned powers are estimated using a tool called QCAPro, which estimates average power dissipation of the circuit.

The switching, leakage, and total energy dissipation are calculated for the given tunneling energies i.e. $0.5E_k$, $1.0E_k$, and $1.5E_k$. Table 2 shows the comparison of the switching, leakage, and total energy dissipation for PMG and existing gates [17-22]. From table 2, it is clear that all three energy dissipations for the PMG are lesser than the gates in [19-22]. It can also be seen that the energy dissipation of [17-18] is less as compared to invented PMG because [17] and [18] are having a less occupational area but they cannot be implemented for single-layer structures, which is a drawback.

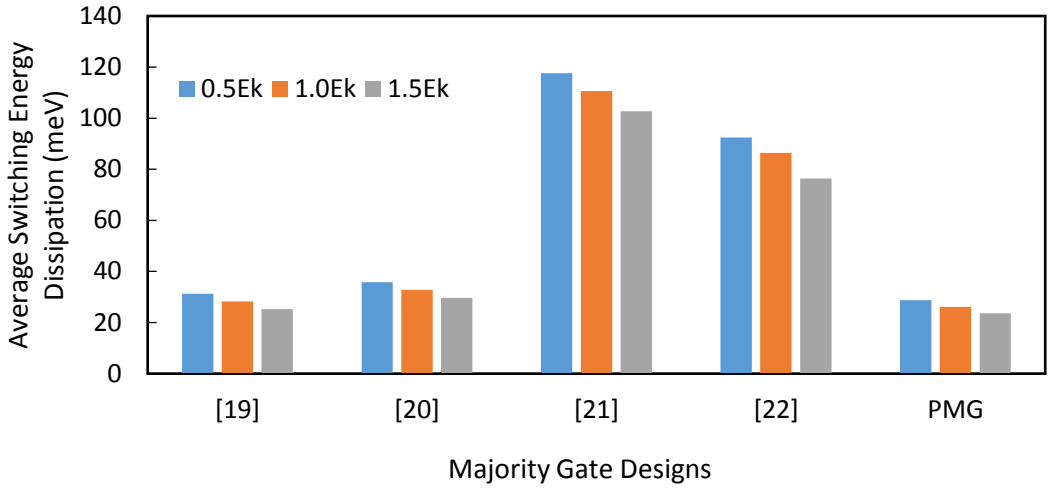
Table 2. *Energy dissipation analysis of proposed gate and previous designs*

5 input Majority Gate	Average leakage Energy Dissipation (meV)			Average Switching Energy Dissipation (meV)			Average Energy Dissipation of the circuit (meV)		
design	$0.5E_k$	$1.0E_k$	$1.5E_k$	$0.5E_k$	$1.0E_k$	$1.5E_k$	$0.5E_k$	$1.0E_k$	$1.5E_k$
[17]	1.28	4.14	7.69	11.53	10.37	9.16	12.81	14.51	16.85
[18]	1.35	4.25	7.8	10.94	9.84	8.7	12.29	14.09	16.5
[19]	4.41	13.55	24.73	31.24	28.31	25.21	35.66	41.85	49.94
[20]	4.4	11.33	24.2	35.78	32.8	29.64	40.18	44.13	53.84
[21]	8.2	26.14	49.15	117.57	110.66	102.67	125.77	136.8	151.82
[22]	6.33	17.34	38.22	92.44	86.45	76.44	98.77	103.79	114.66
PMG	**3.32**	**10.14**	**18.4**	**28.74**	**26.19**	**23.57**	**32.06**	**36.33**	**41.97**

The leakage, switching, and total energy dissipated by the designed gate are compared with the majority gate structures in [19-22] and their results are presented in Figure 5(a), 5(b), and 5(c). The energy dissipation results of the designed gate are not compared with [17] and [18] due to the aforementioned reasons. From the figure 5, it is concluded that the proposed majority gate design dissipates 10.5% less leakage energy, 20.15% less switching energy, and 17.67% less total energy dissipation than the best design conferred in [20] for the single layer as well as multi-layer design.



(a)



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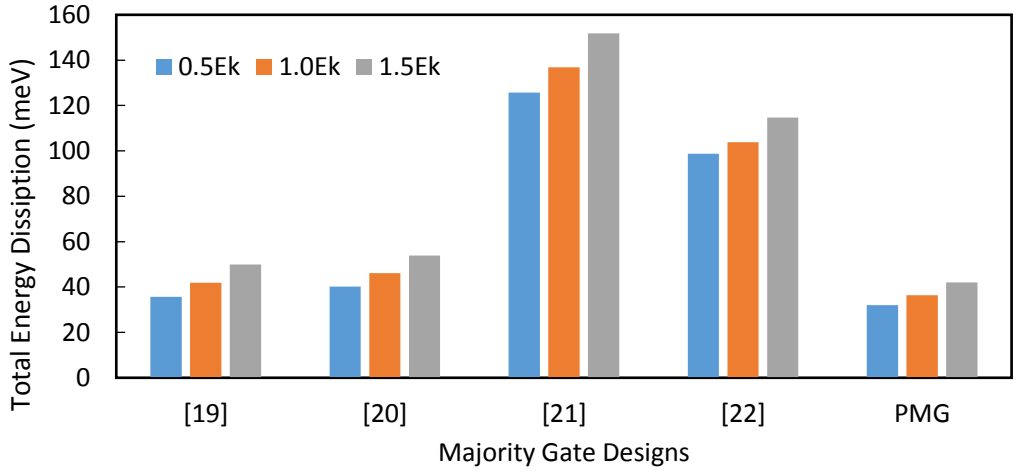
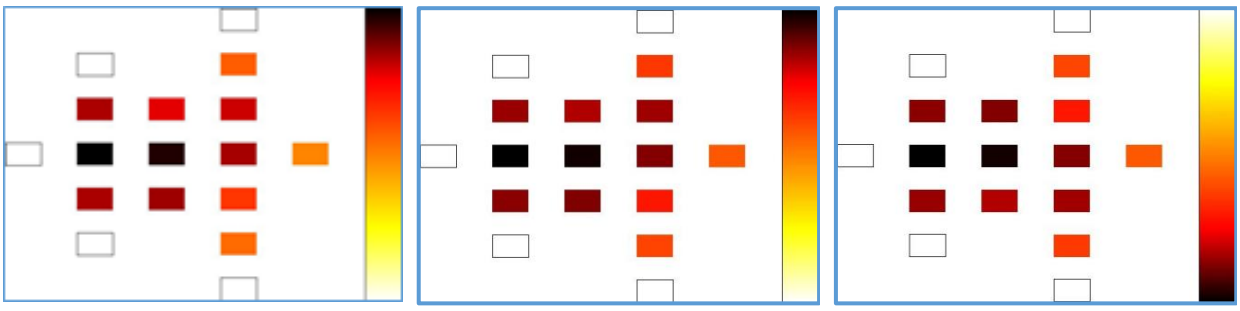


(c)

Figure 5. *(a) Leakage Energy Dissipation (b) Switching Energy Dissipation and (c) Total Energy Dissipation of Proposed Gate and Prior Designs at three tunneling energies 0.5 E_k, 1.0 E_k, and 1.5 E_k*

Figure 6 (a), (b), and (c) shows the thermal layout of proposed majority gate at *0.5 E_k, 1.0 E_k, and 1.5 E_k.* Here the dark-colored QCA cells represent more power dissipation as compared to the light-colored QCA cells.



(a) (b) (c)

Figure 6. *Thermal Layout of PMG at three different tunneling energy (a) 0.5E_k (b) 1.0E_k (c) 1.5E_k*

4. RAM CELL STRUCTURE

Design of a RAM cell is the most prominent paradigm for improving read/write latency, area, and energy dissipation at the nanoscale level. QCA based RAM cell design is classified as a line based [32-33], and loop-based [34]. In a line based designs, QCA based line is utilized to save the previous bit [35-36]. In a loop-based structure, the storing mechanism can be achieved by utilizing a feedback loop containing four clocking zones [37-38].

4.1. Review of Existing RAM Cell Designs

In this section, the details of existing RAM cell structures are reviewed. The primary RAM cell in QCA design presented in [28] utilizes D latch to store a data bit with loop-based architecture, occupying an area of 0.16 $\mu m^2$with 158 QCA cells with a delay of 2 clock cycles is presented in Figure 7. The main flaw of this design is lacking SET/RESET capability, higher occupational area, and high latency. Moreover, it has a coplanar wire crossing structure, which makes it a more complex design for fabrication. The RAM cell presented in [27] utilizes two multiplexers of type 2:1 where one of the multiplexers acts as a D Latch with SET/RESET capability. The latency of this RAM cell is 1.75 clock cycles occupying an area of 0.13 μm^2 with 109 QCA cells. The working of this design becomes more complex due to the presence of two multiplexers. The design in [25] has a lesser area of about 0.06 μm^2 and delay of 1.25 clock

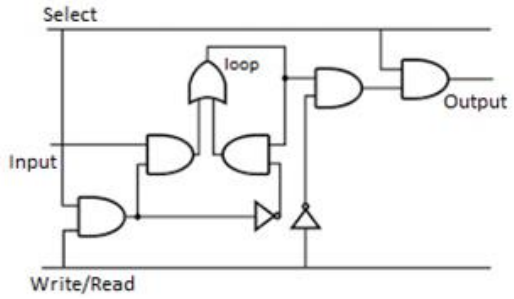
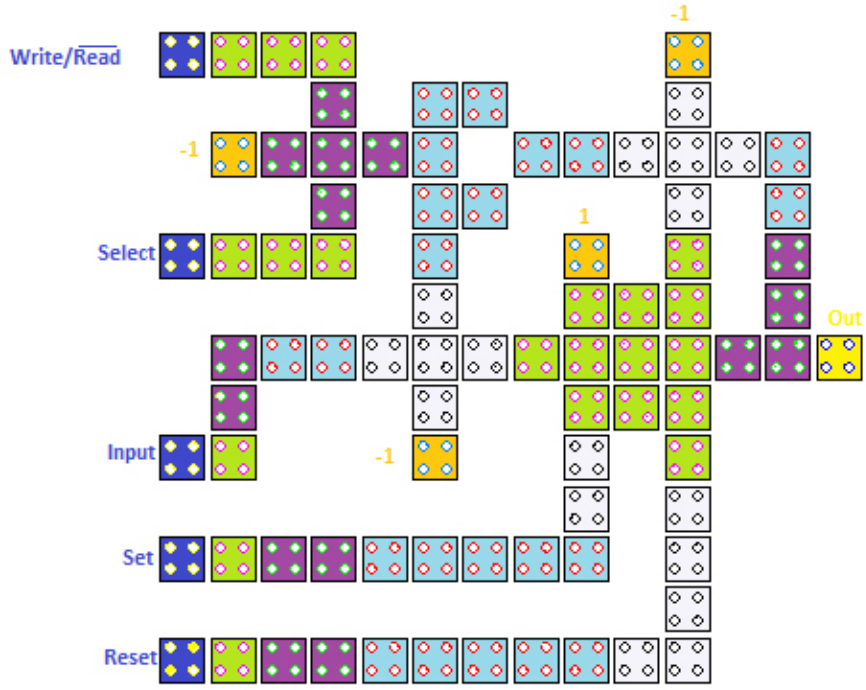


Figure 7. *The Schematic of a Basic RAM Cell [20]*

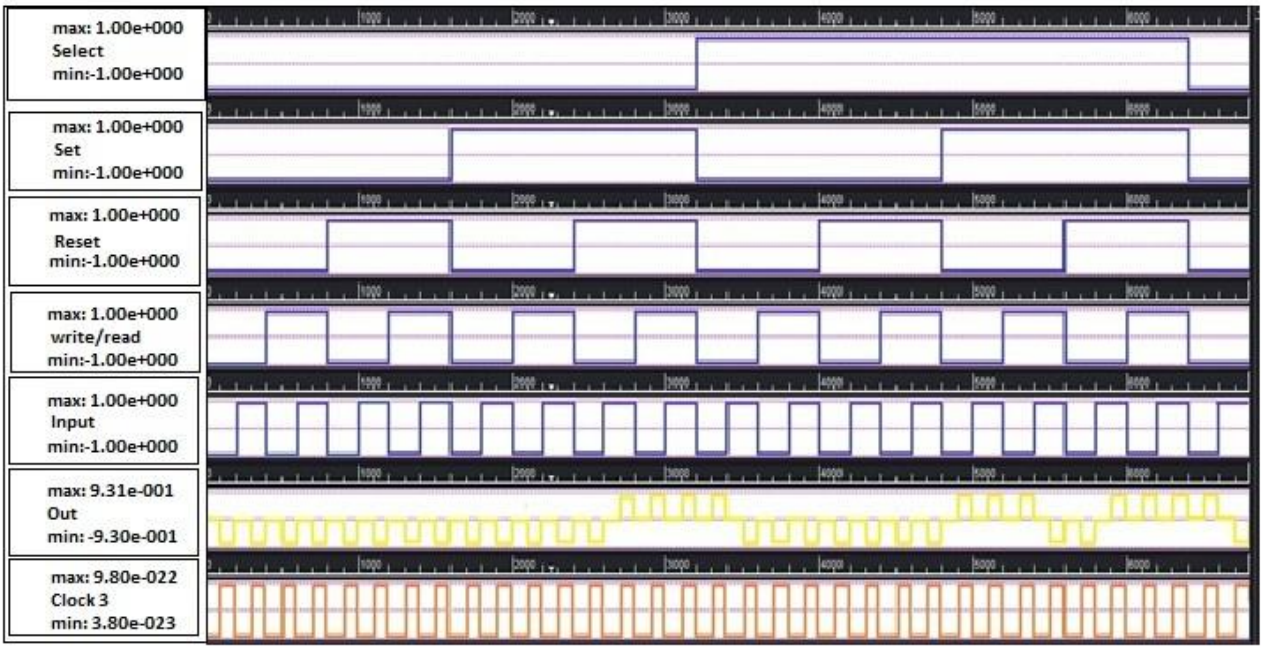
cycles but it has a major drawback of reduced robustness, complex fabrication process and high noise variations due to the presence of two types of QCA cells i.e. rotated and un-rotated cells. The author in [20] utilizes a D latch and SET/RESET capability having an occupational area of 0.08μm^2, 88 QCA cells and a total delay of 1.5 clock cycles. The latency of designed RAM cell is 1.25 clock cycles occupying an area of 0.07 μm^2 with 85 QCA cells, which is better than the designs in [20], [27] and [28]. However, the design presented in [25] utilizes the lesser area of about 0.06 μm^2 but has a disadvantage of reduced tenacity, high implementation cost, and higher noise variations due to the presence of two different styles of QCA cells i.e. rotated and un-rotated style. Whereas the RAM cell structure presented in this paper is utilizing one type of QCA cell. Hence the proposed design outperforms the design best reported design. The disclosed RAM cell design is using only one type of QCA cell overcoming the drawback of design in [25] also.

4.2. Design of Proposed RAM Cell Structure

The new RAM cell structure is designed using invented five input majority gate as discussed in section 3.2. The RAM cell design is utilizing 85 QCA cells with an occupational area of 0.07 μm^2, the power dissipation of 211.1 meV and a total delay of 1.25 clock cycles. The structure contains three AND gates and one 5-input PMG. It is cost-effective due to its reduced size, which duly qualifies the industrial application criteria for data storage purposes. It is a novel Coplanar RAM cell structure with the reduced area, cell count, power dissipation, and input to output delay. Besides that, the present design has the Set/Reset capability and the problem of unreachability of output cell and input cells in a single layer structure has also been resolved. Hence the QCA structure can be used for both single and multilayer architecture. The structure of the designed RAM cell is shown in Figure 8(a). It has two control pins named as ‘Set’ and ‘Reset’.



(a)



(b)

Figure 8. *The Proposed RAM Cell (a) QCA Structure (b) Simulation Result*

Its functionality is explained using Table 3. Here for reading and write mode of operation, 'Set' pin is kept at logic "0" and 'Reset' pin at logic "1". For 'write' operation, both 'select' pin and 'write/read' pin will be at logic "1", as a result, input bit is transmitted at the output. For "read" operation, 'select' pin will be at logic "1" and 'write/read' pin at logic "0" respectively. To operate the RAM cell in Set mode of operation, the 'Set' pin should be kept at logic "1" whereas for reset mode 'Reset' pin should be kept at logic "0". The RAM cell is designed and simulated using QCADesigner tool. Its simulated results are shown in Figure 8(b) matches according to the values given in table 3.

Table 3. *Working of Proposed RAM Cell*

Mode of Operation	Set Pin	Reset Pin	Select Pin	Write/Read Pin	Input Pin	Previous value	Out Pin
Write Mode	0	1	1	1	1	x	1
					0	x	0
Read Mode	0	1	1	0	x	0	0
					x	1	1
Set Mode	1	1	x	x	x	x	1
Reset Mode	0	0	x	x	x	x	0

Table 4. *Comparison of Proposed RAM Cell with Existing Designs*

RAM Cell	Set/Reset ability	Coplanar	Cell Count	Area(μm^2)	Gate Count	Latency (clocking cycles)
[20]	Yes	Yes	88	0.08	5	1.5
[27]	Yes	Yes	109	0.13	8	1.75
[28]	No	No	158	0.16	8	2
Proposed	**Yes**	**Yes**	**85**	**0.07**	**5**	**1.25**

The structural analysis of designed RAM cell with the existing ones is compared in Table 4. However, the RAM cell structure in [25] is not compared in Table 4 because of its reduced robustness and high fabrication cost. Various parameters considered for comparison are occupation area, gate count, total delay, and total QCA cells. It is illustrated that the presented structure occupies an area of 0.07 μm^2, which is 12.5 % less, and latency of 0.07 μm^2, which is 16.6% less than the best design reported in literature.

4.3. Energy Dissipation Analysis of Proposed RAM Cell

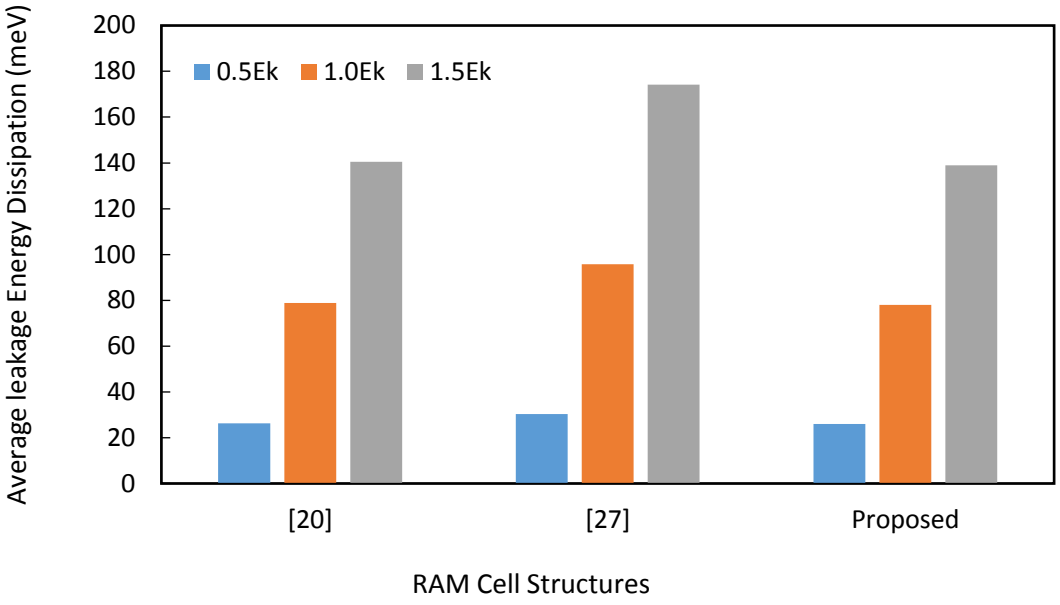
Energy dissipation in QCA is one of the main features in recent years, as it results in very low energy computation [39]. The presented RAM cell structure outperforms the previous designs with 85 QCA cells, the occupational area of 0.07μm^2, gate count of 5, and a total delay of 1.25 clock cycle. Its energy dissipation analysis results are shown in Table 5. The presented RAM cell dissipates 126.7 meV energy at $0.5E_k$ tunneling energy, 164.2 meV energy at 1.0 E_k tunneling energy, and 211.1 meV energy at $1.5E_k$ tunneling energy. It achieves 18.2 % less total energy dissipation, 12.5 % lower area, and 16.6 % lower input to output delay than the best-reported designs.

Table 5. *Energy dissipation analysis of Proposed RAM Cell Structure with Existing Designs*

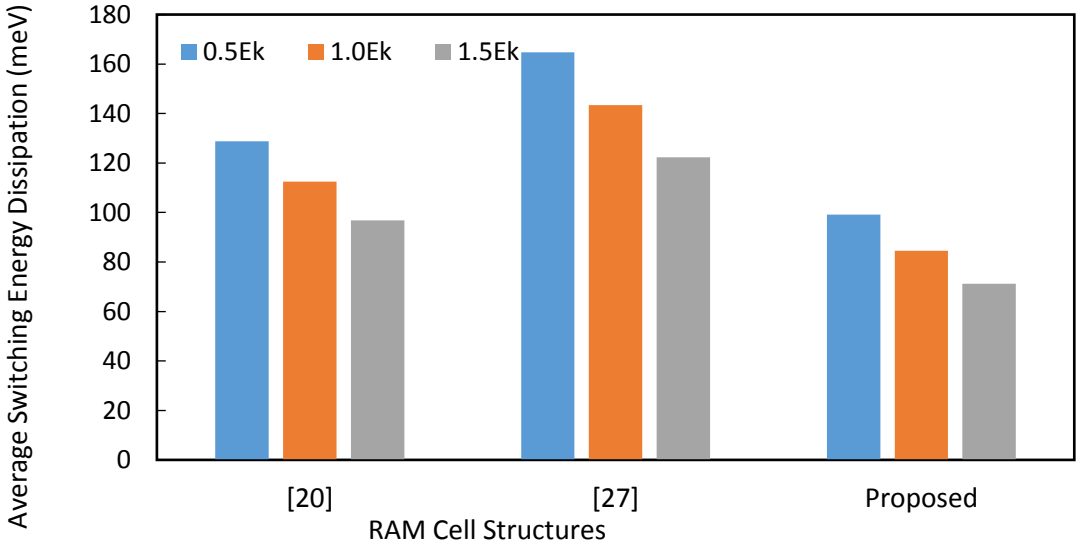
RAM cell Structure	**Average leakage Energy Dissipation (meV)**			**Average Switching Energy Dissipation (meV)**			**Average Energy Dissipation of the circuit (meV)**		
Design	$0.5E_k$	$1.0E_k$	$1.5E_k$	$0.5E_k$	$1.0E_k$	$1.5E_k$	$0.5E_k$	$1.0E_k$	$1.5E_k$
[20]	26.3	79.0	140.48	128.78	112.44	96.80	155.01	191.27	237.28
[27]	30.39	95.78	174.25	164.69	143.33	122.26	195.08	239.11	296.51
Proposed	**26.1**	**78.7**	**139.8**	**99.2**	**84.5**	**71.2**	**126.7**	**164.2**	**211.1**

Figure 9 shows the graph that compares the Average leakage, Switching, and total energy dissipation of newly designed RAM cell with design in [20] and [27]. From the graph shown in Figure 9(a), (b) and (c), it is clear that the average energy dissipation of new RAM cell at $0.5E_k$ is 126.7 meV, which is 18.26 % less, at $1.0E_k$ is 164.2 meV, which is 14.15 % less, at $1.5E_k$ is 211.1 meV, which is 11.03 % less than the best-reported design [20]. The thermal layout of the RAM cell is presented in Figure 10 (a), (b) and (c).

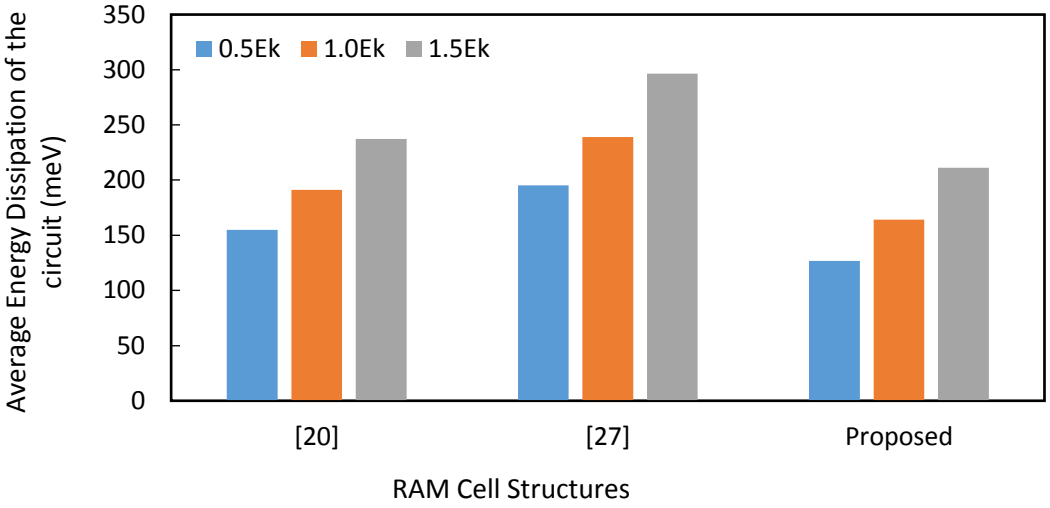
The dark-colored cells represent that they dissipate more energy as compared to the light-colored QCA cells at $0.5E_k$, $1.0E_k$, and $1.5E_k$ of tunneling energy.



(a)

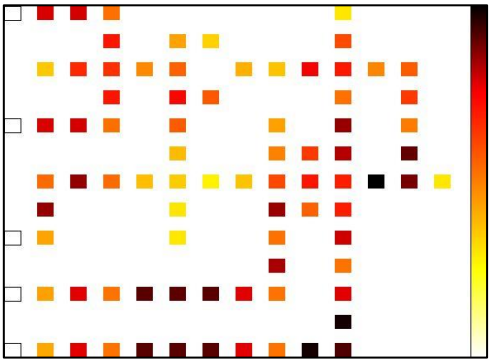


(b)

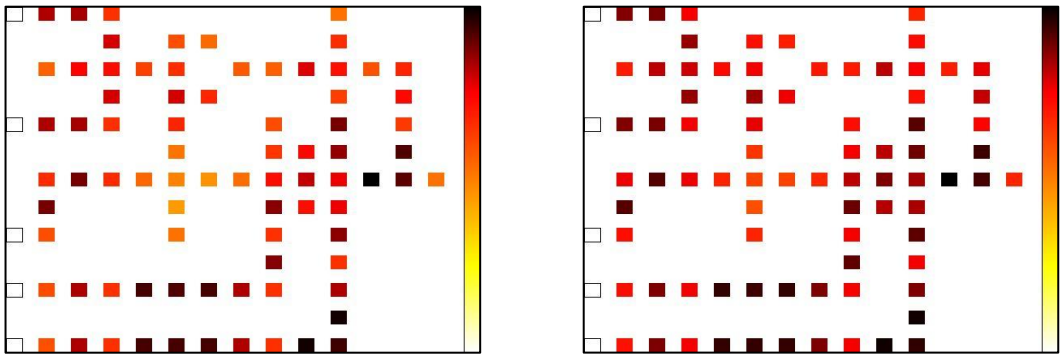


(c)

Figure 9. *The (a) Leakage Energy Dissipation (b) Switching Energy Dissipation and (c) Total Energy Dissipation of Proposed RAM Cell design and Existing Majority Designs*



(a)



(b) (c)

Figure 10. *Energy dissipation Thermal Maps of Proposed RAM cell structure at three different tunneling energies of (a) 0.5E_k, (b) 1.0E_k, (c) 1.5E_k*

4.4. Cost Function of Proposed RAM Cell Structure

The Cost Function values of RAM cell structures have been proposed in Figure 11. The cost function [40] for existing and proposed RAM cell structures have calculated using the below-mentioned formula:

$$Cost_{QCA} = \left(M^k + I + C^l\right) X\, T^p, 1 \leq k, l, p \tag{7}$$

Here, *M*, *I*, and *C* represent the count of majority gates, inverters, and cross-overs. The term *T* presents delay and k, l, and p represents exponential weights respectively. From the results in Fig 11, the RAM cell presented in [28] has the highest cost function value, which means the design is complex with poor performance. The proposed design has the lowest cost function in comparison to the designs presented in the literature. Which means that the new RAM cell has excellent performance capability in terms of gate count, cell count, number of wire crossings, and input to output delay.

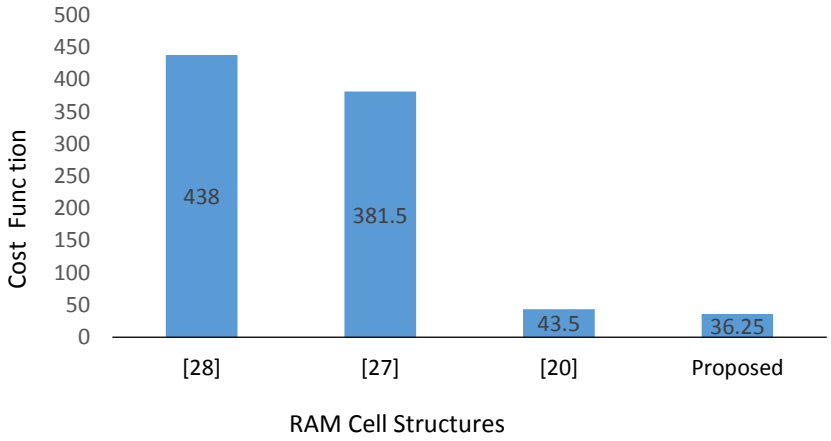


Figure 11. *Cost Function Comparison of Proposed RAM cell with Existing Designs*

5. CONCLUSION

The present invention discloses high-performance RAM cell design using invented majority gate. The PMG gate is designed with an optimized number of QCA cells, which is helpful in reducing the overall size of the design and thereby reducing the power dissipation. The disclosed design of PMG gate has the advantage of reachability of output cell and Input cells in a single layer. So these designs can be used for multilayer structure as well as for single-layered structure. The technical advancement of the paper lies in designing a high-performance RAM cell circuit by using the invented PMG gate with less QCA cells and optimization in the area, delay, and power dissipation characteristics. The disclosed RAM cell structure achieves 18.26 % lower total energy dissipation, 12.5 % lower area, and 16.6 % lower input to output delay than the best-reported designs. Besides that, it has the Set/Reset capability and has the advancement that problem of unreachability of output cell and input cells in a single layer structure has been solved. The RAM cell design is robust due to lesser noise variations with decreased fabrication cost. Re-configurability with Quantum Dot Cellular Automata will add a new dimension to designing of RAM cell circuits as the area and power will be reduced considerably. Hence it could pave for smaller and power-efficient circuit designs in the future.

CONFLICTS OF INTEREST

No conflict of interest was declared by the authors.

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