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Technical Note

Electrostatic discharge risks in electronics used in automotive application

^{1*}Tamilarasu.S, ²P.Thirunavukkarasu, ³N.Sethupathi

¹ Research Scholar, Bharathiar University, Coimbatore, India

² Dept of Electronics, SRMV College, Coimbatore, India

³ Dept of Physics, A.A.Govt Arts College, Namakkal, India.

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Abstract

The automotive industry pays special attention to knowledge-based specification, design, manufacturing and qualification of components and other integrated circuits (ICs). As a result, there is the demand for ICs to be fit-for-application rather than any consideration of fit-for-standard. Thus when the ESD specs are stated, the rationale for the requirements needs to be understood. Therefore, we first need to consider if the ESD requirements for the automotive environment are any different from other consumer product environment requirements. Additionally, automotive product markets often demand “Zero PPM (Parts Per Million)” for overall IC product reliability that includes ESD.

Key words: ESD Risks, ESD in Automotive, ESD Safer System, Optimizing for ESD performance

* Corresponding author

E-mail address: kongutamil@rediffmail.com

1. Introduction

Today many automotive applications comes with lot of features including, car entertainment, automotive networking, automotive immobilizers and keyless entry & start and etc. Many of those are not different from non-automotive, especially with respect to ESD (Electrostatic Discharge). Once installed into the system, the component is not threatened anymore. Therefore regular ESD requirements should hold for these components. In the automotive world, product pins directly interfacing with the outside world (battery monitors, airbag sensors) may see another type of ESD threat. This is the so-called system level ESD. The test procedures are based on the three primary models of ESD events: Human Body Model (HBM), Machine Model (MM) and Charged Device Model (CDM). The models used to perform component testing cannot replicate the full spectrum of all possible ESD events.

2. ESD Risks

ESD damage is directly responsible for approximately 10% of the total failure returns, and the reported number may be higher but for the difficulty in distinguishing between some EOS (Electrical Over Stress) and ESD failures. And in the new millennium, these issues continue to make it an important failure mechanism throughout the automotive electronics industry. As technology feature sizes move into the deep submicron regime, concerns regarding ESD are increasing. There is strong motivation, therefore, to ensure that the present and future automotive electronics have reasonable ESD levels to avoid damage during handling and testing. Another issue, which gives increasing importance to ESD, is the move towards replaceable circuits in automotive electronic systems. Instead of replacing the whole circuit board, as used to be standard practice, users are encouraged to purchase upgrades to their microprocessors and memory cards and do the installation themselves.

3. ESD Strain in Automotive Electronics

In most qualification procedures for ESD performance, the chips are usually stressed at a single ESD voltage level given by the specification and if it passes this test it is considered to have qualified. For example, if the chip passes a stress level of 4 kV (according to the Human Body Model), it is assumed to pass 2 kV also. On the other hand, if it fails a stress level of 2 kV, it is assumed that it will not pass 4 kV. It will be shown here that this may not necessarily be the case if there are interactions with internal parasitic devices.

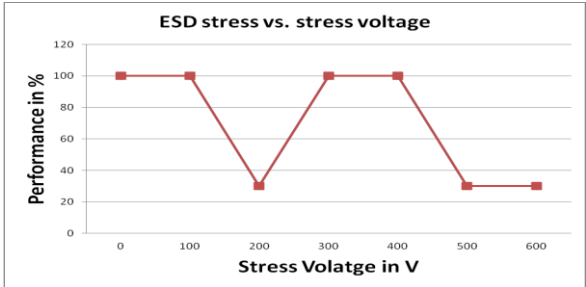


Fig 1 Device performance post-ESD stress vs. stress voltage (MM)

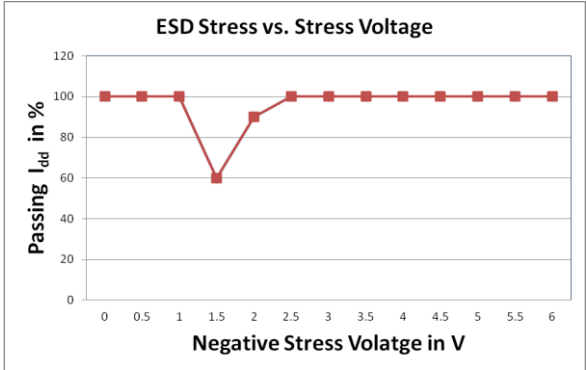


Fig 2 Devices passing Idd leakage test post-ESD stress vs. stress voltage.

In Figure 1 the overall ESD performance of a chip used in automotive application is shown as a function of ESD stress level. And the results shown in Figure 2 are for the Human Body Model stress (applied stress was negative with respect to Vdd performance). These devices were stressed according to the Machine Model with all pins positive to Vss and negative to Vdd. On the y-axis the percentage number of devices passing full functional test after ESD stress are shown and the x-axis gives the applied

ESD stress level. There is clearly a window where the ESD performance of this device is weak. In this particular case, the failing devices are found to have a drastic increase in the V_{dd} to V_{ss} current, I_{dd} , after ESD stress. A more thorough investigation led to the conclusion that the I_{dd} current increase in the failed devices occurred only when the stress applied was negative with respect to V_{dd} .

4. ESD Safer System

The present ESD protection used in automotive circuits elements for MOS processes are the nMOS devices designed as various types of efficient protection clamps, and PMOS devices used as high current MOS conduction devices. The bipolar *npn* devices are used for bipolar/BiCMOS processes. The use of SCR (Silicon Controlled Rectifier) structures has initially increased because of their lower power dissipation after they trigger, but the high trigger voltages have limited their application.

Reducing the trigger voltages for both SCR as well as *npn* devices has been a major thrust in the development of ESD protection circuits with reasonable success. During the introduction of thin epi substrates and again with the introduction of shallow junction isolation, the SCRs have been absent for a while because of the difficulty in achieving their consistent trigger for protection designs. But more recently the SCRs are beginning to make a serious comeback, the most common reason being the low associated capacitance with reasonable ESD levels.

5. Other Options

The high chip capacitance in large ICs used in automotive circuits has increased the effectiveness of the diode protection circuit, which was popular in the early technologies. A diode between the pad and the positive power supply (V_{CC}) is usually supplemented by either an *npn* device or an SCR to the ground (V_{SS}) or negative

supply. Diode circuits also require good protection between V_{CC} and ground, which can be an *npn* type circuit or an SCR depending on the application.

Large ICs have a large number of pin combinations, and consideration must be given to each of these when placing ESD protection circuits. In addition, in many cases multiple V_{CC} and V_{SS} buses may be used, which lead to added complications in terms of protection circuitry. In general, ESD protection circuits are placed between all the important combinations. This requirement makes the use of diode elements attractive because of their small areas. The diodes also offer minimum capacitance ESD protection, which makes it attractive for RF circuit applications. As mentioned, the effect of technology on ESD protection circuit performance has been a major hindrance to achieving consistent ESD behavior. Advanced process development has begun to include ESD considerations in the technology roadmap. In some cases, process features have been implemented just to ensure consistent ESD performance.

6. Optimizing for ESD performance

It is critical to realize that most process improvements that improve ESD will adversely affect other important reliability parameters. The most significant trade-off is the effect on hot carriers. Since the ESD performance is degraded by the presence of the lightly doped devices (LDD) while hot carrier is improved by it, there is clearly an optimum point that needs to be found where ESD performance and hot carriers are both acceptable. Similarly, ESD performance is improved with thicker epitaxial layers and more resistive substrates. However, latch up robustness is reduced by the same parameters. Again, it is essential to find an acceptable point for both ESD and latch up robustness in choice of epitaxial thickness, well doping, and substrate doping.

A properly designed protection circuit should ensure that gate oxide breakdown

does not take place, but during the ESD strike the voltage across the gate oxide will be higher than in typical operation. There is concern that in very thin gate oxides, the stress induced leakage current at elevated gate oxide voltage levels can cause degradation in the oxide reliability after the ESD event. Interconnect reliability is also affected by ESD, and a reduction in electro migration robustness is possible if the metal melts during ESD stress. The quenching effect of the melting and cooling will change the grain properties of the interconnect and make it more sensitive to electro migration. It is important to ensure that these limits are understood and taken into account during process development and protection circuit design as per automotive standards. While the process must be optimized for ESD, it is not possible to maximize the process for ESD.

7. Conclusion

The present approach to ESD protection circuit design and implementation is iterative in automotive electronics. Circuits are designed and evaluated depending on the available area and the pin specifications. In many cases the ESD capability of the process has been previously characterized on test structures to enable basic design guidelines for the protection circuits to be generated. However, in many cases the iterative approach involves too much time and can result in a delay in the release of a product to the market. Since a delay could be costly, the outcome is that ESD protection circuit performance may be sacrificed.

There is a need, therefore, to reduce the number of cycles required for the development of good ESD protection circuits. An important contribution in this direction would be the ability to use accurate simulation tools to evaluate the circuit and the technology. Present generations of automotive ICs are almost entirely designed using simulations, and the

inability to include the ESD circuit into the simulation loop makes it more difficult to include ESD performance into the circuit design. The same is true for technology design. In recent years, there has been a significant thrust to use simulations for initial ESD designs. But even then, the lack of accurate simulation tools is one of the major reasons why ESD is considered to be almost a “black art” in the automotive electronics industry.

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