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Research Article

LOW-POWER DYNAMIC COMPARATOR WITH HIGH PRECISION FOR SAR ADC

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ABSTRACT
In this work, low-power dynamic comparator is presented with auto-zeroing technique for successive approximation register (SAR) analogue-to-digital converter (ADC). The comparator designed with DTMOS technique operates in sub-threshold region. The designed circuit consumes low power with high gain. The dynamic range of the comparator is increased with a new biasing technique for DTMOS transistors. The core design consumes 6.01µW power and overall design consumes 17.06µW. The design is realized with two different supply voltage with 600mV (core design) and 1.8V (biasing circuit). The comparator has been simulated with 0.18µm TSMC process in Cadence environment.

Keywords: *SAR ADC, Comparator, CMOS analog integrated circuits*

1. INTRODUCTION

Comparative circuits are indispensable interface elements between analog and digital world. Also, comparators play key roles in the design of analog-to-digital converters, memories, dynamic logic, and sense amplifiers as decision-making circuits (Cohen *et al*. 2005; Kim, Choi, and Lee 2015; Ming-Dou Ker and Jung-Sheng Chen 2008; Verma and Chandrakasan 2007). The input referred offset voltage in the design of comparator circuits is the biggest problem affecting the resolution of converters. Auto-zeroing and chopper methods are useful techniques to cancel offset and low-frequency noise (Cohen *et al*. 2005; Witte, Makinwa, and Huijsing 2006; Wu, Makinwa, and Huijsing 2009). Dynamic switches with auto-zeroing technique are the common and successful approach to cancel offset (Schinkel *et al*. 2007; Sepke *et al*. 2006).

Dynamic comparators are suitable for low-supply, low-power and high-speed applications (Zhong, Bermak, and Tsui 2017). Furthermore, various types of sensors to gather information are applied to everyday objects of Internet of Things (IoT). These sensor requirements oblige the need of analog-to-digital converters (ADCs) dissipated low power with high resolution and high linearity for use in an energy-constrained environment (Shim *et al*. 2018). Moreover, the power consumption of the dynamic comparators is called the dynamic power. The dynamic power is defined as the power of dissipated during the evaluation of signal in one period of clock. The successive approximation register (SAR) ADCs has the resolution of 12-14 bit level and are very energy-efficient (Yan *et al*. 2018).

Furthermore, in wide common mode range applications, for example, the speed and offset of CMOS designs in A / D converters depends on the common mode voltage of the input and this is a challenging situation for sub-micron CMOS technologies. However, a large voltage headroom, which is problematic, especially in circuits with transistor stacks and especially in low-voltage deep-micron CMOS technologies (Schinkel *et al*. 2007; Wicht, Nirschl, and Schmitt-Landsiedel 2004; Wong and Yang 2004).

In this work, offset cancelled low power dynamic comparator for successive approximation register (SAR) ADCs is designed. The CMOS implementation of the designed comparator is realized with standard 0.18μm CMOS technology with DTMOS technique. The designed circuit has mixed 0.6V-1.8V supply voltage. The biasing circuitries (current sources and current sinks) are designed with normal CMOS transistor to extend headroom. The core design is implemented with DTMOS transistors (Achigui *et al*. 2006; Ramírez-Angulo *et al*. 2001). DTMOS transistor is realized for only pMOS transistor by connecting its gate to the body without the need for another manufacturing process or step. As a result, the DTMOS transistors can be used in standard CMOS process. DTMOS offers the low power designs for especially biomedical applications and portable devices.

This paper is organized as follows. Section 2 explains the CMOS implementation and layout with analysis. Corner and Monte-Carlo analysis are also given in the same section. Finally, section 3 gives some conclusions.

2. COMPARATOR DESIGN

Due to the nature of analog signals, all IoT applications require both analog and digital system design for a high integration level with low cost. Although many analog designs can perform digitally, the analog-digital converters (ADCs) are still required as an interface between the analog domain and the digital (Lin, Wei, and Lee 2018). Many wireless sensor node (WSN) for IoT applications require low-power ADCs ranging in resolution (8 - 12 bit) and speed around (MS / s) (Ding *et al*. 2018). Comparators are the essential building block of the successive approximation register (SAR) ADCs. Comparators need extremely low offset, and very low input noise. The dynamic range of the comparator can be improved by cancelling the low-frequency noise and offset with auto-zeroing technique (Enz and Temes 1996).

Operational amplifiers have been used as basic circuit components in analog circuit design since the emergence of integrated circuits. After the emergence of new analog circuit applications, the performance characteristics of the voltage-mode operational amplifiers are not sufficient for analog signal processing requirements. The compensation capacitance, which ensures the stability of the OPAMP (operational amplifier), reduces the bandwidth of the operational amplifier due to the excessive voltage gain expected from OPAMP (Palmisano G. 1999). Therefore, OPAMPs are replaced by operational transconductance amplifiers (OTAs) whose output resistance is quite high (Maloberti 2006). At the same time, in a fully differential system not only rejects the common mode voltages but also eliminates the external noise. For the reasons mentioned above, the CMOS implementation of comparator is realized with fully differential operational transconductance amplifier in sub-threshold region.

Fig. 1 shows a block diagram of the comparator structure. The proposed implementation is developed based on the comparator proposed in (Allen and Holberg 2012). The structure of the comparator is made up of a fully differential operational transconductance amplifier, latch and switch. The gain of the overall design is 142.8dB. The overall design consists of three cells. Each cell has the gain of 35.7dB. The input referred offset is $V_{OS1} + V_{OS2} \,/\, A_{V1} + V_{OS3}/A_{V1}A_{V2}$. V_{OS1} and A_{V1} is the first cell's offset voltage and gain, respectively. V_{OS2} and A_{V1} define the second cell's offset voltage and gain while the third stage offset and gain is defined as V_{OS3} and A_{V3}, respectively.

OTAs and dynamic latch operate in sub-threshold region and the supply voltage is 0.6V. The biasing circuit operates with 1.8V supply voltage. pMOS transistor of core design are designed with DTMOS technique to decrease the power dissipation and to increase the gain and dynamic range of the design.

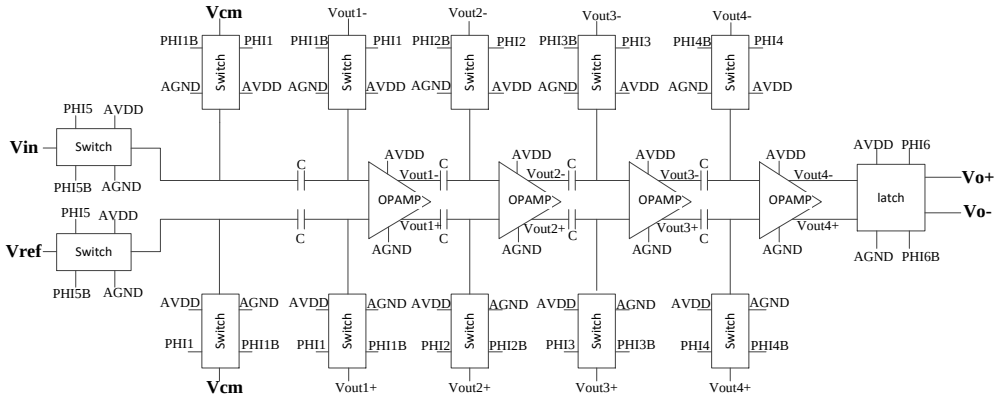

Fig. 1 Block diagram of the designed comparator

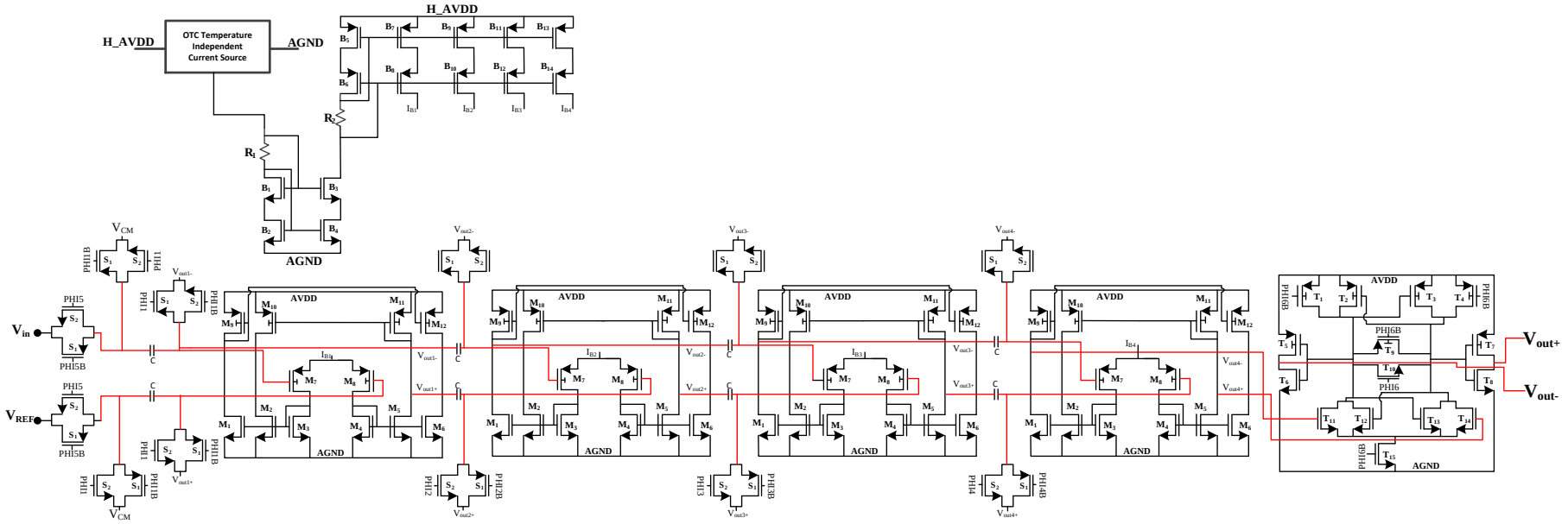

Fig. 2 CMOS implementation of overall comparator

(1) shows the transistor current in sub-threshold region. I_0 and m are technology dependent parameters, $V_T = kT/q$ is thermal voltage.

$$I = I_0 \frac{W}{L} e^{\frac{V_{GS}-V_{th}}{mV_T}} (1 - e^{-(V_{DS}/V_T)}) \quad (1)$$

The sub-threshold current-voltage relationship of the MOS transistor is very similar to the bipolar transistor, but still the gain effect of the threshold voltage is clearly visible as in (1). The threshold voltage of the transistor is decreased dynamically by connecting the device gate and body, seen as the relationship given in (2).

The DTMOS transistor under the same V_{GS} voltage has a higher g_m than the MOS transistor. (3) gives the relationship of g_m under sub-threshold region. As a result, DTMOS transistor has higher gain than the standards under same conditions.

Only pMOS transistors can be selected as DTMOS because of the single well process of used 0.18µm CMOS process. The biasing circuit is designed with standard CMOS transistor with 1.8V supply voltage to increase the swing and gain of amplifier. Table 1 gives the size of the transistors.

Table 1. The size of the transistors

		Transistors	***W/L***
Supply Voltage (1.8V)	**Biasing Transistors**	B_1, B_2, B_3, B_4, B_5, B_6, B_7	10µm/2µm
		B_8, B_9, B_{10}, B_{11}, B_{12}, B_{13}, B_{14}	10µm/2µm
Supply Voltage (0.6V)	**Switch**	S_1	100µm/180nm
		S_2	100µm/180nm
Operational Transconductance Amplifier	Supply Voltage (0.6V) DTMOS Technique	M_1, M_2	8µm/360nm
		M_3, M_4	4µm/360nm
		M_5, M_6	8µm/360nm
		M_7, M_8	10µm/360nm
		M_9, M_{10}, M_{11}, M_{12}	8µm/360nm
Latch		T_1, T_4	6µm/180nm
		T_2, T_3	1.3µm/180nm
		T_5, T_7	6.6µm/180nm
		T_6, T_8	6.6µm/180nm
		T_9	4µm/180nm
		T_{11}, T_{14}	3µm/180nm
		T_{12}, T_{13}	1µm/180nm

The CMOS implementation of the comparator is given in Fig. 2. The implementation of temperature independent current generator is designed based on (Alaybeyoğlu and Kuntman 2016). Layout of the comparator is given in Fig. 3. The core occupation area of the designed circuit is 61.5µmx115.4µm; 0.007mm^2.

$$|V_{th,p}| = |V_{th0,p}| + \gamma_p(\sqrt{|2\Phi_F| + V_{SB}} - \sqrt{|2\Phi_F|}) \quad (2)$$

$$g_m = \frac{\partial I_D}{\partial v_{GS}} = \frac{I_D}{nV_T} \quad (3)$$

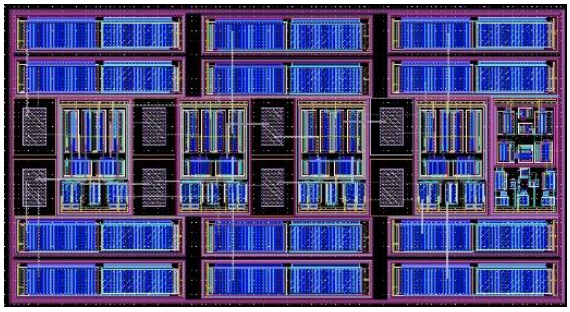

Fig. 3 The layout of overall comparator

Fig. 4 shows the DC gain of single cell. The gain of the overall circuit is 142.8dB for four cascaded OPAMPs. The timing diagram of comparator is given in Fig. 5. Reset and Comparison phased of the comparator are two operation duration. The evaluation of the comparison is realized after the offset cancellation in reset time.

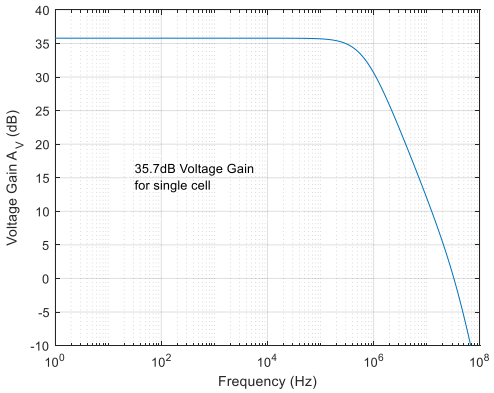

Fig. 4 DC gain of single cell.

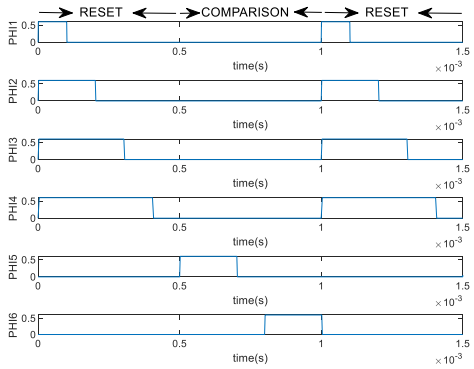

Fig. 5 Timing diagram of comparator.

Offset analysis under the variation of process (ss, tt, ff, sf, fs), power supplies (AVDD [0.54V, 0.66V]) and temperatures (−40ºC, 85ºC) is given in Fig. 6. The solution in Fig. 6 is realized without offset cancellation. Table 2 gives the offset value for each corners. Offset coming from fourth stage is suppressed by the 1st, 2nd and 3th stage gain. Furthermore, offset coming from third stage is suppressed by the 1st and 2nd stage gain. As a result, the most dominant offset contributed by M_7, M_8 is 1st- stage offset (Zhong, Bermak, and Tsui 2017).

The 1st- stage offset is cancelled out with auto-zeroing capacitances (50fF). Fig. 7 shows the Monte Carlo analysis of offset without offset cancellation (OC) Histograms of offset with OC technique given in Fig. 1. is shown in Fig. 8.

Table 2 The offset values according to the each corner

Temperature	-40º					27º					85º				
Process Variations	ss	tt	ff	sf	fs	ss	tt	ff	sf	fs	ss	tt	ff	sf	fs
AVDD=0.54V	22.9m	5.1m	3.3m	23.1m	3.6m	25.9m	5.3m	3.0m	26.0m	3.3m	28.6m	5.9m	3.6m	28.7m	3.1m
AVDD=0.60V	4.9m	3.2m	5.1m	3.5m	3.5m	5.2m	2.8m	5.4m	3.9m	3.1m	5.8m	2.6m	6.0m	2.0m	2.9m
AVDD=0.66V	5.1m	3.5m	2.3m	5.1m	3.4m	5.4m	3.1m	2.6m	5.4m	3.1m	6.0m	2.9m	2.8m	6.0m	2.9m
Offset Voltage is 5.4mV at nominal (for AVDD=0.6V, 27º and tt-process variation)															

Table 3 Comparison with the State of Art comparator designs

Parameters	(Cohen *et al.* 2005)	(Pipino *et al.* 2016)	(Belloni *et al.* 2010)	(Lu and Holleman 2013)	***This Work***
Technology	0.35µm	28nm	0.18-0.5µm	0.5µm	0.18 µm
Supply Voltage	3.3/4.5V	0.9V	1.8/5V	5V	0.6/1.8V
DC Gain	55.7dB	106dB	168dB	118.1dB	142.8dB
GBW	-	329kHz	260kHz	-	33.3MHz
Input Referred Offset Standard Deviation	413µV	2.2µV	1.94µV	50.57µV	6.5 µV
Supply Current	40µA	60µA	14.4µA	0.93µA	10.01µA
Power	160µW	54µW	26/72µW	4.62µW	6.01/17.06 µW
Area	0.0024mm^2	0.014mm^2	1.14mm^2	0.062mm^2	0.007mm^2

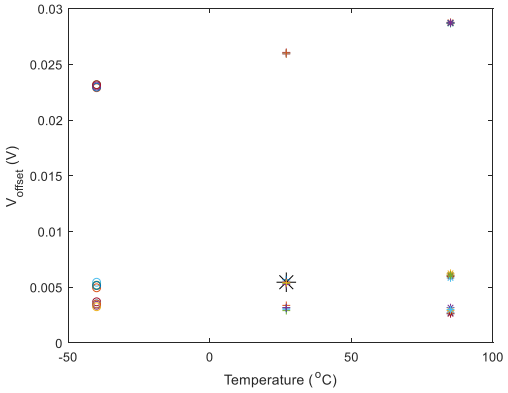

Fig. 6 Offset analysis {under the variation of process (ss, tt, ff, sf, fs), power supplies (AVDD [0.54V, 0.66V]) and temperatures (−40ºC, 85ºC)}.

Table 3 shows the comparison with state of art. The performances of designed comparator is higher than the previous works in terms of gain, GBW (gain bandwidth product) and core occupation area. GBW of the designed comparator is 33.3MHz while the core occupation area is 0.007mm^2 without Electrostatic Discharge Protection.

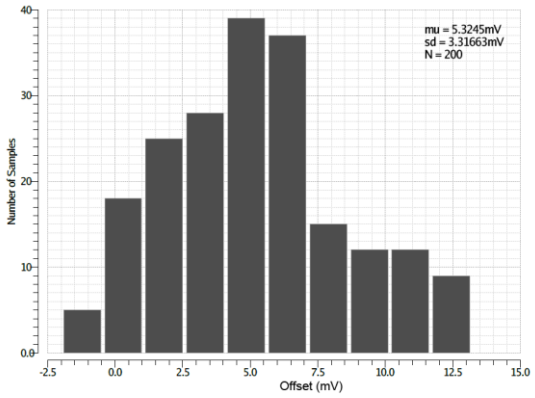

Fig. 7 Monte Carlo analysis of Offset without Offset Cancellation.

Fig. 9 shows the dynamic range of a single amplifier. The dynamic range of the comparator is increased with a new biasing technique for the positive rail. The positive rail of 0.56V approximately approaches to the positive supply voltage of 0.6V with the proposed biasing technique.

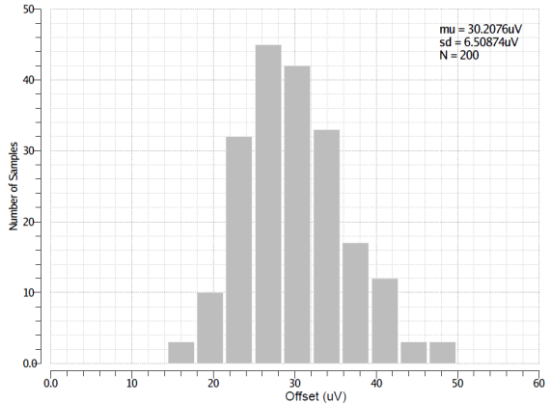

Fig. 8 Monte Carlo analysis of Offset with Offset Cancellation.

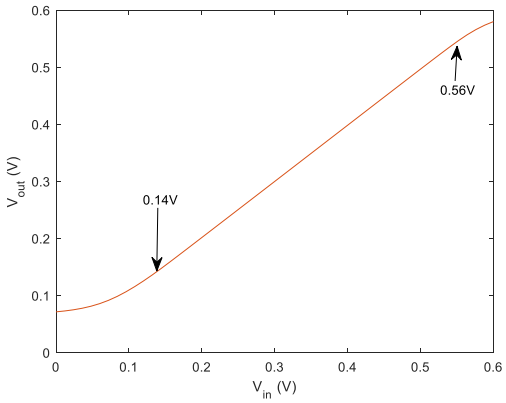

Fig. 9 Dynamic range of a single amplifier.

3. CONCLUSION

In this work, the design of a low power high precision comparator with 142.8dB gain is presented. The sub-circuits (OTA, latch) of the comparator is designed with DTMOS technique. The standard deviation of offset voltage is reduced from 3.31mV to 30.2µV. The core occupation of the designed circuit is 0.007mm^2. The comparator designed with offset cancellation can operate up to 30MHz with energy consumption per comparison of 20pJ. The designed comparator is implemented with TSMC 0.18µm process in Cadence environment.

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