GU J Sci, Part A, 7(2): 59-68 (2020)

Gazi University

Journal of Science

PART A: ENGINEERING AND INNOVATION

http://dergipark.gov.tr/gujsa

Experimental Verification of Output Inductor-less Phase-Shifted Full-Bridge Converter for Capacitor Charger Application

Halil KAVAK[1,*], Muhammed Yusuf CANDAN[2], M. Timur AYDEMİR[3]

[1,2]*ASELSAN Inc., Defense System Technologies Business Sector, Electronic Design Department, Ankara – TURKEY*
[3]*Gazi University, Faculty of Engineering, Dept. of Electrical and Electronic Eng. Ankara-TURKEY*

Article Info

Received: 22/02/2020
Accepted: 21/07/2020

Keywords

Output inductor-less, Phase-shifted full-bridge, Capacitor charger, DC-DC power conversion

Abstract

DC-DC power conversion can take three main forms in the sense of level conversion: buck (step-down), boost (step-up) and buck-boost (step-up/down). DC-DC power conversion from lower voltage value to a higher voltage value is called step-up application. A step-up application can be done with and without isolation. Non-isolated and isolated step-up power conversion can be achieved with different DC-DC converter topologies. In this paper, experimental verification of Output Inductor-less Phase-Shifted Full-Bridge (OIPSFB) DC/DC converter topology for constant current capacitor charging application is presented. The designed converter is able to charge an output capacitor to 700V DC. The charged capacitor can range from 1mF to 100mF. Experimental results are taken from a laboratory prototype with 24-36V DC input voltage range, maximum output power of 150W, switching frequency of 75 kHz and a digital average current mode controller. The results are for an output capacitor of 15 mF.

1. INTRODUCTION

Step-up power conversion can be achieved with or without isolated converter topologies. Isolated topologies such as forward, half-bridge and full-bridge DC-DC converters with step-down DC gain can be used for step-up applications [1]. The use of isolated topologies with step-down DC gain is possible for step-up application by means of transformer gain. The transformer gain is used to obtain a DC gain that is greater than 1, so that the step-up of the input voltage is achieved at the output.

A Phase-Shifted Full-Bridge (PSFB) DC-DC converter can be used for step-up of input voltage with a suitable transformer gain. The major disadvantage of the widely used PSFB converters is the reverse recovery losses in the secondary rectifier diodes and high voltage ringing caused by the resonance between the diode parasitic capacitance and transformer leakage inductance [2-7]. The stated problem exists not only in step-up converters, but also in step down power converters too [8]. The voltage ringing is quite important in step-up application since it is difficult to find devices with high voltage rating. The reverse recovery problem and the ringing voltage problem can be solved and/or avoided by means of snubbers [8]. As remedy to the stated problems, output inductor-less (output capacitive filtered) full-bridge topologies have been proposed in [2-4], so that the voltage stresses of the rectifier diodes can be clamped to output voltage, which eliminates the need for dissipative RC snubber or active snubber.

Use of fewer components in a converter is another important goal in the design in addition to avoiding the losses and voltage ringing. Fewer components are preferred not only for low cost but also for reliability. Especially in military applications, longer life and lower failure rate are preferred for the reliability of the system in which the converter is used is increased. As the name implies the output inductor-less (capacitive output filtering) full-bridge topologies do not have inductors, and this also eliminates the need for snubbers. As a result component count is further reduced.

*Corresponding author, e-mail: halilkavak@aselsan.com.tr

Moreover, the use of output inductor-less (output capacitive filtered) full-bridge topologies eliminate the ringing on the output diodes and this allows the designer to avoid the effects of high voltage on the rectifier diodes. Otherwise, voltage rating of output diode should be selected for higher voltages. Even in some cases, series use of diodes is needed to stand against high voltage due to ringing effects. Therefore, the component count is increased in addition to the increase due to the output inductor.

To prevent the ringing effect and eliminate the output inductor, LLC converter topology might be an alternative. However, LLC converter is not a fixed frequency converter. It should operate at different frequencies for different line and loading cases. In a capacitor charger application with changing line and zero load cases, the operating frequency varies in a wide range resulting in reduction in efficiency [9]-[10]. It also complicates magnetic component filter design [10]. In addition to this frequency variation, LLC converter needs additional capacitor for resonant operation. This additional capacitor reduces overall reliability.

Detailed theoretically parameterized output characteristics for the converter and commutation analysis of the power switches can be found in literature [7]. However, suitability of this converter for capacitor charging applications and its experimental verification were needed. In this paper, digital average current mode-controlled Output Inductor-less Phase-Shifted Full-Bridge (OIPSFB) converter is experimentally verified for constant current charging of a 15mF capacitor to 700V DC. The implemented converter is able to convert low and variable input voltage to constant high voltage with capacitor charger ability. The DC gain of the implemented converter is around 18. This gain is pretty high as compared to gains of OIPSFB converters given in literature [2,6,7,11].

The remaining of the paper is structured as follows: Operation principles are presented in Section II. Section III explains the considerations needed for the design process. Experimental work is described in Section IV.

2. OPERATING PRINCIPLE

In Fig. 1, the circuit diagram and main waveforms for Continuous Conduction Mode (CCM) operation of the OIPSFB converter are shown. The primary-side switches are controlled with the conventional phase-shift control, that is, both halves of the bridge network operate with a 50% duty cycle and the phase difference between the half bridge switch networks is controlled [12]. For CCM operation, the static gain of the converter is as given in equation (1):

$$\frac{V_{out}}{V_{IN}} = 2nD \tag{1}$$

The effective duty cycle ratio “D” given in equation (1) is seen once in half of the period. Since this duty cycle is seen twice in a single switching period, the DC gain is same as standard full bridge converter in continuous conduction mode. For DCM operation of the converter, equation (2) and (3) can be used. Similar gain equations can be found in [2] and [11].

$$K = \frac{D^2 R_o}{Lf} \tag{2}$$

$$\frac{V_{out}}{V_{IN}} = \frac{\left[-\frac{K}{n} + \sqrt{\frac{K^2}{n^2} + K} \right]}{2} \tag{3}$$

The details of operation in CCM is given below:

T0-T1: “S1 and S4” and “D1 and D4” are in conduction. Transformer primary and secondary voltages are positive. Power is drawn from input and transferred to the secondary side. Also, energy is stored in L_R due to current passing through.

T1-T2: "S2 and S4" and "D1 and D4" are in conduction. Energy stored in L_R is transferred to the secondary.
T2-T3: "S2 and S3" and "D1 and D4" are in conduction. Primary voltage is negative and secondary voltage is positive. Due to negative primary voltage L_R is discharged faster as compared to the previous interval.
The rest of the intervals for CCM is similar to the preceding intervals.

The details of operation in DCM is given below:

T0-T1: "S1 and S4" and "D1 and D4" are in conduction. Transformer primary and secondary voltages are positive. Power is drawn from input and transferred to the secondary side. Also, energy is stored in L_R due to current passing through.
T1-T2: "S2 and S4" and "D1 and D4" are in conduction. Energy stored in L_R is transferred to the secondary. At the end of this interval, secondary current becomes zero so that D1 and D4 turn off.
T2-T3: "S2 and S3" are in conduction. No diodes are in conduction. The parasitic capacitances of output diodes L_R resonates. Please not here that output diodes are assumed to be without parasitic capacitor in the following figure.
The rest of the intervals for DCM is similar to the preceding intervals. For detailed operation principles of each mode and interval one can visit [2] and [11].

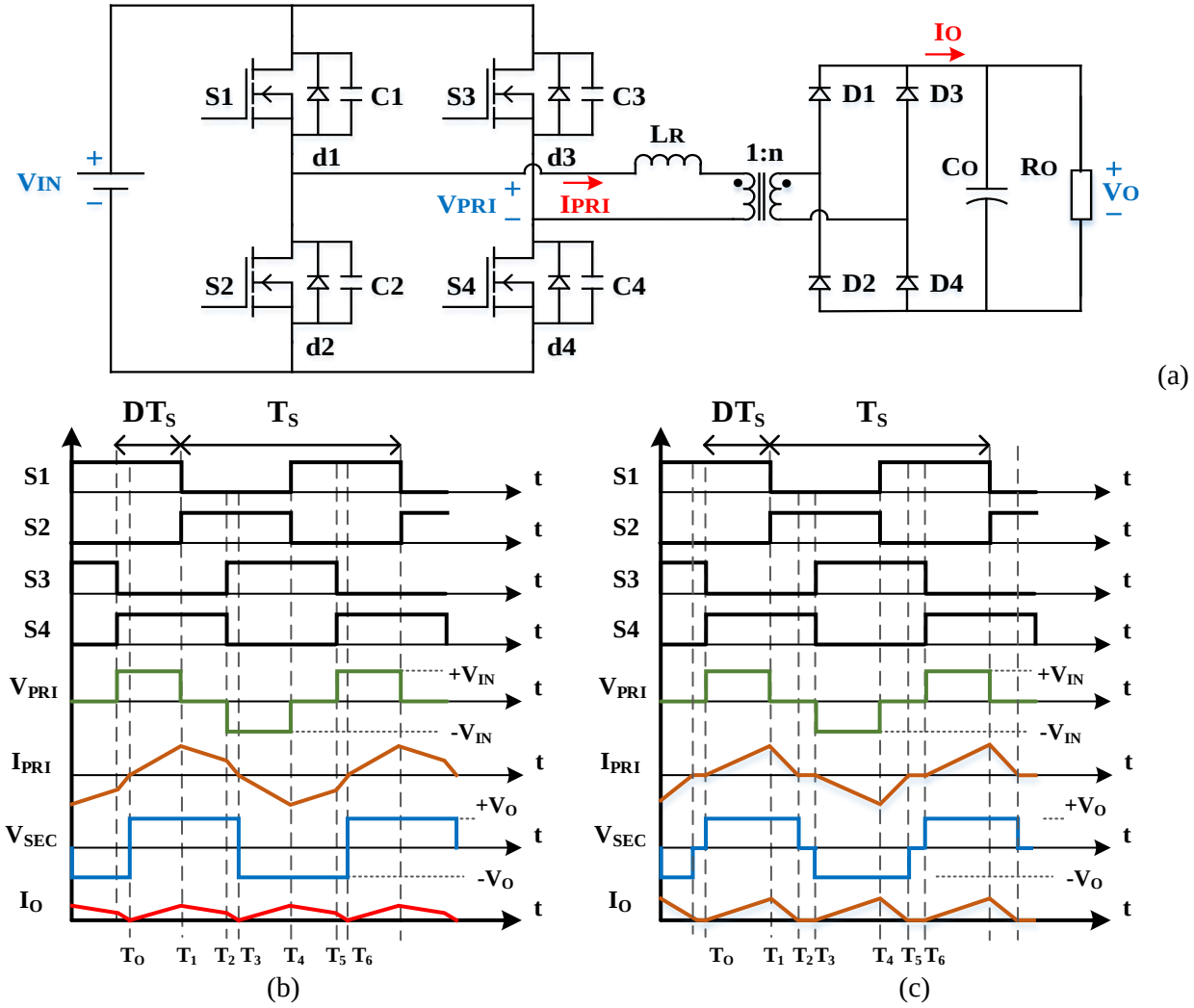


Figure 1. *Circuit diagram and main waveforms for the CCM of the OIPSFB converter. (a) Main power circuit, (b) CCM waveforms, (c) DCM*

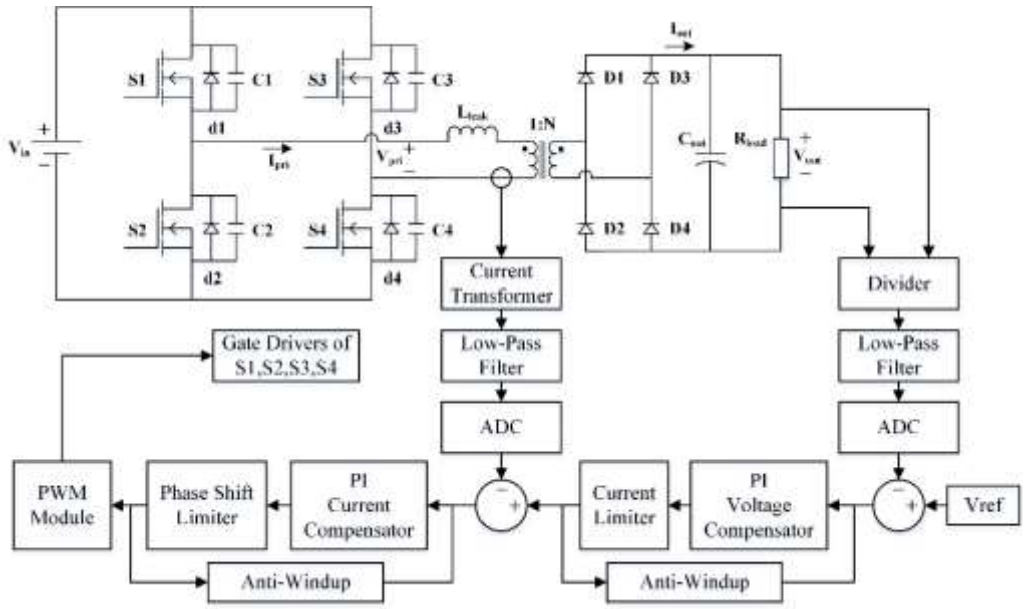


Figure 2. *Block diagram of the average current mode controlled OIPSFB converter*

3. DESIGN CONSIDERATIONS

A 150W prototype of the converter was built for 700V DC output voltage. The design specifications of the converter and the selected components are given in Table I and Table II, respectively. The input voltage is selected for a military vehicle bus voltage which is nearly 28V DC at the battery terminals and around 24V DC at the load (DC-DC converter in this case) terminal. The output voltage is 700V DC that is used as DC bus for a motor drive with standard switching elements with rating around 1000V or above. For selection of the output voltage (700V DC) market availability of high voltage high capacitance electrolytic capacitors is important as well as the rating of available MOSFET/IGBT switches. The capacitor with capacitance value of 15 mF is an intentional selection based on the high voltage high capacitance electrolytic capacitors available in the market (30mF/400V capacitors are connected in series to get 15 mF). Switching frequency selection is based on engineering experiences and to use readily available EMI filters.

One of the most critical parameters in this topology is the equivalent resonant inductor including both transformer leakage inductance and inductance of an additional discrete element [12] if needed. In this prototype, windings are designed such that the resonant inductance value is achieved only by the leakage inductance, which eliminates the need for an external inductor. The elimination of external inductor not only reduces the component count and cost, but also increase the overall reliability. There is a trade-off between power handling capability and efficiency in resonant inductor selection. Increasing the value of resonant inductor yields in increased efficiency of the converter. On the other hand, the increased value of the resonant inductor results in reduction of power transfer for low input line cases. The equivalent resonant inductance should be less than the value needed for maximum power delivery at the lowest input voltage and more than the value satisfying the desired efficiency provided by soft commutation of the primary switches.

In Fig. 2, proposed feedback control system for the application is shown. For constant current charging operation, a digital average current mode controller with appropriate current limiter is designed in a dsPIC environment [13]. Using a current transformer, a scaled value of the primary current is rectified, filtered and fed back to the inner loop so that the average of the current fed to the transformer is controlled. The sense of the current fed to the transformer enables the converter to control not only the active power but also the reactive power exchanged between the transformer and input filters. By controlling the reactive power, the converter is able to operate with higher output capacitance values, even with indefinite output short cases. In addition to current sense and control; the output voltage is scaled, isolated, filtered and fed back to the outer loop of the control system. The output voltage sense and

control enable the converter to keep the output voltage within the desired limits after charging the capacitor. Because of the current and phase shift depend on these loops, both loops have anti-windup for the integrators to prevent undesired overshoots after signal limits.

The gain of the transformer is selected to achieve 700V DC output voltage for inputs lower than 24V DC. The ratings of the semiconductor devices are in accordance with the current and voltage stresses seen on the devices.

Table 1. *Design Specifications*

Parameter	***Value***
Input DC Voltage Range	24-36V DC
Desired Efficiency	>90%
Output DC Voltage	
Maximum Output Power	150W
DC-DC Switching Frequency	75kHz
Output Capacitor	15mF

Table 2. *Component Selection*

Parameter	***Value***
S1-S4	Si-MOSFET, 150V/90A
D1-D4	SiC-Diode, 1200V/8.5A
Transformer Turns Ratio	1:40
Transformer Leakage Inductance	2.22µH
Transformer Core Type	PQ4040

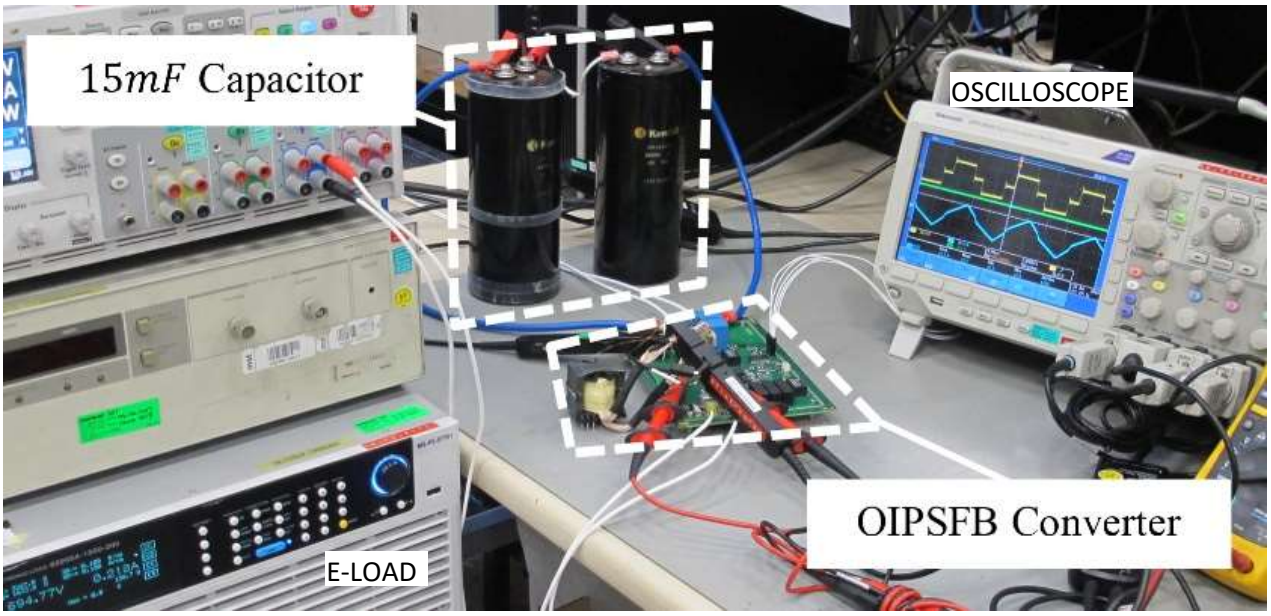


Figure 3. *Experimental prototype of the 150W OIPSFB converter for 15mF capacitor charger application*

4. EXPERIMENTAL RESULTS

In Fig. 3, experimental prototype setup is shown. For 15mF, two series connected 30mF/400V capacitors are used. For the resistive output load, dynamic response to load change and short circuit tests, a 1200V/5kW electronic load is used. The maximum resistance value provided by the electronic load is 20kΩ, that is, why for the no external load cases there is still approximately 25W power delivered. The tests were conducted at an ambient temperature around 26 °C.

In Fig. 4, main waveforms for Continuous Conduction Mode (CCM), Boundary Conduction Mode (BCM) and Discontinuous Conduction Mode (DCM) are given. The converter is operated with 150W load for different input voltages so that different conduction modes are obtained. In other words, since the input voltage range is wide the converter operates at different conduction modes.

In this topology, the main source of loss is the circulating energy (no power delivery) interval, that is, conduction loss due to high RMS current passing through the switches. For lower input voltages, more effective duty cycle is needed, which results in less interval for circulating energy. So, the efficiency at the lower input is expected to be high. The efficiency for the input voltage of 24V DC at full load for one hour of operation without heat sink on switches is shown in Fig. 5. Note that the efficiency of the converter is decreased by the time and leveled after a while. This is due to the positive temperature coefficient (PTC) devices used in the design, since PTC device resistance increases with the temperature not only the MOSFET switches but also the SiC diodes at the output are PTC devices [14-15]. Therefore, the initial efficiency is higher due to low temperature and low resistances (loss elements). The efficiency is leveled after the thermal balance is satisfied. Note that, the efficiency of the converter can be kept at higher value by keeping the temperature of the PTC components at a low value by means of heat sink and/or using an air circulation to drive the dissipated heat away.

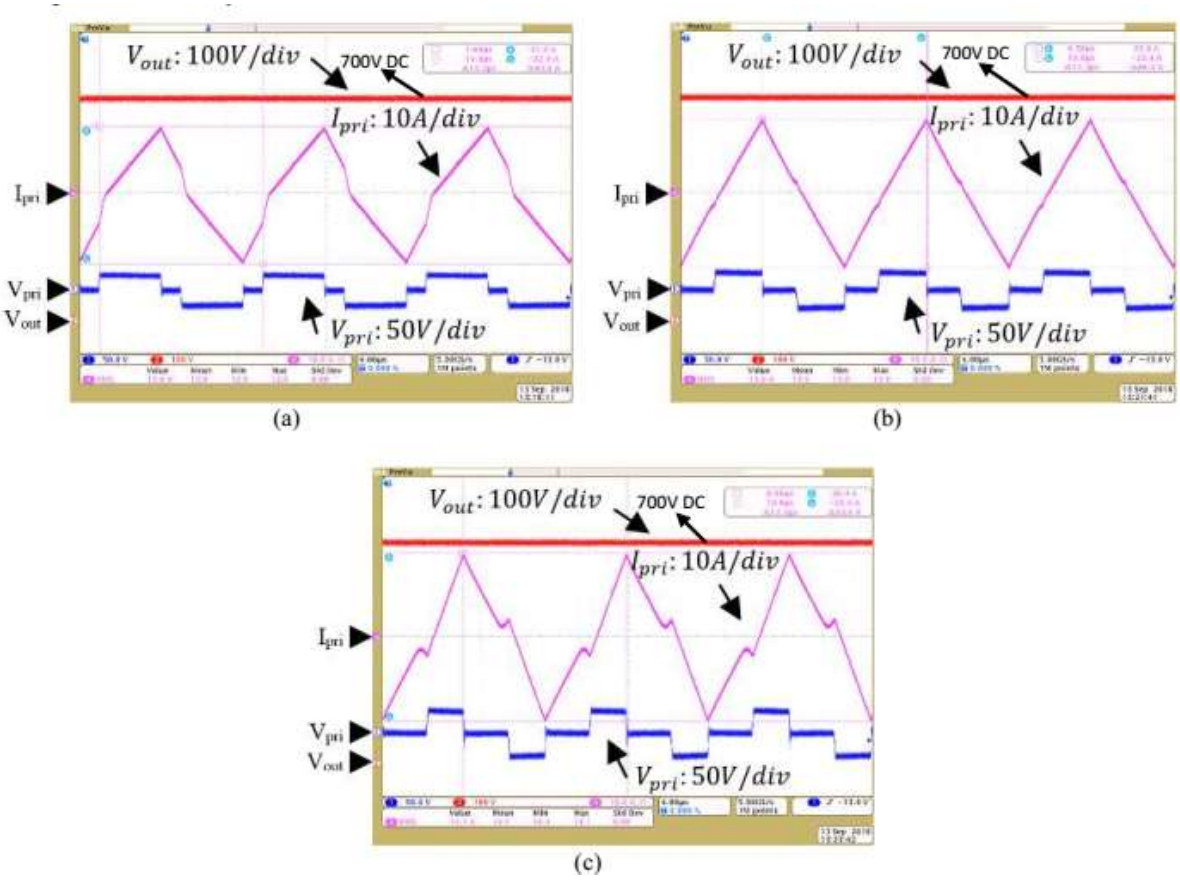


Figure 4. *Experimental waveforms of V_{out},V_{pri} and I_{pri} at 150W full load. (a) CCM, Input voltage, $V_{in} = 24VDC$. (b) BCM, Input voltage, $V_{in} = 28VDC$. (c) DCM, Input voltage, $V_{in} = 36VDC$*

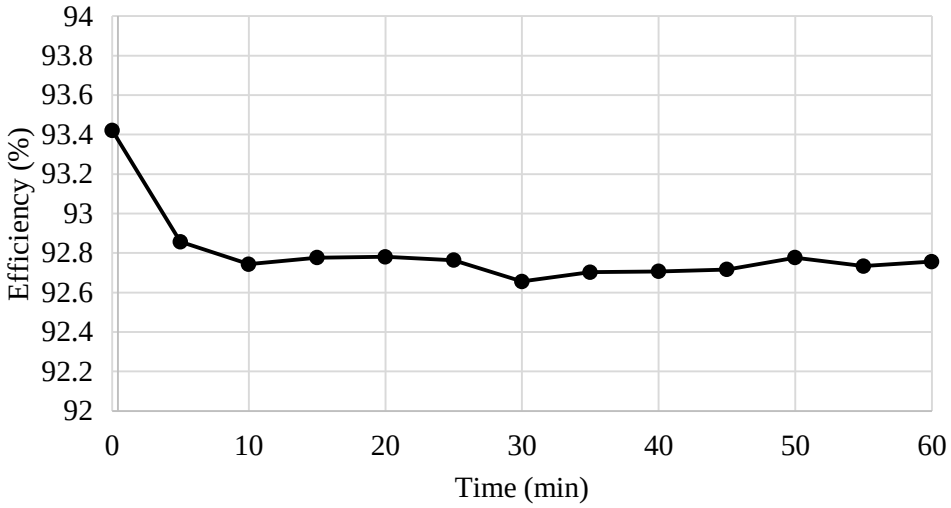


Figure 5. *Efficiency vs. time (minutes) for 24V DC input voltage at full load operation*

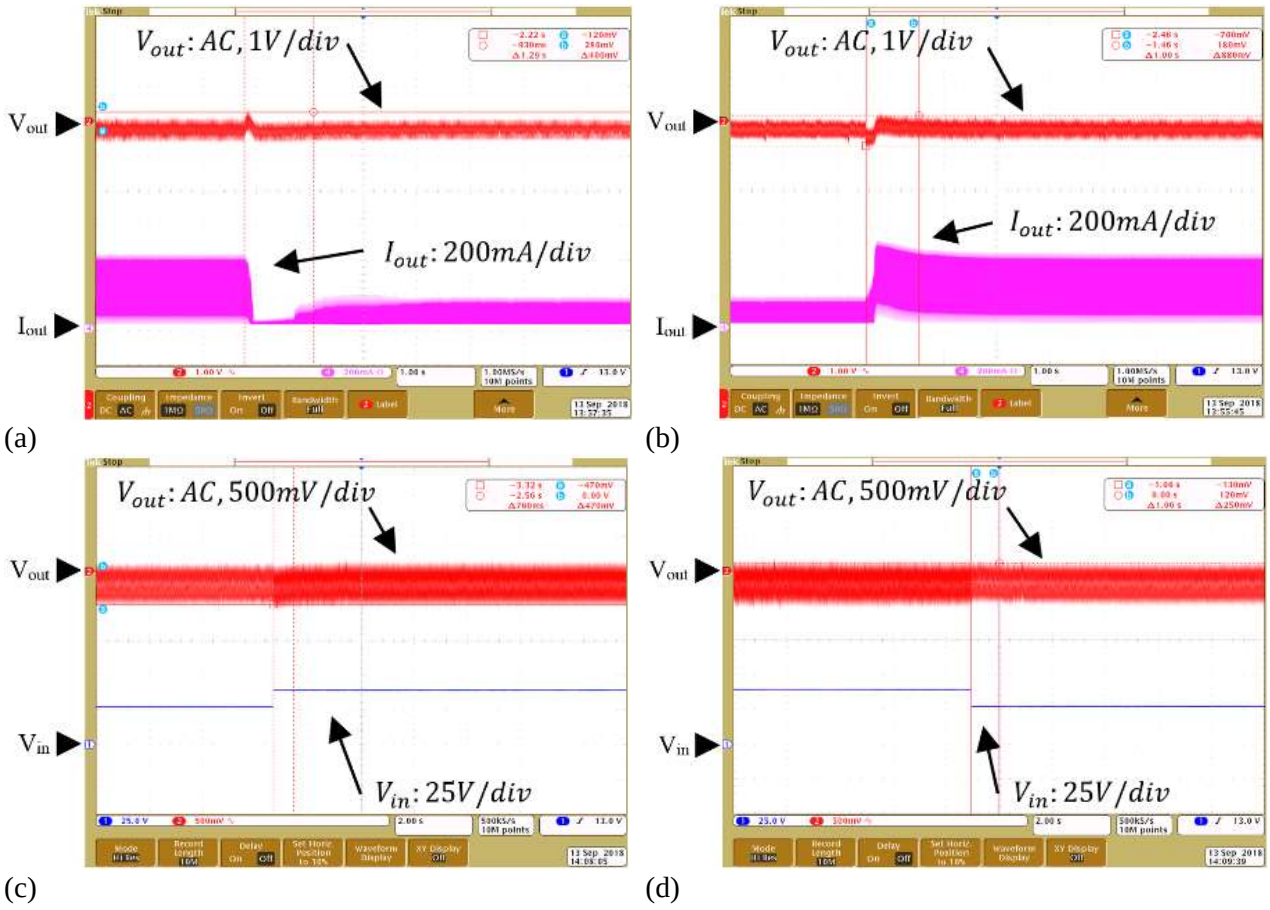


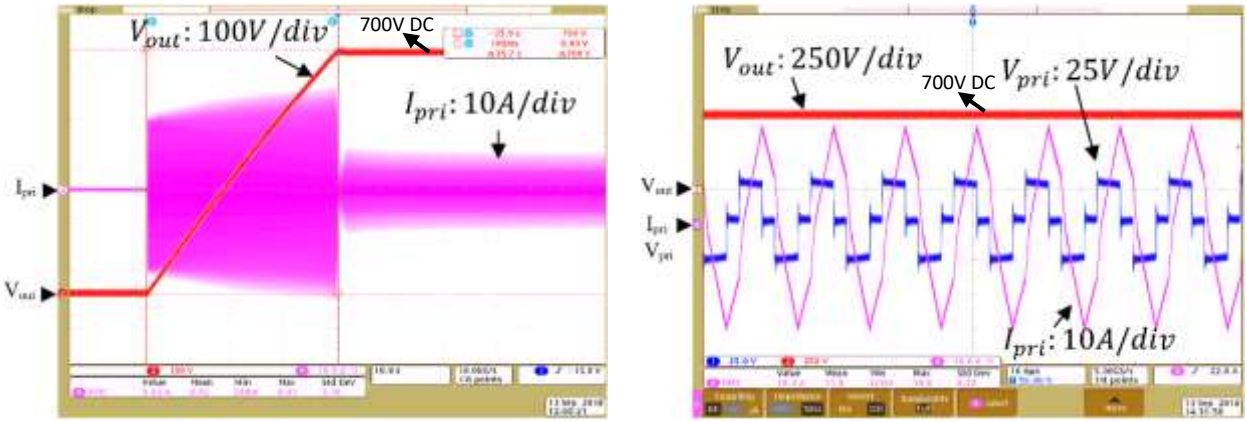
Figure 6. *Experimental waveforms of dynamic responses. (a) Load change from full load to no load. (b) Load change from no load to full load. (c) Input voltage change from 24V DC to 36V DC. (d) Input voltage change from 36V DC to 24V DC.*

Dynamic responses of the controller for the output load and input voltage changes are tested and associated waveforms are shown in Fig. 6. These waveforms are taken when the output capacitor of 15mF is connected. That is the reason why the responses are slow. As can be seen from Fig.6, the converter

responds to the changes in a stable manner. That is, the controllers designed for the converter are stable.

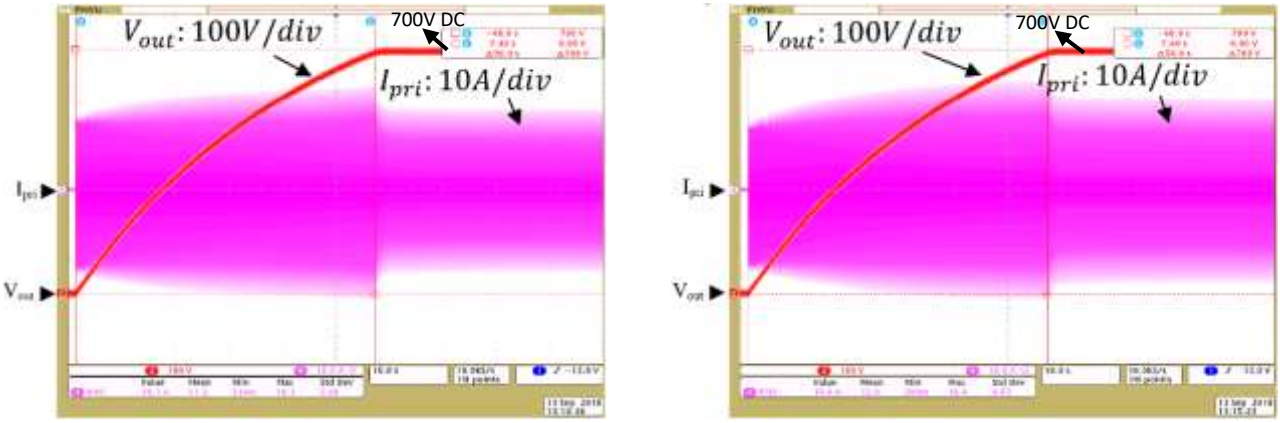
For constant current charging, $18A_{rms}$ current limit is set for the transformer primary current. This value is determined considering the maximum RMS current in the primary at full load. This current limit is kept the same for all input levels and output conditions. By means of this limit, the converter can operate with higher output capacitances even with indefinite output shorts.

Waveform of full charging operation taking 35.7 seconds and zoom in version of an instant from this operation for 28V input voltage are shown in Fig. 7.a and Fig. 7.b, respectively. During this charging, the output contains no load other than the capacitor connected. Note from Fig.7 that the current fed to the transformer is limited. That is average current controller is able to keep the current below the defined value. Note also from the figure that the output does not rise linearly. Because the constant RMS current does not imply constant active current, the rise of voltage is nonlinear. Moreover, as the voltage increases at the output, the power transferred to the secondary side is increased, since the increasing output capacitor voltage results in higher output impedance. The increased impedance means the matching between primary and secondary is better, so that the power transfer is better.



(a) (b)

Figure 7. *Experimental waveforms of V_{out} and I_{pri} for 15mF capacitor charging at 28V input and no external resistive load. (a) Complete charging waveform of V_{out}. (b) Waveform showing RMS current limit of $18A_{rms}$ in I_{pri} during charge.*



(a) (b)

Figure 8. *Experimental waveforms of V_{out} and I_{pri} for 15mF capacitor charging at 150W full load. (a) Input voltage $V_{in} = 28VDC$, (b) Input voltage $V_{in} = 36VDC$*

In Fig. 8, charging waveforms at full load for different input voltages are shown. Since the resistive load is included in these tests, the rise of voltage is more nonlinear (order of the input impedance is increased). The presence of the resistive load increased the total charging time. Because of the constant current operation, the charging time for input voltage of 28V DC and 36V DC are almost the same (56 seconds) at full resistive load.

Note that the charging process in the design is at constant switching frequency. The obtained charging durations are based on this constant frequency operation. The duration can be changed by using a different operation algorithm for the converter. For instance, one can use a different frequency of operation depending on the level of the output voltage.

5. CONCLUSIONS

In this paper, experimentally verified, digital average current mode controlled OIPSFB DC/DC converter topology for constant current charging of a 15mF capacitor to 700V DC from 24-36V DC input voltage at maximum output resistive load of 150W is presented. After briefly describing the operation principles of the topology, design considerations are stated and experimental results of steady-state operation, dynamic responses and full waveforms for charging characteristics at different conditions are provided. During the presentation of the results the comments for the related figures are provided within the text.

The implemented and tested converter showed that it is possible to implement a high gain step-up converter as a capacitor charger using this topology. The test results showed that the hardware design, control loop design and software design are successful. Moreover, it can be seen from the test results that control loop design is valid both for CCM and DCM mode operations of the converter.

It is also clear from the unloaded tests of the converter that capacitor charging with a fixed frequency converter is possible. However, it is also clear from the results that “charging a capacitor with constant current” is not possible using a fixed frequency converter. On the other hand RMS of the current can be limited so that short circuit protection can be implemented for the converter. RMS current control enables the converter to protect itself from continuous output short circuits.

CONFLICT OF INTEREST

No conflict of interest was declared by the authors

REFERENCES

[1] Forouzesh, M., Siwakoti, Y. P., Gorji, S. A., Blaabjerg, F., & Lehman, B., “Step-Up DC-DC converters: A comprehensive review of voltage-boosting techniques, topologies, and applications” *IEEE Transactions on Power Electronics*, 32(12), 9143-9178 (2017) https://doi.org/10.1109/TPEL.2017.2652318.

[2] Gautam, D. S., Musavi, F., Eberle, W.,and Dunford, W. G., "A Zero-Voltage Switching Full-Bridge DC-DC Converter With Capacitive Output Filter for Plug-In Hybrid Electric Vehicle Battery Charging" in *IEEE Transactions on Power Electronics*, 28(12), 5728-5735 (2013).

[3] Lee, W., Kim, C., Moon, G.and Han, S., "A New Phase-Shifted Full-Bridge Converter With Voltage-Doubler-Type Rectifier for High-Efficiency PDP Sustaining Power Module" in *IEEE Transactions on Industrial Electronics*, 55(6), 2450-2458 (2008).

[4] Pahlevaninezhad, M., Das, P., Drobnik, J., Jain, P. K. and Bakhshai, A., "A Novel ZVZCS Full-Bridge DC/DC Converter Used for Electric Vehicles" in *IEEE Transactions on Power Electronics*, 27(6), 2752-2769 (2012).

[5] Cha, W., Kwon, J. and Kwon, B., "Highly Efficient Asymmetrical PWM Full-Bridge Converter for Renewable Energy Sources" in *IEEE Transactions on Industrial Electronics*, 63(5), 2945-2953 (2016).

[6] Domoto, K., Ishizuka, Y., Abe, S. and Ninomiya, T., "Output-inductor-less full-bridge converter with SiC-MOSFETs for low noise and ZVS operation," *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Long Beach, CA, pp. 2422-2429 (2016).

[7] Bottion, A. J. B. and Barbi, I., "Full bridge zero-voltage-switching PWM dc-dc converter with output capacitive filter" *2015 IEEE 13th Brazilian Power Electronics Conference and 1st Southern Power Electronics Conference (COBEP/SPEC)*, Fortaleza, pp. 1-6 (2015).

[8] Sahaté, J.A., Vlatkovic, V., Ridley, R.B., and Lee, F.C., "High-Voltage, High-Power, ZVS, Full-Bridge PWM Converter Employing an Active Snubber", *IEE APEC*, 158-1663 (1991).

[9] Jovanovic, M. M. and Irving, B. T., "On-the-Fly Topology-Morphing Control—Efficiency Optimization Method for LLC Resonant Converters Operating in Wide Input- and/or Output-Voltage Range" *IEEE Trans. Power Electron*., 31(3), 2596-2608 (2016).

[10] Luo, J., Wang, j., Fang, Z., & Shao, J., & Li, J., "Optimal Design of a High Efficiency LLC Resonant Converter with a Narrow Frequency Range for Voltage Regulation" *Energies*. 11. 1124. 10.3390/en11051124 (2018).

[11] Jitaru, I. D., "A 3 kW soft switching DC-DC converter" in *Proc. 2000 IEEE Appl. Power Electron. Conf. Expo*., 1, pp. 86–92 (2000).

[12] Erickson, R. W., Maksimovic, D., "Fundamentals of Power Electronics", *Kluwer Academic Publishers*, 2nd Edition (2003).

[13] Candan, M.Y., Kavak, H., Ankaralı,M.M., "Modeling and Simulation of High Gain Output Inductor-Less Full-Bridge Capacitor Charger with 28V DC Military Bus Input and 700V DC Output", *8th National Defence Modelling and Simulation Conference* (2019).

[14] IXYS Corporation, "X3-Class HiPerFETTM Power MOSFET", DS100808B (10/17) (2017).

[15] CREE, "C2D05120E, Silicon Carbide Schottky Diode, Zero Recovery® Rectifier", C2D05120E Rev. B. (2013).