BALKAN JOURNAL OF ELECTRICAL & COMPUTER ENGINEERING, Vol. 8, No. 1, January 2020

Desinging Analog Mixed Signal Circuits Using Graphene Nano Ribbon Field Effect Transistors

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***Abstract*—Graphene is a 2D material formed by planar honeycomb placement of Carbon atoms. Besides its many superior physical properties it has superior electronic properties foremost of which is the high mobility it possesses. Due to this high mobility many Graphene based transistors have been designed. Graphene nano ribbons exhibit a band gap property, which is crucial for implementing transistors as switches. Moreover there exist models for these Graphene Nano Ribbon devices. In this work we first propose a gate array based manufacturing approach. Next assuming devices manufactured in this gate array methodology. We realize and simulate analog mixed signal blocks using Graphene Nano Ribbon transistors. The particular blocks that we used included telescopic amplifiers and StrongARM latches. Next we compared these blocks' performances against the same blocks implemented in 14nm high performance Silicon CMOS transistors. As a result we observed that the graphene transistors could attain comparable performances to circuits designed in 14nm CMOS. Specifically Graphene blocks can reach up to 80% of the bandwidth of Silicon devices. However Graphene devices have greater power consumption as a result of higher leakage current.**

Index Terms—***Graphene; Nano Ribbons; Nano Technology; Graphene Transistors; Graphene Circuit Design; Graphene Transistor modelling.***

I. INTRODUCTION

GRAPHENE IS the 2D material comprised of a monolayer of carbon atoms arranged in a honeycomb lattice. Graphene and other 2D materials have superior electrical and mechanical properties than compared to other materials. For example, electronics can move relatively massless within this structure. As a result the electrons are delocalized and exhibit anomalous quantum Hall Effect. Moreover high electron mobility in Graphene, high Young's modulus and high thermal conductivity are all superior properties of this material that increase the possible uses of graphene. In short graphene is a multi purpose material that will have many industrial uses going forward [1-4].

High mobility is a very attractive electronic property of graphene. Due to this property same voltage can induce higher levels of current compared to other materials of similar dimensions. Therefore graphene transistors have many advantages for use as high-speed switching and amplifying devices.

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Manuscript received August 05, 2019; accepted December 21, 2019.
DOI: 10.17694/bajece.601554

Despite these advantages transistors that can switch voltages and currents on and off has not been possible to realize. The main reason for this is the lack of a significant band gap between the valence and conduction bands in graphene devices. The electrons can move freely between valence and conduction bands. That is even though current can be created between the source and drain terminals of a transistor, this current cannot be reduced to significantly merely by changing the gate voltage. And the transistor on-current off-current ratio is not large enough. As a result graphene transistors using 2D graphene sheets as bodies cannot be used to design logic gates.

Single transistor amplifiers such as Low Noise Amplifiers or other single transistor circuits have been designed and published earlier. Also very simple analog circuits were simulated using GNRFET models.[5]

In this study using graphene transistor models developed for graphene nano ribbon based transistors are used to simulate practical analog mixed-signal circuits such as telescopic amplifiers and Strong ARM type latches. The novelty of our study comes from two aspects. First we are proposing a gate array based methodology to realize the multiple GNRFET devices. Second by using these devices and the GNRFET models available in literature we are simulating analog mixed signal blocks and estimating their performances. The existing GNRFET circuits are mainly digital designs [6, 7] however in our work we chose to study frequently used analog mixed signal circuit blocks such as telescopic amplifier and comparators. Additionally the same circuit blocks are designed using 14nm Silicon CMOS transistors. Finally two designs are compared in terms of a number of circuit parameters.

The rest of the paper is outlined as follows. Section II discusses the devices and intended gate array based manufacturing method. Section III describes the realized circuits. Section IV discusses the simulation results and comparisons between GNRFET and Silicon devices. Section V is the conclusion.

II. DEVICES

Circuits using 2D graphene transistors are generally used to design Graphene circuits. These circuits usually include single transistor LNA's, RF mixers and other amplifiers [8]. As mentioned earlier it's not surprising as Graphene devices are used to fast operation.

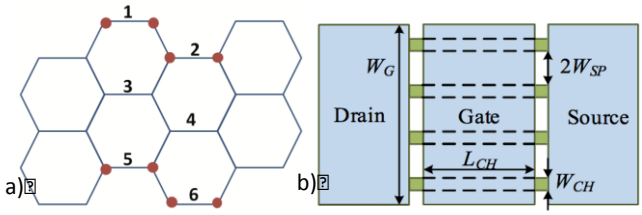

Figure 1 a) Graphene nano ribbon lattice diagram for a 6 dimer and armchair AGNR form structure [9] b) GNR transistör illustration. [10]

A. Physical Properties

When graphene is implemented in 1D it can have a larger band gap voltage. That is when graphene transistor bodies are realized on 10-100nm wide Graphene Nano Ribbons (GNR) a band gap voltage that is inversely proportional to the width [9, 10]. Despite the fact that below 100nm wide graphene nano ribbons exhibit band gap voltage when the graphene width goes over 100nm the band gap drops to converge eventually to the non existent band gap observed on 2D graphene structures.

Due to the extreme dimensions of graphene nano ribbons we can assume that they would include a small number of dimer lines (5-20). Additionally we can assume that the ribbons will be in Armchair GNR configuration (AGNR) [10].

Illustrations of the physical and structural parameters of the Graphene Nano Ribbons as well as the GNR Field Effect transistors (GNRFET) are included in Figure 1. In this figure gate, source and drain terminals are assumed to be covering multiple of graphene nano ribbons, as transistor bodies. In this figure each terminal covers 4 nano ribbons

The cross section of a GNRFET is shown in Figure 2. Here a SiO2 layer is added below the gate terminal. While the source and drain terminals are deposited right above the GNR sections.

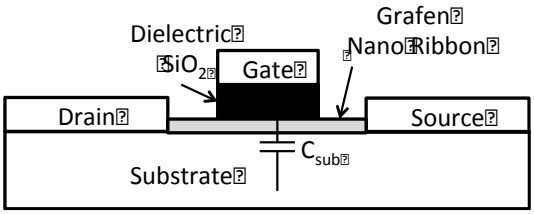

Figure 2 Transistor cross section

The source and drain terminals are expected to contact all the nano-ribbons. The distance between these two terminals constitute the channel length of the transistors. Nominally the channel lengths are assumed to be around 15nm. The total width of all the nano ribbons under the terminals defines the total width of the transistor. The transistor widths can be expected to assume discrete values, which is similar to FinFET devices.[11]. Using more transistors in parallel is the main mechanism to realize wider transistors. We assume that the nano-ribbons used in our case has 12-15dimer lines [12]. It can be noted that if the number of ribbons is low within the transistor the terminals need to be carefully aligned. However using a higher number of ribbons can alleviate any problems due to contact misalignment can be remedied.

In addition to the nano ribbon widths their separation is an additional physical parameter. This inter-ribbon spacing leads to a sub-optimal usage of area.

B. Fabrication Plan

Assuming a substrate with GNR's, and as seen in Figure 3 we can first shape GNRFET gate array [13] unit elements by etching graphene to create separations between GNRFET 's. Next regular arrays of electrodes are deposited to cover all GNR strips across all unit elements. For each transistor only 3 terminals are deposited. Two terminals are the source and drain electrodes while the third terminal is the gate electrode. The electrodes are anticipated as 5nm thick chromium layer and 100nm thick gold layer. The first two operations allow us to have a GNRFET transistor array and last but not least multi layer connections.

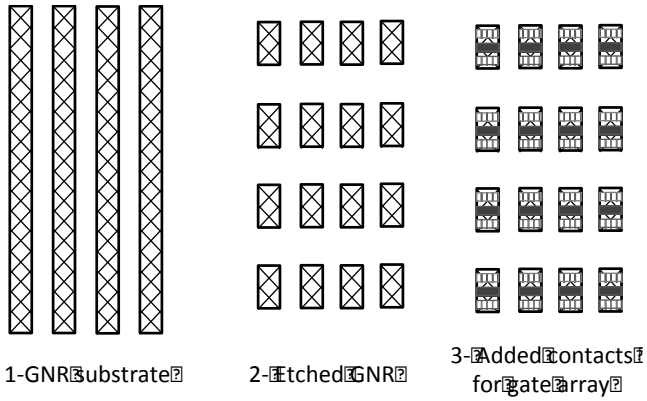

Figure 3 Preparation for GNRFET gate array

Once the devices and their electrodes are realized, the inter-device connections can be realized using SiO_2 insulation and gold metallization. In summary after fabricating a base device that includes structures similar to a gate array. The additional interconnect can be implemented to realize intended circuits. The final form of the intended circuit realization can be illustrated in Figure 4.

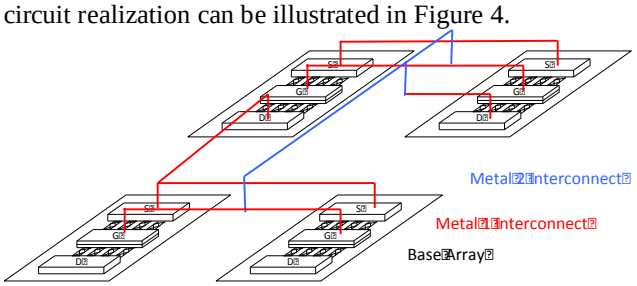

Figure 4 Gate array - like methodology.

The gate array implementation will obviously lead to inefficient use of area. For example to realize a transistor with W/L = 28n/14n we would roughly need 100n x 50n area per transistor. However till we can selectively grow GNR's the possible till then gate array methodology is a reasonable compromise.

C. Electronic Properties and Models

The transistor models that were utilized for this study are developed and published by UIUC [12]. They are compatible with SPICE format and can be used with commercial circuit simulators. The parameters used for these models are as follows: Channel length (L_{CH}), Nano ribbon width (W_{CH}), Gate terminal width (W_G), Spacing between ribbons ($2W_{SP}$), SiO2 -oxide- thickness (t_{ox})

The main mechanism that creates the transistor current is the current induced within the channel [9]. The small dimensions of the transistors have significant impacts on their electronics parameters. First of all due to the small

dimensions of the devices their supply voltages are 0.8V. Therefore the any designs using these transistor models will need to observe low power and low voltage circuit design principles. Moreover again due to the small device sizes increased inter transistor capacitance and capacitive coupling will deserve extra attention.

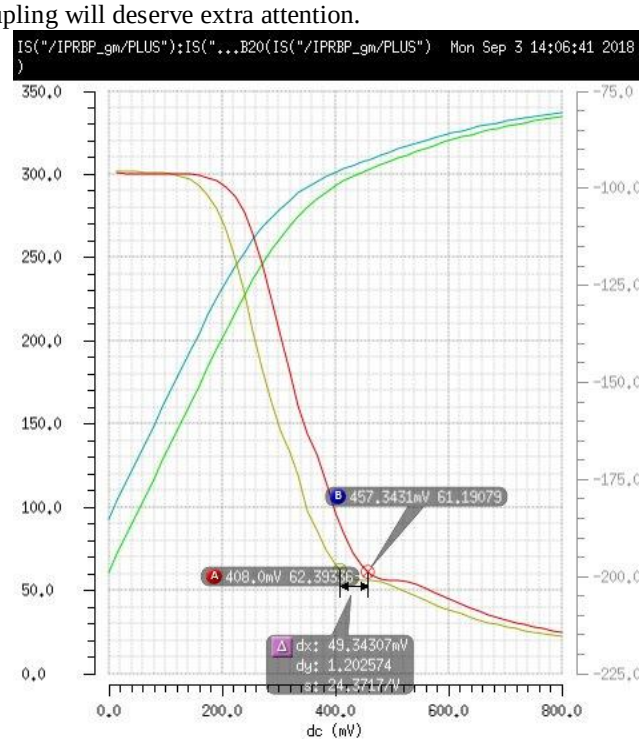

Figure 5. log(I_{DS}) vs. V_{GS} Gate voltage for the GNRNFET (green) and GNRPFET (cyan) devices. The I-V curves' slopes for GNRNFET(red) and GNRPFET (yellow) are also plotted to estimate their threshold voltages of

Transistors use 0.8V as supply voltage. For transistors to operate successfully at such supply voltage levels the threshold voltages be accordingly. As a result of our simulations the NFET transistors using the Graphene Nano Ribbons (GNRNFET) have a threshold voltage of 457mV and PFET devices (GNRPFET) have thresholds of 408mV. The plot for the simulations supporting this conclusion is shown in Figure 5. Here Threshold voltage is defined as the infliction point of the logarithmic plot of the transistor current.

The internal voltage gain (g_m * r_o) of the transistors, which is an important criterion in analog circuit design, is simulated next. These results are shown in Figure 6 where the GNRPFET internal gain is at maximum 15 and the GNRNFET internal gain is at maximum 2100. When looked closer the NFET output resistance seems to have a value of 3 orders of magnitude larger than the PMOS.

III. Realized Circuits

To analyze the performance of GNR based circuits mixed signal circuits will be designed using both GNRFET transistor models and also using 14nm Silicon CMOS based transistor models. The performance results of these circuits will be compared to test the viability of GNRFETs to be used in mixed signal circuits. The Silicon transistor are used assuming 14nm process node where the models are from Predictive Technology Modeling (PTM) variant which targets FinFET modeling [14]. Because the GNRFET devices have 15nm channel length, the silicon transistors selected for comparison also had 15nm channel lengths.

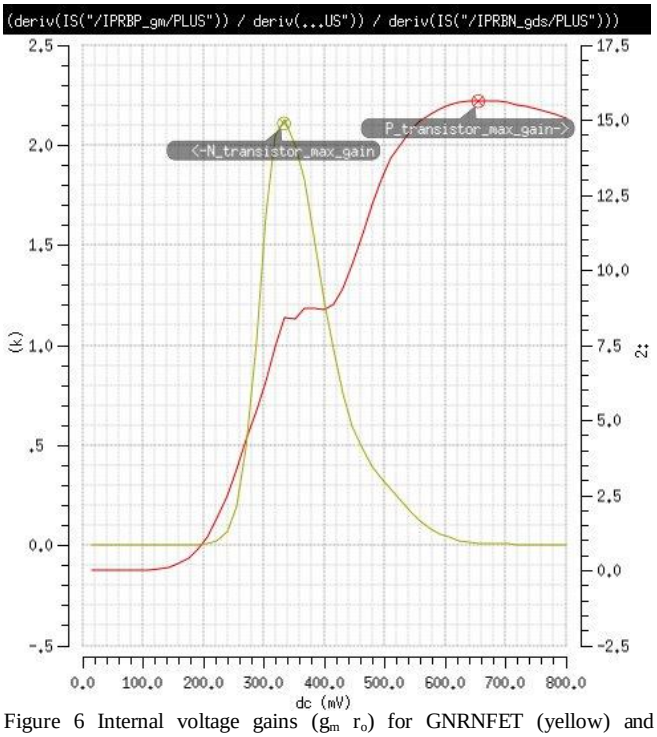

Figure 6 Internal voltage gains (g_m r_o) for GNRNFET (yellow) and GNRPFET (red) transistors.

To evaluate performance, we compared the speed, power consumption and area of similar circuits designed using GNRFETs and Silicon transistors.

The first circuit used for comparison is a voltage buffer designed using a single stage telescopic amplifier [15] shown in Figure 7. This circuit was biased in 10uA and drives a 10fF load capacitance. The simulations were used to determine loop gain, bandwidth and voltage range. The second circuit is the important comparator circuit, which is common in many mixed signal circuits. In particular the popular StrongARM latches were used for the simulations [16]. The particular implementation is shown in Figure 8. The comparators are clocked at a 100MHz speed. Both these circuits are designed for comparison and they are compared in terms of their speed and power consumption.

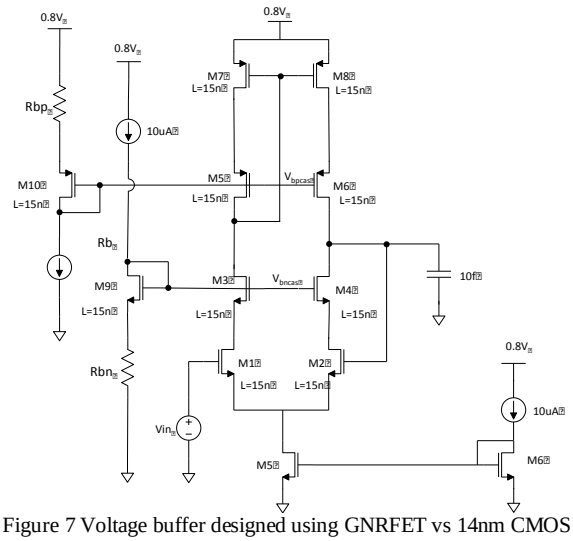

Figure 7 Voltage buffer designed using GNRFET vs 14nm CMOS transistors.

Even though mismatch and noise performances are important for both circuits they were not included in our

study. The main reason for this is the models not including noise and mismatch information. This is because noise and mismatch parameters are measured as a result of statistical analysis of measured data. Therefore using the models in consideration it is not possible to complete noise and Monte Carlo Simulations.

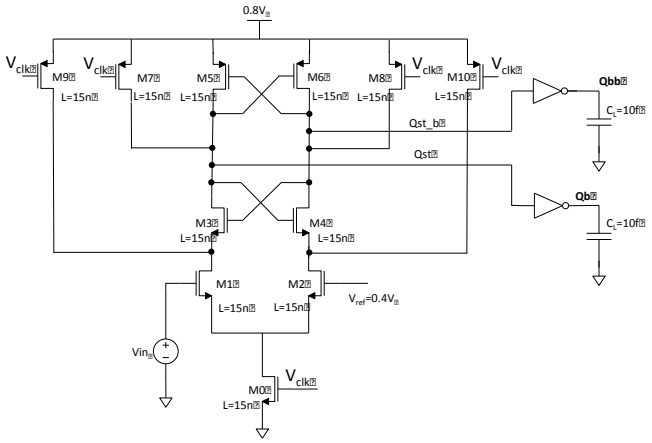

Figure 8 Comparator circuit implemented in GNRFET and 14nm CMOS devices

For area estimates an assumed 12nm S/D terminal widths are added onto the device channel lengths. Also 50%utilization is assumed so that the connections will increase the area consumption by an additional 50%.

IV. Simulations and Results

Tables 1 and 2 summarize the circuit performances obtained through simulations. Table 1 includes the performance results for the voltage buffer design. As can be seen from this table the same bias current consumption yields a 20% faster voltage buffer using Si CMOS transistors. One possible explanation for this advantage of Si FET devices over GNRFET devices can be the optimistic (high) mobility and (low) parasitic capacitance expectations in the devices assumed by the PTM models. Loop Gain DC value is 3dB larger for the Graphene implementation. This result is partly due to the unrealistically large DC gain of the GNRNFET devices. GNRPFET devices mainly dominate the DC gain of the graphene amplifier.

	Graphene	14nm Si
Bandwidth (GHz)	1.25	1.46
DC gain (dB)	29.89	27
Power Consumption(uA)	9.95	9.1
Area estimate (nm2)	50000	20000

Table 1 Comparison of voltage buffers designed using GNRFET and Si14nm FET devices

In terms of area consumption area estimate for both implementations the GNRFET's are implemented using gate arrays therefore have significant overhead. On the contrary the silicon devices can be built using custom layout and have reduced area overhead. As a result the area needed for Si circuits' are estimated to be less than half of the GNRFET implementations.

	Graphene	14nm Si
Output HL delay (ps)	60	61
Output LH delay (ps)	61	63
Power Consumption(uA)	6.6	2
Area estimate(nm2)	75000	30000

Table 2 Performance Comparison of comparators designed using GNRFET and Si14nm FET devices

As the result of the comparator simulations both implementations have a 60ps delay for the rising and falling edge transitions. The comparators are clocked at 100MHz speed. Meanwhile 14nm Si FET based implementations consume 60% lower average current. The current consumption is mainly during the regeneration phase when Vclk is high. The difference in power consumption is mainly due to the leakage current that the GNRNFET transistors exhibit when turned off. As mentioned before, we cannot complete comparator-offset analysis due to the lack of mismatch parameters.

V. Conclusion

In this study graphene nano ribbon transistors are used for mixed signal circuit design. Graphene based transistors have been used for design and simulations of logic gates and other digital circuits. On the contrary only single transistor amplifiers have been proposed in terms of analog mixed signal circuit design. To design the mixed signal circuits models for Graphene Nano ribbon based transistor are assumed. The attraction of these devices is the presence of a band gap present in 1D devices. With such a band gap nano ribbon based transistor can be used as electronic switches. As the mixed signal circuits to be used for comparison a voltage buffer and a comparator are implemented. These circuits are implemented using GNRFET transistors as well as 14nm Si FET devices. Comparing these implementations reveal that Si FET devices can realize 20% faster operation for voltage buffers while consuming speeds are comparable for StrongARM based comparators. Graphene power consumption is slightly larger. As a result graphene transistors can operate at comparable speed and power levels with their Si counterparts.

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BIOGRAPHIES

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From 2006 to 2010 he was a staff design engineer working at Broadcom Corp. working on data converters, analog mixed signal circuits, filters, sensor interfaces. From 2010 to 2014 he was a Sr. Design engineer at Silicon Laboratories Inc. working on RF circuits, Analog mixed signal circuits, power electronics and digital circuit design.

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