





## Modelling and Control of a Three-Level Diode-Clamped Medium Voltage Distribution Static Synchronous Compensator using Space Vector Pulse Width Modulation

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### Highlights

- Modelling of a grid-connected three-phase three-level diode-clamped converter based D-STATCOM.
- Utilization of space vector pulse width modulation technique.
- Reactive power compensation under fluctuating grid conditions.
- Performance analysis of D-STATCOM under voltage sags and swells occurring on the generation side.

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### Abstract

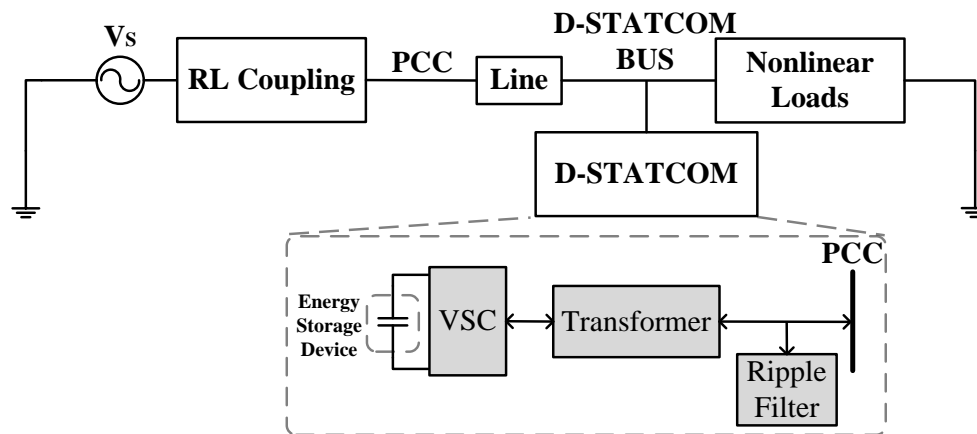
Efficient utilization of power networks under extreme voltage sags and swells and reducing the losses are widely recognized as the most important issues in energy industry. Power electronic converter based flexible AC transmission system (FACTS) devices play a significant role in power flow control, power quality improvement, voltage regulation and efficient energy utilization. Distribution static synchronous series compensator (D-STATCOM) is a FACTS device and it compensates for voltage sags and swells by injecting or absorbing reactive power to/from the power network. Modulation of D-STATCOMs is mostly based on pulse width modulation (PWM) techniques and space vector PWM (SV-PWM) is attracting considerable interest due to its better DC utilization and wide linear modulation range. In this paper, a three-level SV-PWM is suggested for the modulation of D-STATCOM which is based on a three-phase diode-clamped inverter (DCI). A grid connected three-phase power system feeding a 1 MW and 500 kvar load is designed in simulation environment and D-STATCOM is tested under voltage sags and swells occurring on the generation side. Results demonstrate that D-STATCOM successfully injects/absorbs reactive power to/from the system under fluctuating grid conditions.

## 1. INTRODUCTION

Utilization of power networks at the highest efficiency is increasingly becoming a vital factor with the increased loading conditions and cost of the power networks [1]. Extreme voltage sags, swells and dips; stability issues and high losses may be counted as some of the challenges that can be faced on a power network [2-4]. These challenges generally occur due to nonlinear and/or unbalanced loads and high impedance on distribution networks [5]. Power electronic converters are fast becoming a key instrument on power networks and their high speed and low cost make them more useful for power networks than traditional electromechanical devices [6]. The past decade has seen the rapid development of flexible AC transmission system (FACTS) devices and their utilization on power networks became inevitable [7]. Recently, FACTS devices are extensively utilized in power flow control [8], power quality improvement [9], voltage regulation [10], efficient energy utilization [11], harmonic mitigation [12, 13], damping power system oscillations and steady-state voltage stability enhancement [14-16]. FACTS devices can be mainly divided into two categories: Thyristor-based FACTS devices and self-commutated switches based FACTS devices [17]. Thyristor-based FACTS devices generally use line commutation and employ large energy storage elements whereas FACTS devices based on self-commutated switches utilize gate turn-off thyristors (GTOs) or insulated-gate bipolar transistors (IGBTs). Thyristor-controller reactor (TCR), thyristor-switched capacitor (TSC), static var compensator (SVC), thyristor-switched series capacitor (TSSC), thyristor-controlled series capacitor (TCSC) and thyristor-controlled phase angle regulator (TCPAR) are types of thyristor-based FACTS devices. On the other hand, static synchronous compensator

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(STATCOM) and static synchronous series compensator (SSSC) are major types of FACTS devices based on self-commutated switches. STATCOM is nothing but a shunt connected FACTS device [18]. STATCOMs have the ability to both absorb and generate reactive power. The major advantage of STATCOMs is that they can generate high reactive power output at low grid voltages [9]. A STATCOM along with a coupling transformer, an energy storage device and a converter is called as distribution static synchronous compensator (D-STATCOM) as seen in Figure 1. The central function of D-STATCOM in the power system is to regulate the voltage at point of common coupling (PCC) by injecting and absorbing reactive power to/from the system at a very high rate [19-21]. D-STATCOMs are also utilized in voltage support [22], excess power circulation [23], enhancing the photovoltaic (PV) installation capacity of distribution networks [24], reduction of fluctuations caused by PV systems [25] and reduction of voltage sags and swells [26-29].



**Figure 1.** Single line block diagram of D-STATCOM

Pulse width modulation (PWM) techniques are widely used in controlling D-STATCOMs. While a number of researchers use high frequency sinusoidal PWM (SPWM) [27, 30], some others use fundamental frequency selective harmonic elimination PWM (SHE-PWM) techniques [31-33] to control D-STATCOMs. Although SPWM is very simple to implement and SHE-PWM is very good at eliminating harmonics at the output of D-STATCOM, space vector PWM (SV-PWM) combines the advantages of both techniques. Popularity of SV-PWM to control D-STATCOMs increases among researchers due to its better DC utilization at high voltages, wide linear modulation range and ease of realization [34]. In [35], a two-level SV-PWM algorithm is developed and applied on STATCOM. It should be noted that a three-phase six-pulse VSI is utilized inside the STATCOM. A three-level SV-PWM algorithm is proposed in [36] for a diode-clamped inverter (DCI) based STATCOM. Despite this interest, no one to the best of the author's knowledge has studied the implementation of space vector PWM on D-STATCOM.

In this paper, a three-level space vector PWM for a DCI based D-STATCOM is proposed. Control of D-STATCOM is performed by SV-PWM technique. Designed system is tested under voltage fluctuations occurring on the generation side of the power system for different load configurations.

This paper proceeds as follows: Control technique of the D-STATCOM is investigated in Section 2. Section 3 deeply examines SV-PWM for three-phase three-level DCI. Simulation results are presented in Section 4 by observing the system behavior under voltage sags and swells that happen in grid. Finally, a brief discussion on the findings is presented in Section 5.

## 2. CONTROL OF D-STATCOM

In this section, control technique of D-STATCOM will be investigated. A detailed circuit diagram of D-STATCOM connected three-phase power system is shown in Figure 2. As seen a three-phase D-STATCOM is connected to the distribution side of the power system. A three-phase three-level DCI is utilized as voltage source converter in D-STATCOM. Exchange of reactive power between D-STATCOM

and AC system is held depending on the magnitude of the bus voltage of D-STATCOM ( $V_{STAT}$ ). If  $V_{STAT}$  is greater than the PCC voltage ( $V_{PCC}$ ), D-STATCOM supplies reactive power to AC system. If  $V_{STAT}$  is smaller than  $V_{PCC}$ , reactive power is absorbed by D-STATCOM from AC system.

A detailed control diagram of D-STATCOM is demonstrated in Figure 3. Firstly, D-STATCOM bus voltages for each phase ( $V_{STAT-A}$ ,  $V_{STAT-B}$ ,  $V_{STAT-C}$ ) are measured. Measurements are used by a phase-locked loop (PLL) circuit to extract the phase and frequency information of  $V_{STAT}$  voltages. Using the phase information, three-phase voltage and current signals are converted from  $abc$  reference frame to orthogonal direct-quadrature ( $dq$ ) frame to ease the control of the system. After this conversion, current values in  $dq$  axis are obtained ( $I_d$ ,  $I_q$ ). In addition to this, generated  $V_d$  and  $V_q$  signals are used to generate the magnitude of the AC voltage ( $V_{ac}$ ). Sum of the DC voltages of the capacitors ( $V_{dc}$ ) in the three-phase three-level DCI is compared and regulated to a predetermined DC voltage ( $V_{dc_{ref}}$ ) by a proportional-integrator (PI) controller in DC voltage regulator unit. Similarly,  $V_{ac}$  is regulated to a unity AC reference ( $V_{ac_{ref}}$ ) by a PI controller in AC voltage regulator unit. DC and AC voltage regulator units generate current references  $I_{d_{ref}}$  and  $I_{q_{ref}}$  respectively. Previously generated  $I_d$  and  $I_q$  values are regulated to  $I_{d_{ref}}$  and  $I_{q_{ref}}$  respectively in current regulator unit. Again, PI controllers are utilized and voltages in  $dq$  frame are produced ( $V_d$ ,  $V_q$ ). Finally, voltage references in  $abc$  frame are obtained in reference signal generation unit for each phase and they are sent to be processed in SV-PWM block. As a result of this operation, gating signals ( $S_a$ ,  $S_b$ ,  $S_c$ ) for the three-phase three-level DCI are produced. In the section that follows, SV-PWM algorithm for the three-phase three-level DCI will be deeply investigated.

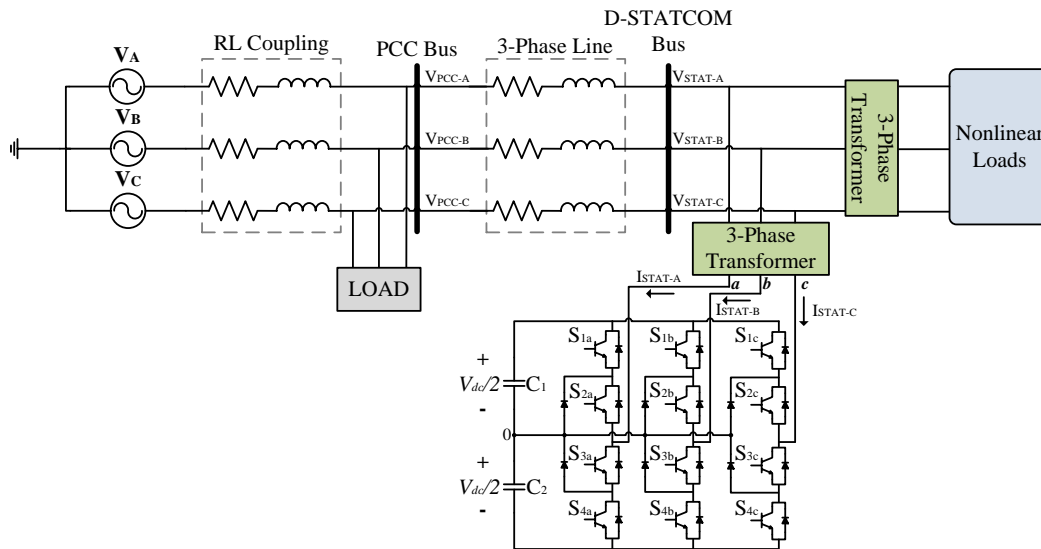


Figure 2. Detailed circuit diagram of D-STATCOM connected to a three-phase system

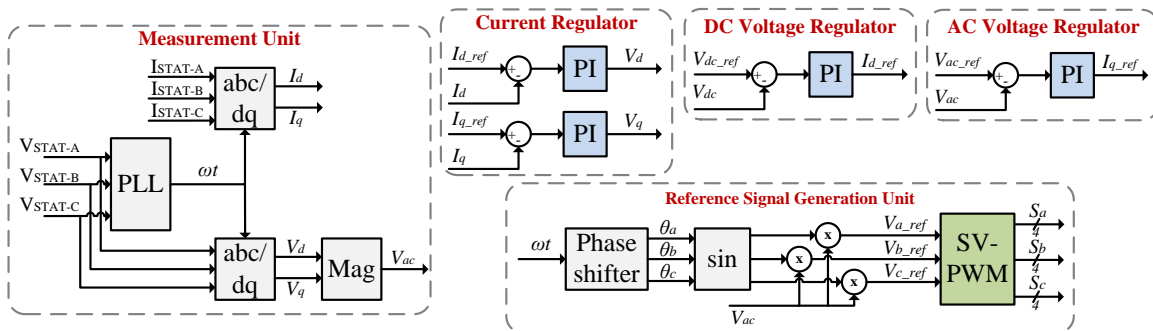


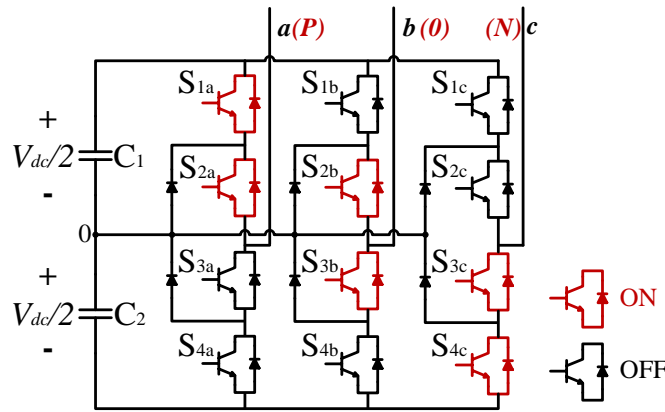
Figure 3. Block diagram for the control of D-STATCOM

### 3. THREE-LEVEL SPACE VECTOR PWM

In this section, SV-PWM algorithm for a three-phase three-level DCI will be investigated. Mainly in SV-PWM, three-phase voltages are converted to a voltage vector which has a fixed amplitude and rotates at an angular frequency of  $\omega = 2\pi f$  where  $f$  is the fundamental frequency. The three-phase three-level DCI is given in Figure 2. As seen, there are two DC capacitors with a neutral point between them and four power semiconductors in each phase along with two clamping diodes. Switching states for the single-phase of a three-phase three-level DCI are given in Table 1. As indicated, there are three possible switching states for a phase of the DCI. A visual demonstration of the switching states for a three-phase three-level DCI is given in Figure 4. Under the circumstances given in Figure 4, three-phase state of the DCI is  $P0N$ .

**Table 1.** Switching states for a single-phase three-level DCI

$S_{1x}$	$S_{2x}$	$S_{3x}$	$S_{4x}$	Phase voltage	Switching state
ON	ON	OFF	OFF	$+V_{dc}/2$	P
OFF	ON	ON	OFF	0	0
OFF	OFF	ON	ON	$-V_{dc}/2$	N



**Figure 4.** States of the three-phase three-level DCI

Three-phase switching states of DCI can be represented in a two-dimensional diagram using Clarke transformation [37]. The formula to convert three-phase output voltages ( $v_{a0}$ ,  $v_{b0}$ ,  $v_{c0}$ ) into two-dimensional vectors ( $v_\alpha$ ,  $v_\beta$ ) in  $\alpha\beta$  plane is as follows:

$$\vec{V} = v_a + jv_b = \frac{2}{3}(v_{a0}\vec{a}^0 + v_{b0}\vec{a}^1 + v_{c0}\vec{a}^2) \quad (1)$$

where  $\vec{a} = e^{j\frac{2\pi}{3}}$ .

Using Equation (1), 27 switching state space vectors of the three-phase three-level DCI are obtained as seen in Figure 5. As seen in Figure 5, there are 19 different state vectors. These state vectors can be divided into four main groups as large, medium, small and zero state vectors. Large state vectors ( $PNN$ ,  $PPN$ ,  $NPN$ ,  $NPP$ ,  $NNP$ ,  $PNP$ ) sets voltage of each phase of the DCI to  $+V_{dc}/2$  or  $-V_{dc}/2$ . Medium state vectors ( $P0N$ ,  $0PN$ ,  $NP0$ ,  $0NP$ ,  $PN0$ ,  $ONP$ ,  $PNO$ ) assign voltage of each phase of the DCI to different voltage levels as  $+V_{dc}/2$  or  $-V_{dc}/2$ . Small state vectors ( $P00$ ,  $0NN$ ,  $PPO$ ,  $00N$ ,  $NON$ ,  $OP0$ ,  $OPP$ ,  $N00$ ,  $00P$ ,  $NN0$ ,  $ON0$ ,  $POP$ ) connect at least one phase of the DCI to DC link while setting other phases to neutral point. Each state vector can be represented by two states. Zero state vectors ( $000$ ,  $NNN$ ,  $PPP$ ) assign each phase of the DCI to same DC link or the neutral point. It should be noted that since length of one edge of the hexagonal is  $2V_{dc}/3$ , magnitudes of large, medium and small state vectors are  $2V_{dc}/3$ ,  $V_{dc}/3$  and  $V_{dc}/3$  respectively. In addition state vectors, three-phase reference signals are also represented in two-dimensional  $\alpha\beta$  plane. The angle ( $\theta$ )

between reference vector  $V_{ref}$  and  $\alpha$  line determines the sector number that  $V_{ref}$  lies in. The relationship between  $\theta$  and sector number is given in Table 2.

As seen in Figure 5,  $V_{ref}$  should be within a circle and maximum magnitude of it is determined by the magnitude of medium state vectors. Taking into account only the first sector of the state vector diagram given in Figure 5 and normalizing all state vectors with small state vectors, diagram in Figure 6 is obtained. As seen, maximum value of normalized reference vector  $V_{ref,n}$  becomes  $\sqrt{3}$ . If  $V_{ref,n}$  gets greater than  $\sqrt{3}$ , overmodulation occurs. Figure 6 also demonstrates the regions within first sector and as seen, there are four regions for a single sector.

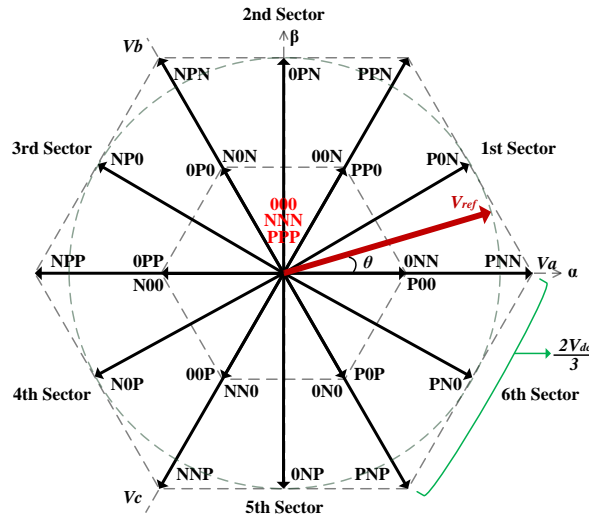


Figure 5. Space vector diagram of three-phase three-level DCI

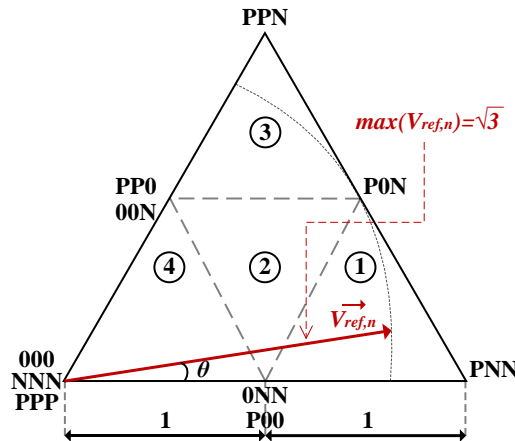


Figure 6. Regions within the first sector of the space vector diagram

Table 2. Sector determination with respect to  $\theta$

Angle criteria	Sector number
$0 \leq \theta < 60$	1
$60 \leq \theta < 120$	2
$120 \leq \theta < 180$	3
$180 \leq \theta < 240$	4
$240 \leq \theta < 300$	5
$300 \leq \theta < 360$	6

Space vector diagram given in Figure 5 is used to generate switching sequence and time of each state vector. For this reason, a widely used nearest-three-vector (NTV) modulation technique is utilized in this paper. NTV is more advantageous than other SV-PWM techniques in terms of good quality of output voltage and low switching frequency [38]. In this technique, the nearest three state vectors ( $\vec{V}_1, \vec{V}_2, \vec{V}_3$ ) to reference vector are determined at that sampling time and switching is accomplished by these vectors. Switching times ( $T_1, T_2, T_3$ ) of these three vectors are determined by their duty cycles ( $d_1, d_2, d_3$ ). Assuming that  $T_s$  is the sampling period, switching times of  $\vec{V}_1, \vec{V}_2$  and  $\vec{V}_3$  become  $d_1T_s, d_2T_s$  and  $d_3T_s$  respectively. To sum up, switching times of  $\vec{V}_1, \vec{V}_2$  and  $\vec{V}_3$  are calculated as follows:

$$\begin{aligned} \vec{V}_{ref}T_s &= \vec{V}_1T_1 + \vec{V}_2T_2 + \vec{V}_3T_3, \\ T_s &= T_1 + T_2 + T_3, \\ 1 &= d_1 + d_2 + d_3. \end{aligned} \quad (2)$$

Therefore, the next thing to do is to calculate the duty cycles for the corresponding state vectors at that time instant. Since  $V_{ref,n}$  could be in any region at any time instant, duty cycle calculations should be performed for all regions of each sector. Taking into account the fourth region of the first sector,  $\vec{m}_1$  and  $\vec{m}_2$  are the two components of  $V_{ref,n}$  as seen in Figure 7.  $\vec{m}_1$  and  $\vec{m}_2$  are calculated as follows:

$$\begin{aligned} m_1 &= V_{ref,n} \left( \cos(\theta) - \frac{\sin(\theta)}{\sqrt{3}} \right), \\ m_2 &= 2V_{ref,n} \frac{\sin(\theta)}{\sqrt{3}}. \end{aligned} \quad (3)$$

In the fourth region of sector 1,  $\vec{m}_1$  and  $\vec{m}_2$  directly determine  $d_1$  and  $d_2$  respectively. Combining this with Equation (2) and Equation (3),  $d_1, d_2$  and  $d_3$  are obtained as follows:

$$\begin{aligned} d_1 &= m_1 = V_{ref,n} \left( \cos(\theta) - \frac{\sin(\theta)}{\sqrt{3}} \right), \\ d_2 &= m_2 = 2V_{ref,n} \frac{\sin(\theta)}{\sqrt{3}}, \\ d_3 &= m_3 = 1 - V_{ref,n} \left( \cos(\theta) - \frac{\sin(\theta)}{\sqrt{3}} \right) - 2V_{ref,n} \frac{\sin(\theta)}{\sqrt{3}}. \end{aligned} \quad (4)$$

**Table 3.** Duty cycle calculations for each region of sector 1

Region	Conditions	Duty Cycles
1	$m_1 > 1$	$d_1 = d_{PNN} = m_1 - 1$ $d_2 = d_{P0N} = m_2$ $d_3 = d_{0NN/P00} = 2 - m_1 - m_2$
2	$m_1 \leq 1$ $m_2 \leq 1$ $m_1 + m_2 > 1$	$d_1 = d_{0NN/P00} = 1 - m_1$ $d_2 = d_{00N/PP0} = 1 - m_2$ $d_3 = d_{P0N} = m_1 + m_2 - 1$
3	$m_2 > 1$	$d_1 = d_{P0N} = m_1$ $d_2 = d_{PPN} = m_2 - 1$ $d_3 = d_{00N/PP0} = 2 - m_1 - m_2$
4	$m_1 \leq 1$ $m_2 \leq 1$ $m_1 + m_2 \leq 1$	$d_1 = d_{0NN/P00} = m_1$ $d_2 = d_{00N/PP0} = m_2$ $d_3 = d_{000/NNN/PPP} = 1 - m_1 - m_2$

Duty cycle calculations depending on the region  $V_{ref,n}$  lies in are demonstrated in Figure 7 and summarized in Table 3. Similar analysis can be held for other sectors. Finally, switching sequences and timings for all regions of sector 1 are given in Figure 8. Again, switching sequences are determined for all sectors in a similar fashion. In the next section, simulation results will be presented for various cases.

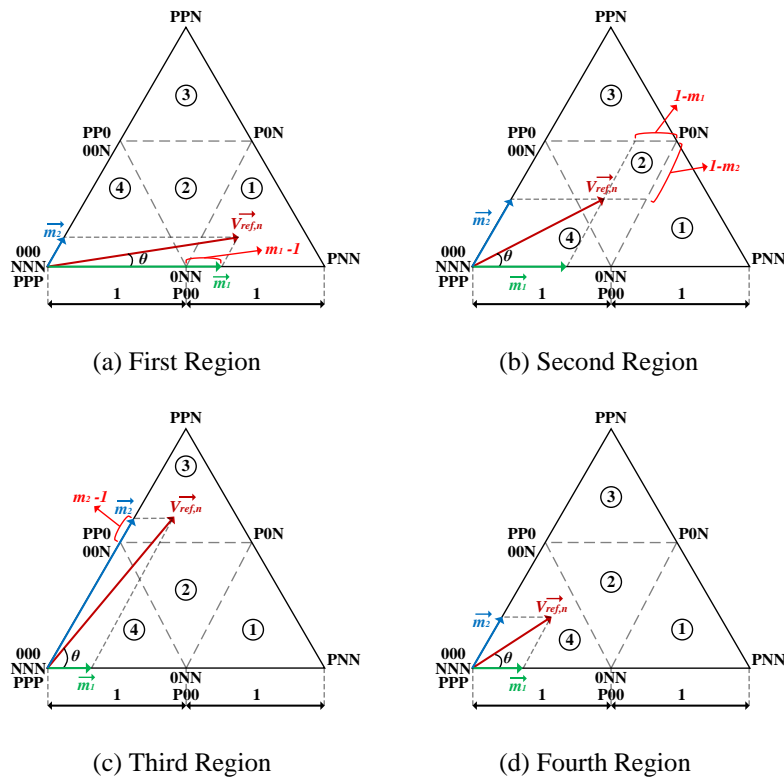


Figure 7. Duty cycle calculations for all regions of sector 1

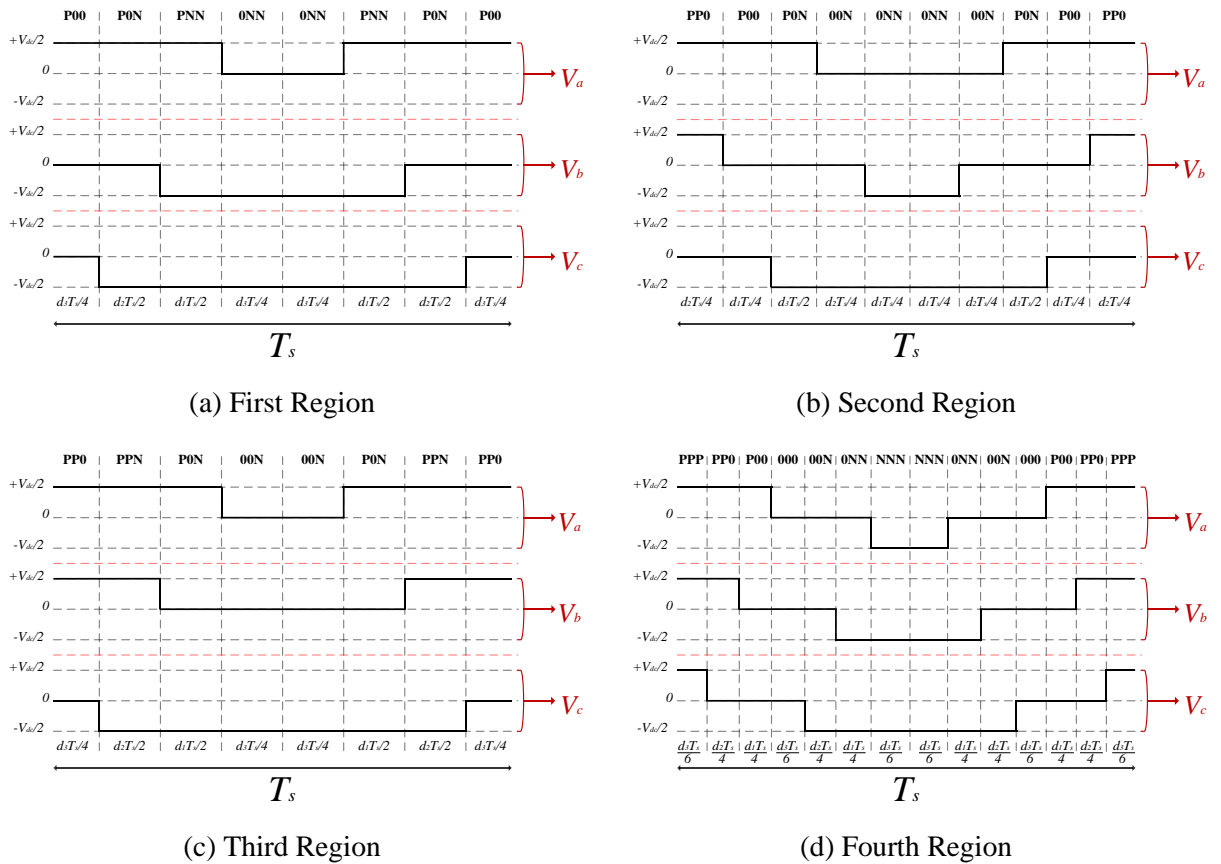


Figure 8. Switching sequences for each region of sector 1 at each sampling time ( $T_s$ )

#### 4. SIMULATION STUDIES

In this section, the whole power system including a three-phase three-level DCI based D-STATCOM given in Figure 2 is modelled in simulation environment. Behaviour of the system is observed under voltage sags and swells occurring on the grid side and different types of loads are utilized on load side. Design parameters for each part of the power system are given in detail in Table 4. Grid voltage and frequency is 25 kV and 60 Hz respectively. Fundamental and switching frequencies of DCI are selected as 60 Hz and 3600 Hz respectively. At the load side, R, RL and RC type loads are employed in different simulation runs. Active and reactive power requirements of each type of load are given in Table 4. Simulations are run for 0.15 s and a voltage sag of 20 % with respect to per unit value of the voltage occurs at each phase of the grid at  $t = 0.03$ s. At the  $t = 0.08$ s, a voltage swell of 15 % with respect to per unit value of the voltage occurs at each phase of the grid. Amplitude of the grid voltage returns to per unit value at 0.13s in the system. Controller parameters of AC voltage, DC voltage and current regulator are given in Table 5.

**Table 4. General design parameters**

Design Part	Parameter Name	Value
Grid	Grid Voltage (L-L) ( $V_{grid}$ )	25 kV
	Grid Frequency ( $f_{grid}$ )	60 Hz
RL Coupling	Coupling Resistance ( $R_{coup}$ )	62.5 $\Omega$
	Coupling Inductance ( $L_{coup}$ )	1.66 H
3-Phase Line	Positive and Zero Sequence Resistances ( $R_{pos}, R_0$ )	0.12, 0.39 $\Omega$ /km
	Positive and Zero Sequence Inductances ( $L_{pos}, L_0$ )	1.05, 2.70 mH/km
	Positive and Zero Sequence Capacitances ( $C_{pos}, C_0$ )	1.13, 5.34 nF/km
	Line Length	21 km
Diode-Clamped Inverter (DCI)	DC Capacitors ( $C_1, C_2$ )	20 $\mu$ F
	Reference DC voltage ( $V_{dc,ref}$ )	2600 V
	Fundamental Frequency ( $f_{fund}$ )	60 Hz
	Switching Frequency ( $f_{sw}$ )	3600 Hz
STATCOM Transformer	Connection Type	$\Delta$ - Y
	Nominal Power and Frequency ( $P_{nom}, f_{nom}$ )	1 MW, 60 $\sqrt$ Hz
	Winding Voltages ( $V_1, V_2$ )	1300 V, 25/ 3 kV
Load Transformer	Connection Type	$\Delta$ - Y
	Nominal Power and Frequency ( $P_{nom}, f_{nom}$ )	6 MW, 60 Hz
	Winding Voltages ( $V_1, V_2$ )	25 kV, 600 V
Load	Nominal Voltage and Frequency ( $V_{nom}, f_{nom}$ )	600 V, 60 Hz
	Active Power ( $P$ )	1 MW
	Inductive Reactive Power ( $Q_L$ )	500 kvar, 0 var
	Capacitive Reactive Power ( $Q_C$ )	0 var, 500 kvar
Sampling	Sampling frequency ( $f_{samp}$ )	100 kHz

**Table 5. Controller parameters**

Controller Part	Parameter Value
AC Voltage Regulator	$K_p = 0.55$
	$K_i = 2500$
DC Voltage Regulator	$K_p = 0.5$
	$K_i = 10$
Current Regulator	$K_p = 0.75$
	$K_i = 200$

Figure 9 shows per unit value of the voltage on each bus on the power system. As seen, voltage sags and swells occur on the grid. Figure 10 demonstrates the three-phase voltage and current signals on D-STATCOM bus. As seen in Figure 10b, D-STATCOM currents go to zero when PCC and D-STATCOM voltages are almost equal to each other.

Figure 11a shows injected/absorbed reactive power to/from the power system by D-STATCOM. As seen, when voltage sag occurs on the grid side,  $V_{PCC}$  becomes smaller than  $V_{STAT}$  and reactive power is injected to the system by D-STATCOM. Under these circumstances D-STATCOM works in capacitive mode. However, when voltage swell occurs on the grid side  $V_{PCC}$  becomes greater than  $V_{STAT}$  and reactive power is absorbed from the system by D-STATCOM. At these time instants, operating mode of the D-STATCOM is called as inductive mode.



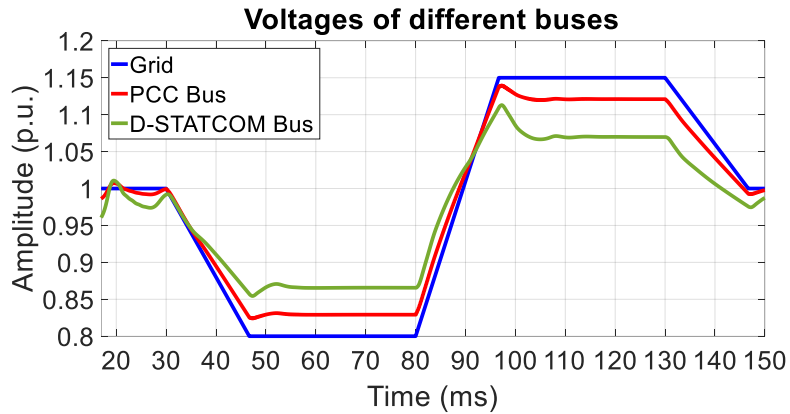
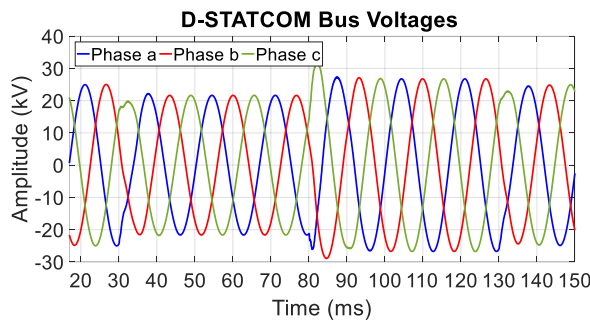
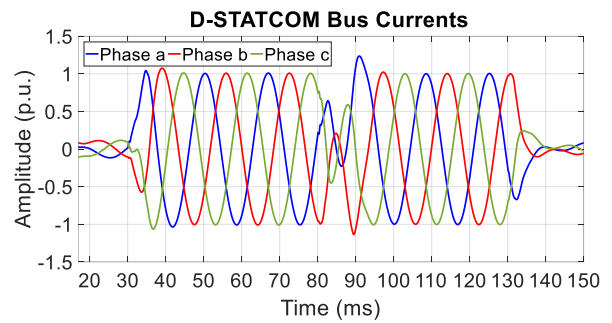


Figure 9. Voltages on different buses on the system

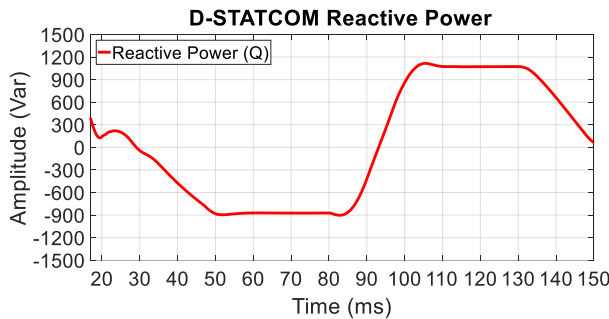


(a) D-STATCOM Bus Voltage

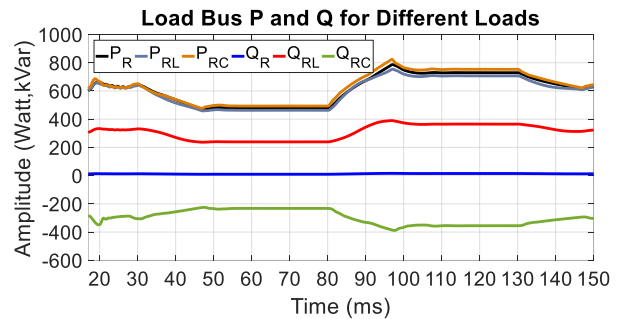


(b) D-STATCOM Bus Current

Figure 10. Voltage and current of each phase on D-STATCOM bus

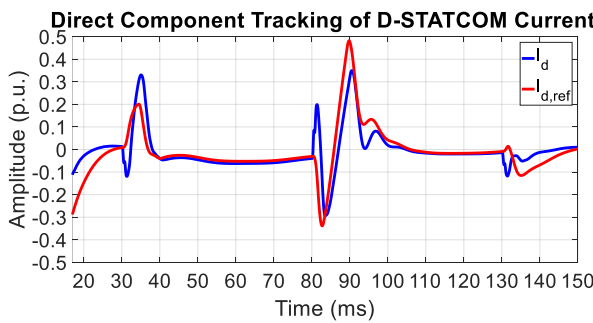


(a) D-STATCOM Reactive Power

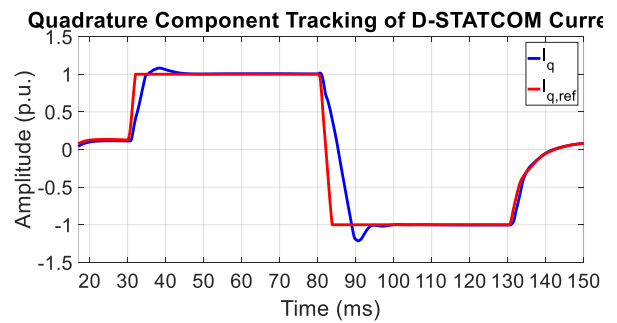


(b) Active and Reactive Power on the Load Bus

Figure 11. a) Reactive power injected/absorbed to/from the system by D-STATCOM, b) and active and reactive power on the load bus for different loads



(a) Direct Component



(b) Quadrature Component

Figure 12. Tracking performances for direct and quadrature component of D-STATCOM current

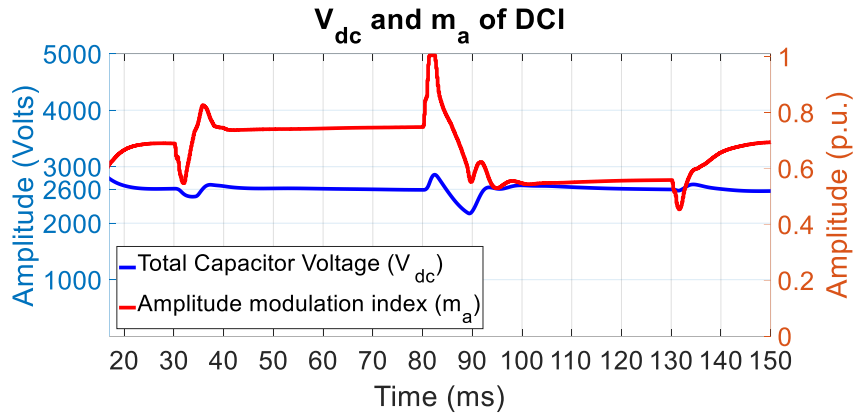
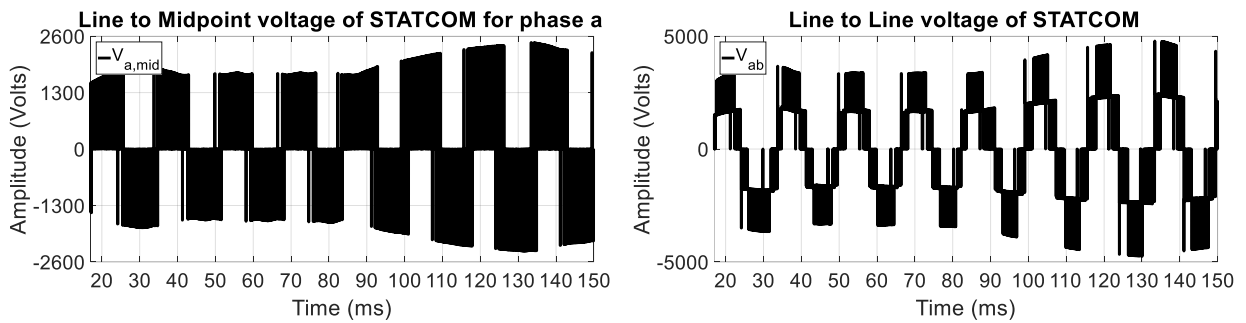
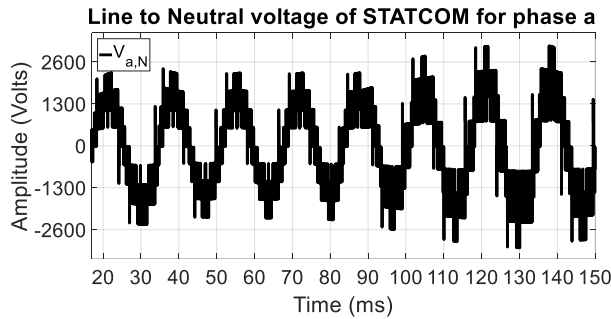


Figure 13. Total capacitor voltage  $V_{dc}$  and amplitude modulation index  $m_a$  of the DCI



(a) L-Midpoint Voltage for Phase a

(b) L-L Voltage between Phase a and Phase b



(c) L-N Voltage for Phase a

Figure 14. Output voltages of D-STATCOM

Table 6. THD<sub>50</sub> values of D-STATCOM voltages and currents obtained at capacitive mode (at  $t = 60$  ms) and inductive mode (at  $t = 110$  ms)

D-STATCOM Mode	$V_{L-mid}$	$V_{L-L}$	$V_{L-N}$	$I_L$
Capacitive	24.05 %	14.73 %	12.62 %	4.02 %
Inductive	41.83 %	23.06 %	22.59 %	5.73 %

Active and reactive power on the load bus is demonstrated in Figure 11b for different loads. As seen, active power remains almost the same for all cases, however, reactive power changes depending on the demand of the load and injected/absorbed power by D-STATCOM. To observe the performance of the current controllers, measured and reference direct and quadrature components of D-STATCOM current are compared to each other in Figure 12. It can be seen that PI controller shows better performance on tracking

quadrature component than direct component. It is because while quadrature component shows a step behaviour, direct component demonstrates a fluctuating behaviour. Nonetheless, it can be stated that current regulator can successfully track reference direct and quadrature components.

Figure 13 demonstrates total capacitor DC voltage and amplitude modulation index of DCI. It is seen in Figure 13 that DC voltage regulator achieves to keep DC voltage of the DCI at previously reference DC voltage ( $V_{dc,ref} = 2600V$ ). As indicated in Figure 13,  $m_a$  of the DCI changes in time and shows a stable performance in capacitive and inductive modes. Finally, D-STATCOM line to midpoint voltage ( $V_{L-mid}$ ) for phase a, line to line voltage ( $V_{L-L}$ ) between phase a and phase b, line to neutral voltage ( $V_{L-N}$ ) for phase a are demonstrated in Figure 14a, Figure 14b and Figure 14c respectively. Note that, neutral point is generated by connecting a balanced Y-connected RL load at the output of the DCI. Total harmonic distortion ( $THD$ ) values of  $V_{L-mid}$ ,  $V_{L-L}$ ,  $V_{L-N}$  and line current of the D-STATCOM ( $I_L$ ) are given in Table 6 for both capacitive and inductive mode of operation. Note that  $THD$  values are calculated using the first 50 harmonics and it is called as  $THD_{50}$ . It is observed that better  $THD_{50}$  values are obtained in capacitive mode for all parameters.

## 5. CONCLUSION

In this paper, a three-phase three-level DCI based D-STATCOM is designed by utilizing SV-PWM as the modulation technique. Firstly, control part of D-STATCOM is examined. Types and jobs of all controllers in the control diagram are explained. Direct and quadrature components of voltage and current are fed to SV-PWM block. Secondly, a three-level SV-PWM is presented. Here, the states of the DCI and space vector diagram are deeply investigated. Each sector of the space vector diagram is divided into four regions. Duty cycle calculations and switching diagrams are presented for all regions. Finally, a three-phase power system which includes a three-level D-STATCOM modulated by SV-PWM is designed in simulation environment. Behaviour of the system is observed under voltage sags and swells occurring on the grid side for different load configurations. It is inferred that D-STATCOM successfully injects/absorbs reactive power to/from the system depending on the condition.

## CONFLICTS OF INTEREST

No conflict of interest was declared by the authors.

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