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ON THE DESIGN OF NEW CMOS DO-OTA TOPOLOGIES PROVIDING HIGH OUTPUT IMPEDANCE AND EXTENDED LINEARITY RANGE

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ABSTRACT

In this paper, new realization techniques to enhance the performance of the CMOS differential output transconductance amplifiers (DO-OTAs) are proposed by combining the high-performance input and output stages given in the literature. The circuits proposed exhibit higher linearity and input signal range compared to the conventional counterparts. The advantage provided by the circuits proposed is demonstrated by SPICE simulations on current mode filters. The results prove that the new circuits exhibit a better performance for the input linearity and for the output impedance.

Keywords: *DO-OTA, transconductance, linearity, current mode circuits, filters*

1. INTRODUCTION

The current-mode analogue circuits employing active elements such as OTAs, current conveyors, DO-OTAs, DO-CCIIs, FTFNs play an important role in the IC design, since these active elements exhibit greater linearity, wider bandwidth and wider dynamic range over the voltage mode counterparts. The operational transconductance amplifier (OTA) is the oldest and frequently used circuit among the current-mode circuits. [1-12].

However, actual OTA and DO-OTA realization circuits exhibit some important drawbacks such as the finite output resistance, limited bandwidth and limited input linearity range. The finite output resistance is parallel to the load capacitor and causes a lossy integration, thus generating filtering errors. Therefore very high output impedance output stages are required both to enable filtering at low frequencies and to reduce filtering errors. Some works were performed for this purpose and appeared in the literature [1, 2, 5, and 9]. Another drawback of the OTAs and DO-OTAs is the limited input voltage range, which influences seriously the device linearity. Several works were performed in the last twenty years to overcome this shortcoming, new topologies to replace the conventional differential input stages are proposed [3,10,11,12]. The aim of this paper is to propose a high performance CMOS DO-OTA structure combining the high performance input and output stage properties.

2. DO-OTA DEFINITIONS

The circuit symbol of the DO-OTA (dual-output operational transconductance amplifier) is given in Figure 1a.

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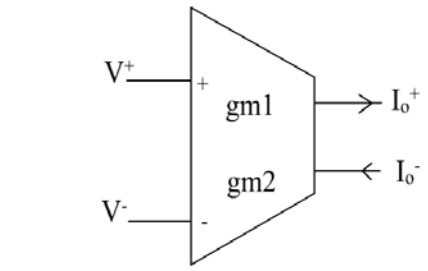
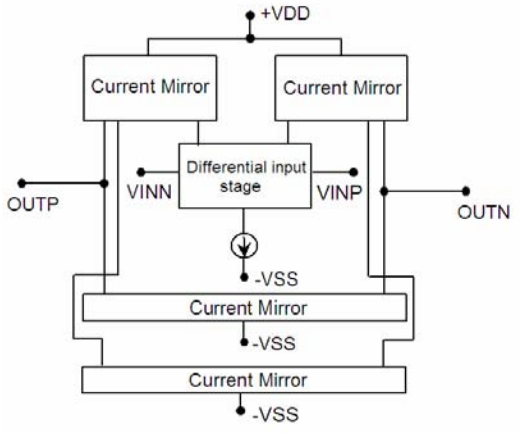


(a)



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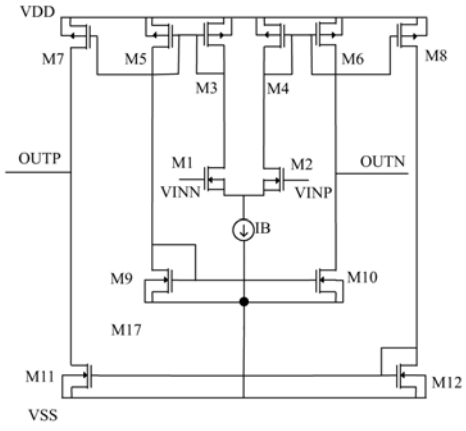


(c)

Figure 1 a) Circuit symbol of the DO-OTA, **b)** Realization of DO-OTA **c)** simple CMOS realization: symmetrical CMOS DO- OTA.

Ideally, DO-OTA is assumed as an ideal voltage controlled current source and can be described by following equations.

$$I_o^+ = g_{m1}(V^+ - V^-) \quad I_o^- = g_{m2}(V^- - V^+) \qquad (1)$$

Generally, the transconductances of the DO-OTAs are chosen as $g_{m1}=g_{m2}$ similar to the topologies described in this work. For some applications unequal $g_{m1}=g_{m2}$ values are obtained by taking different width and length values for MOS transistors of the output stages. Figure 1b illustrates the realization of the DO-OTA. From Figure 1b it can be easily observed that the dual-output operational transconductance amplifier consists of two main blocks, namely the differential input stage and the output stage. A simple CMOS realization circuit is shown in Figure 1c. Note that several works were performed to enhance the performance of input and output stages which appear recently in the literature [3, 4, 8, 9, 10, 11, and 12].

3. PROPOSED TOPOLOGIES

From the equation (1), it can be easily observed that the relation between input voltage and output current is linear for ideal case. But it is a well-known fact that this relationship is not linear in real world. In today's world, the linearity is an important subject in telecommunications area. So circuits must be very linear to have the best performance.

To achieve a linear relationship between input differential voltage and output current in a specified range, linearization techniques for input cells are proposed in the literature. Some of these circuit topologies will be summarized in the following.

On the other hand, another limiting factor for OTA performance is the output impedance. To provide an extended performance, the circuits must exhibit high output resistances [1].

To increase the output resistance some works were performed, high performance output stages were given in previous works by Zeki and Kuntman [1]. The output stage is realized by the use of high-output-impedance current mirrors [1, 2]. Furthermore it was demonstrated that this type output stage exhibits improved output characteristics compared to the conventional circuits constructed with cascode-current mirrors. The output stage achieves a much larger R_{out} and therefore a much larger DC gain with respect to its classical cascode counterpart while keeping mirroring precision and GBW high.

In this paper, new CMOS DO-OTA structures are proposed by combining the high-performance input and output stages given in the literature.

The enhanced performance of the circuits proposed was demonstrated by SPICE simulation results of application examples.

Input stages

To compare DO-OTA linearized input stages, one classical input stage and four other linearised input stages are given at this work. The difference between these circuits is given by total harmonic distortion (THD) analysis [8].

Conventional input stage: The conventional input stage for an OTA circuit is the differential pair illustrated in Figure 2.

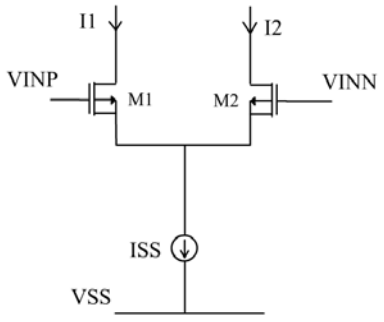


Figure 2. Differential pair

If we ignore the channel-length modulation and the body effect of MOSFETs, the current-voltage relationship is,

$$I_{D1}=\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_1[V_{GS1}-V_{th}]^2 \quad I_{D2}=\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)_2[V_{GS2}-V_{th}]^2 \tag{2}$$

Differential input signal can be defined as,

$$\Delta V_I = V_{INP} - V_{INN} = V_{GS1} - V_{GS2} \tag{3}$$

If we combine the equations (2) and (3) we achieve,

$$\Delta I_D = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)\Delta V_I \sqrt{\frac{2I_{SS}}{\mu C_{ox}\left(\frac{W}{2L}\right)}-(\Delta V_I)^2} \tag{4}$$

The equation (4) is valid only for the signals that are,

$$\Delta V_I \le \sqrt{\frac{2I_{SS}}{\mu C_{ox}\left(\frac{W}{L}\right)}} \tag{5}$$

But if the input signal is larger than this limit, the conductivity of one of the input MOSFETs become larger than the other and current flows from this MOSFET and becomes $\Delta I_D = I_{SS}$.

The transconductance of the circuit is given by,

$$G_m = \sqrt{I_{SS}\mu C_{ox}\left(\frac{W}{L}\right)} \tag{6}$$

Nedungadi input circuit: One of the most popular linearized input circuits is Nedungadi's input circuit illustrated in
Figure **3** [3]. The principle of this linearization technique is based on insertation of a constant voltage source between the input pairs.

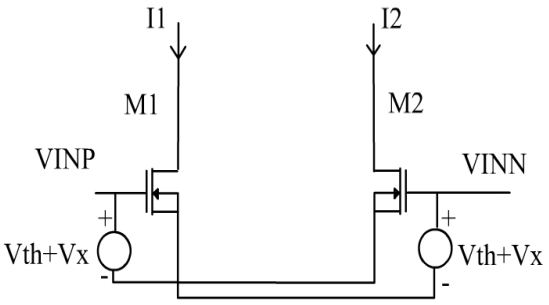


Figure 3 Nedungadi-Visvanathan input circuit

From
Figure 3 we have,

$$I_1 = k(V_x + \nu)^2 \tag{7}$$

$$I_2 = k(V_x - \nu)^2 \tag{8}$$

where $k=\frac{\mu C_{ox}}{2}\left(\frac{W}{L}\right)$. The differential output current is calculated as

$$i = I_1 - I_2 = 4kV_x\nu \tag{9}$$

where a transconductance of $g_m = 4kV_x$ is obtained.

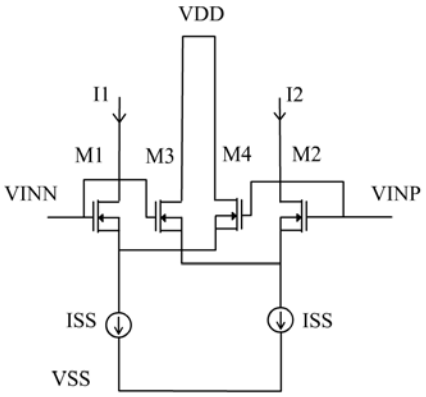


Figure 4 Practical Nedungadi-Visvanathan input cell

The practical realization of the circuit is given in **Figure 4**. The transistors M_3 and M_4 are n times wider than M_1 and M_2 and all transistors have same lengths. If we describe $V_b = \sqrt{\frac{I}{k}}$ and $x = \frac{\nu}{V_b}$, $y = \frac{i}{I}$ we obtain the following equations,

$$y = \frac{i}{I} = \frac{i_1 + i_2}{I}, \quad \nu = V_1 - V_2, \tag{10}$$

$$\alpha = \frac{4n}{n+1}, \quad \beta = \frac{n}{(n+1)^2}, \quad \gamma = \frac{n(n-1)}{(n+1)^2} \tag{11}$$

The normalized output current can be written as[2],

$$y = \alpha x\sqrt{1-\beta x^2}, \qquad |x| \le \sqrt{\frac{n+1}{n}} \tag{12}$$

$$y = 1 + \gamma x^2 + \alpha|x|\sqrt{1-\beta x^2}, \qquad \sqrt{\frac{n+1}{n}} \le |x| \le \sqrt{n+1} \tag{13}$$

$$y = (n+1)\,\mathrm{sgn}(x), \qquad |x| > \sqrt{(n+1)} \tag{14}$$

Cross-coupled input circuit: The main idea of this linearization technique shown in Figure 5 is the same as Nedungadi's input circuit. This time, the gate-source voltageV_{GS} of MOS transistors provide a constant voltage source. But the drawback of this circuit is the requirement of extra transistor level. The realization of circuit can be seen from

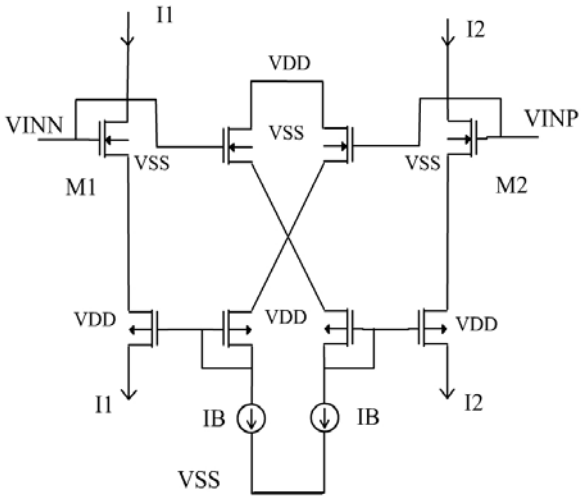


Figure 5 Cross coupled input circuit

The related current-voltage relations are given by:

$$I_{D1} = k(V_{GS1} - V_{th})^2 \tag{15}$$

$$I_{D2} = k(V_{GS2} - V_{th})^2 \tag{16}$$

Then we achieve the differential current,

$$\Delta I_D = I_{D1} - I_{D2} = k(V_{GS1} + V_{GS2} - 2V_{th})\left(\frac{V_{GS1} - V_{GS2}}{2}\right) \tag{17}$$

Assuming $V_b = (V_{GS1} + V_{GS2} - 2V_{th})$, we have

$$\Delta I_D = 2\beta V_b \nu \tag{18}$$

Krummenacher input circuit: This technique is based on the linearization by emitter resistors. From bipolar versions of amplifiers this is a common way for linearization. In CMOS circuits these resistors are realized by the use of MOS transistors to achieve smaller chip with reduced matching problems. The circuit can be seen in Figure 6.

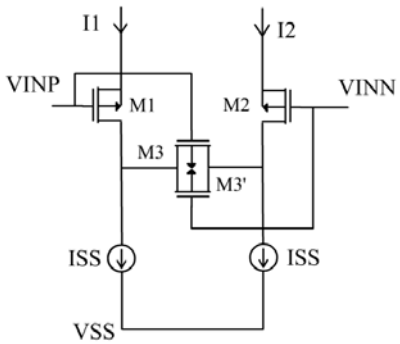


Figure 6 Krummenacher's input circuit

If M3 and M3' are not saturated, we have

$$I_{D3} = \mu C_{ox} \frac{W}{L}\left[(V_1 - V_{S2} - V_{th})(V_{S1} - V_{S2}) - \frac{(V_{S1} - V_{S2})^2}{2}\right] \quad (19a)$$

$$I_{D3'} = \mu C_{ox} \frac{W}{L}\left[(V_2 - V_{S2} - V_{th})(V_{S1} - V_{S2}) - \frac{(V_{S1} - V_{S2})^2}{2}\right] \quad (19b)$$

And from Kirchoff's law,

$$I_1 - I - I_{SS} = 0, \qquad I_2 + I - I_{SS} = 0 \quad (20)$$

are achieved. If we define

$$a = 1 + \frac{\beta_1}{4\beta_3}, \quad v = g_{m0}, \quad i = \frac{\Delta I_D}{I_{SS}}, \quad g_{m0} = \frac{\partial \Delta I_D}{\partial \Delta V_i},$$

we achieve the following equations:

$$i = v\sqrt{1 - \frac{v^2}{4}}, \quad g_{m0} = \left.\frac{\partial \Delta I_D}{\partial \Delta V_i}\right|_{v=0} = \frac{I_{SS}}{a(V_{GS} - V_{th})_{M1}} \quad (21)$$

If M3 and M3' are at saturation region,

$$|v| = \left|\frac{g_{m0} v}{I_{SS}}\right| > V_1 = \sqrt{\frac{a^2 + a + 0{,}5}{a^4 + 0.25}} \quad (22)$$

gives the linearity region. At this time output current equation is,

$$i = \pm \frac{\left[av\sqrt{4a - 2} \pm \sqrt{4a - 1 - a^2 v^2}\right]}{(4a - 1)^2} \quad (23)$$

And maximum output current can be found from equation 24.

$$|v| = \left[\frac{g_{m0} v}{I_{SS}}\right] = V_2 = \frac{\sqrt{4a - 2}}{a} \quad (24)$$

The results of DO-OTA circuits are at Chapter 4.

Output stages

To achieve best performance from a DO-OTA circuit, an output stage with a very high output resistance is necessary. Two different CMOS DO-OTA structures employing conventional differential pairs and formerly proposed output stages are given in Figures 7 and 8. The CMOS DO-OTA circuit of Figures 7 is proposed in a previous work by Zeki and Kuntman [1]. Note that the output stage is constructed with regulated cascade current sources to increase the output resistance. However, the input stage is a conventional differential pair consisting of the MOS transistors M1, M2, MLA, and MRA which exhibits a limited input range.

A further DO-OTA structure employing also a conventional differential pair and a newly proposed output stage is shown in Figures 8. The output stage is derived in the frame of this work from a NMOS single ended version given in a previous work. Replacing the conventional input stages with the linearized input stages described above, new high-performance CMOS DO-OTA topologies are proposed.

High-performance DO-OTA circuits

Using the high performance input and output stage properties new high performance CMOS DO-OTA structures are obtained. For this reason three different linearization techniques and two different output stages described above are combined with each other which results in six different DO-OTA circuits. Note that the input differential pairs in Figure 7 and 8 are constructed with PMOS transistors. To extend the input linearity range of the DO-OTAs the input differential pair is replaced with Nedungadi-Visvanathan, Krummenacher and cross-coupled input stages, respectively. Note that the input differential pairs in Figure 7 and 8 are constructed with PMOS transistors. Therefore, the NMOS and PMOS transistors in Nedungadi-Visvanathan, Krummenacher input stages are interchanged to provide this replacement. For the cross-coupled input stage the lower terminals are used to drive the output stage. Two of the DO-OTA structures proposed are illustrated in Figures 9 and 10. The others are not given for space reasons. The high performance DO-OTA employing the output stage of Figure 7 and Nedungadi-Visvanathan input stage is shown in Figure 9. Figure 10 illustrates the CMOS DO-OTA employing the output stage of Figure 8 and Krummenacher input stage. The performance of the six topologies proposed are investigated simulations and given briefly in the next section.

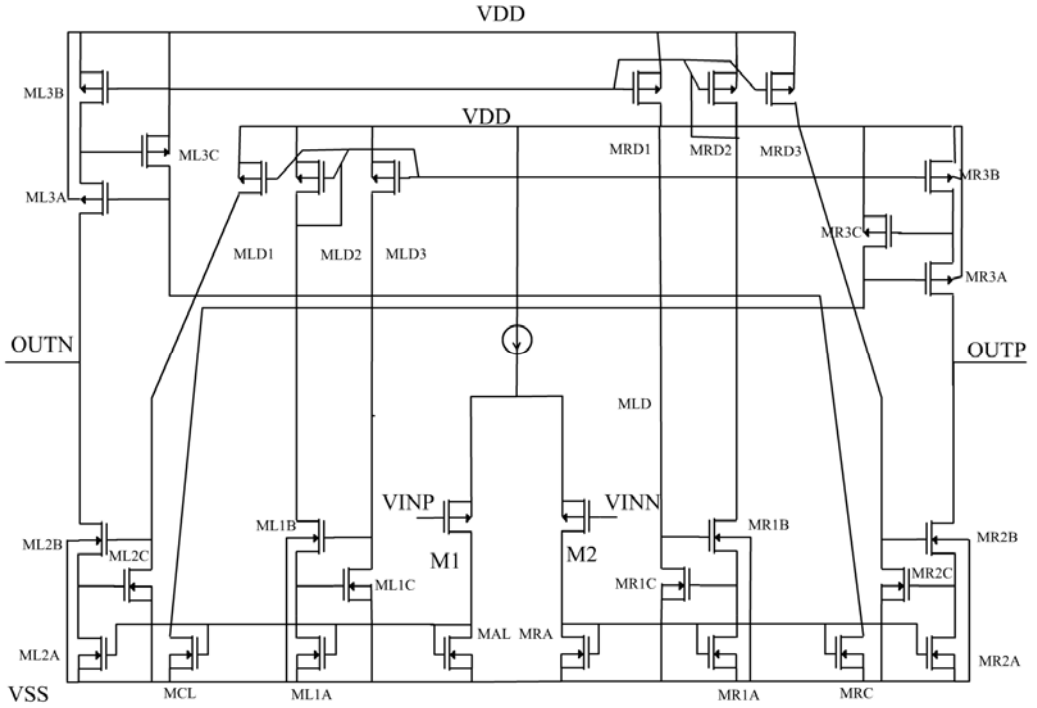


Figure 7 Regulated cascode stage (RGC)

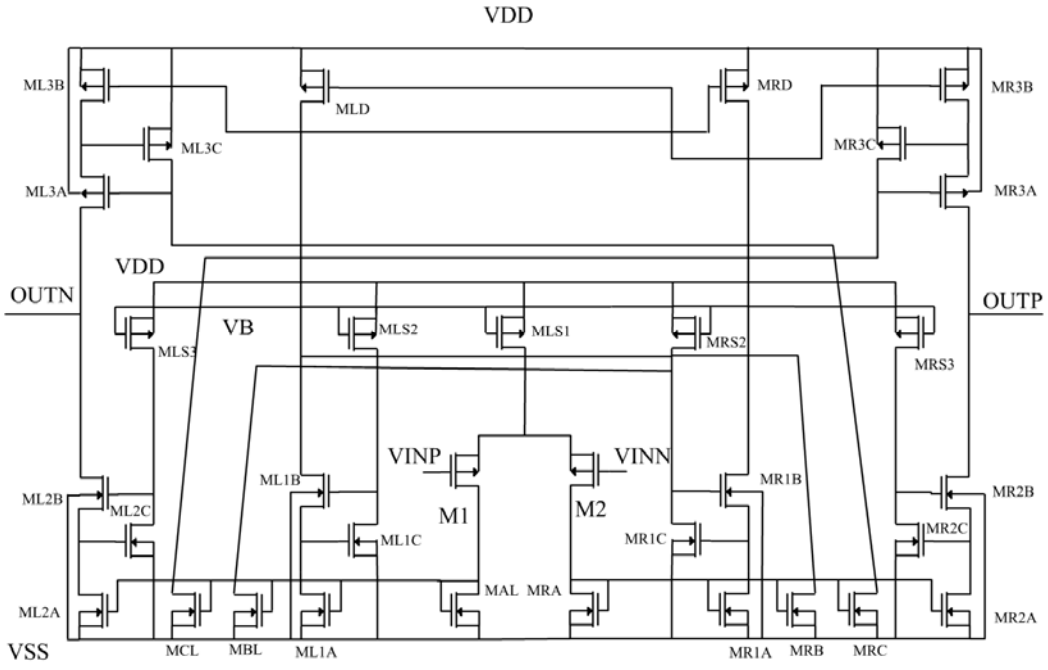


Figure 8 Newly introduced RGC output stage

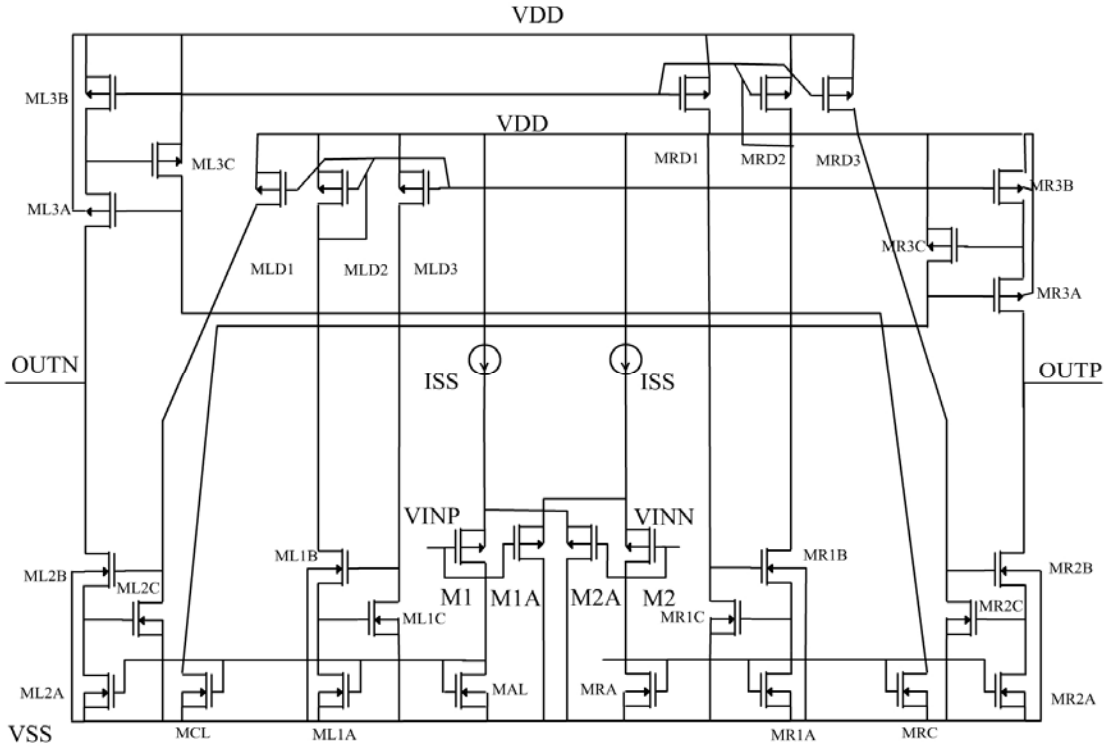


Figure 9. Proposed DO-OTA circuit employing the output stage of Figure 7 and Nedungadi-Visvanathan input stage

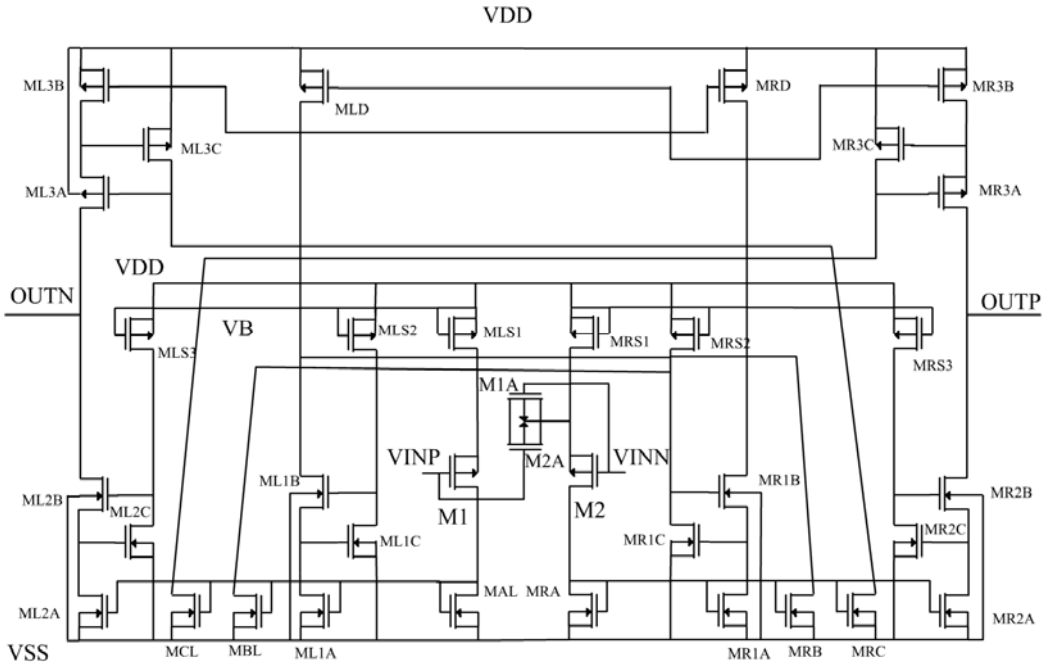


Figure 10. Proposed DO-OTA circuit employing the output stage of Figure 8 and Krummenacher input stage

4. SIMULATION RESULTS

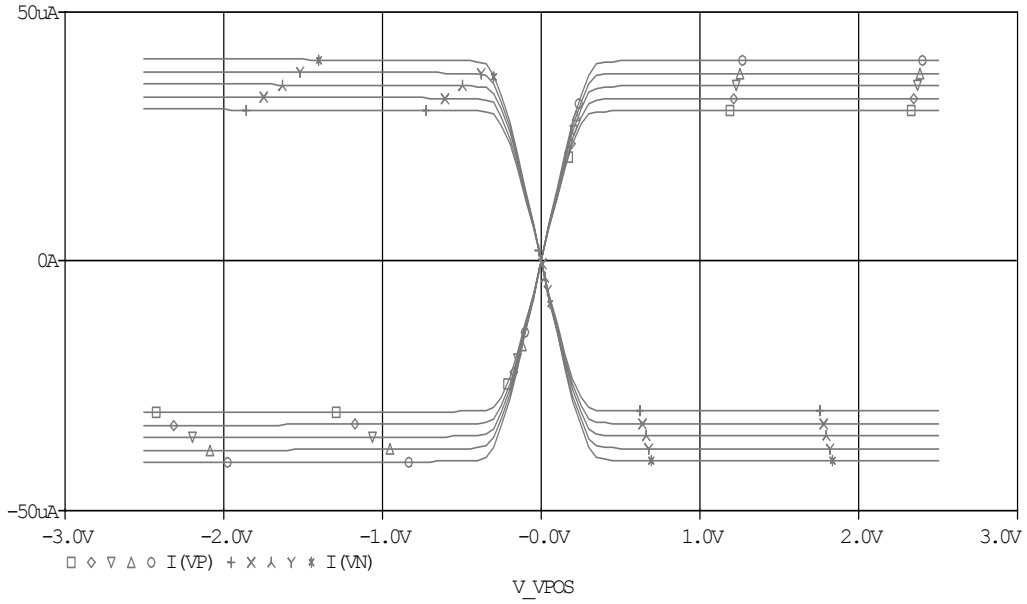
The performances of the CMOS DO-OTA topologies are demonstrated by SPICE simulations. For the simulations AMS 0.8µm MOS models are used. The supply voltages are taken as 2.5 V and –2.5 V. SPICE simulations were performed for circuit characterizations and for a design example of a BP active filter. The results obtained for the circuits are compared with each other. The simulated characteristically plots of DO-OTA structures employing conventional and Nedungadi input differential pairs and the output stage of Figure 7 are given in Figures 11 and 12.

The important properties obtained for the topologies employing other input circuits are summarized in Table I.

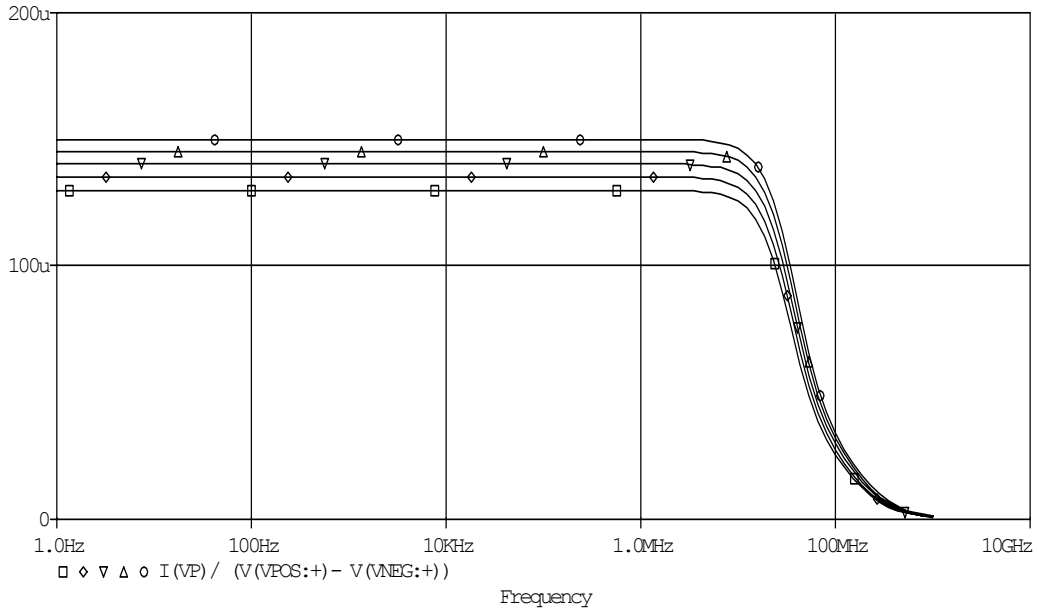
The output resistance and capacitance values of the circuit are summarized for different biasing currents in Table 2.

Table 1 Theorical and Practical Linearity ranges

Input Stage	With First Output Stage		With Second Output Stage	
	Theoretical (mV)	Practical(mV)	Theoretical(mV)	Practical(mV)
Classical	330	380	110	180
Nedungadi	1420	1220	556	597
Cross Coupled	490	420	150	220
Krummenacher	930	510	700	280

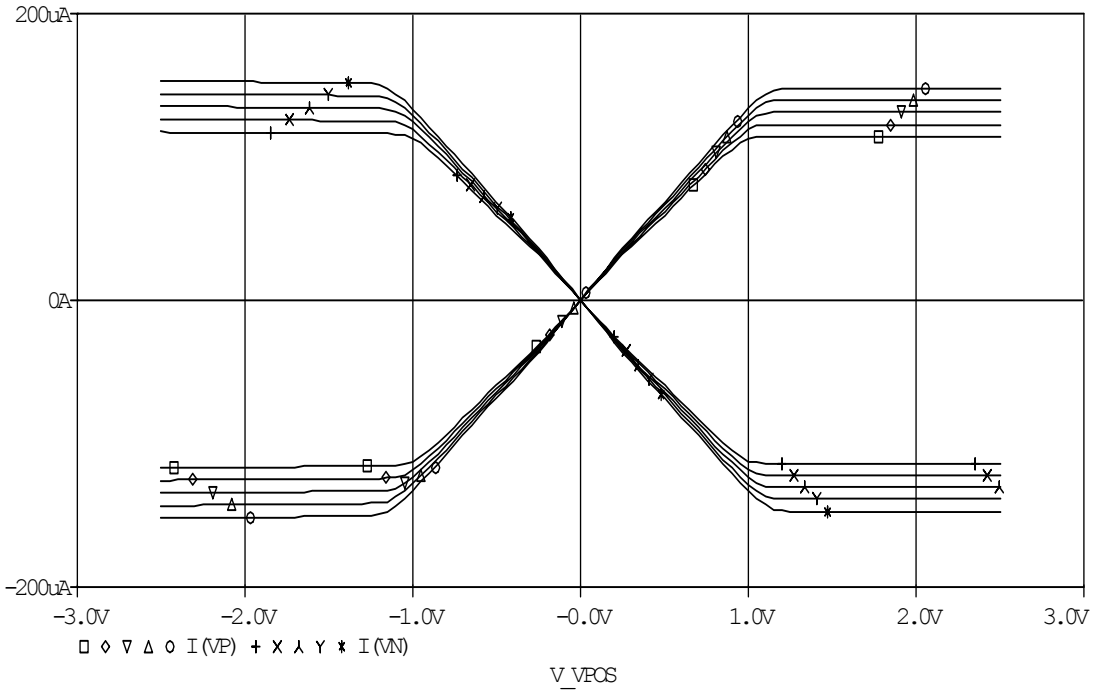


(a)



(b)

Figure 11. Characteristical DC and AC plots obtained for the DO-OTA given in Figure 7. **a)** DC Characteristics **b)** Frequency response of the OTA-transconductance for different biasing currents. Biasing currents: □ 60μA, ◊ 80μA, ∇100μA Δ 120μA and 150μA.



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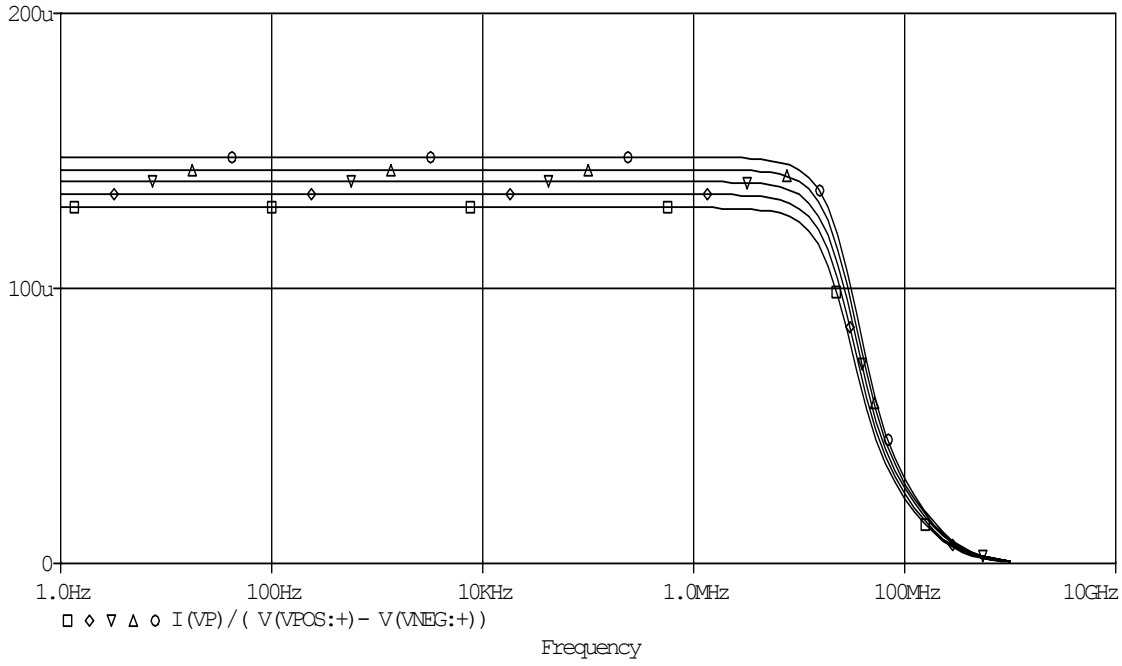

(b)

Figure 12. Characteristical DC and AC plots obtained for the DO-OTA given in Figure 7 **a)** DC Characteristics **b)** Frequency response of the OTA-transconductance for different biasing currents. Conventional differential pair is replaced with linearized Nedungadi-Visvanathan input stage. Biasing currents: □ 60μA, ◊ 80μA, ∇100μA Δ 120μA and 150μA.

Table-2 The output resistance and capacitance values of the circuit for different biasing currents

Biasing current	Output resistance, Ro	Output capacitance, Co
60 μA	6.87 GOhm	24.2 fF
80 μA	4 GOhm	25 fF
100 μA	2.42 GOhm	25.9 fF
120 μA	1.40 GOhm	26 fF

To compare the linearity regions of DO-OTA circuits proposed, the integrator of Figure 13 is used as test circuit. Capacitors are taken 1 nF for all tests. Connecting the inverting input to the reference node a sinusoidal input voltage of 1 kHz is applied to the non-inverting circuit and the signal amplitude is varied in the range of 0V to 2V. For each step the total harmonic distortion at he outputs are calculated and given in Figure 14. From Figure 14 it can be easily observed that, compared to the conventional differential pair, the Nedungadi-Visvanathan, Krummenacher and cross-coupled input stages exhibit lower harmonic distortion at the output where the Nedungadi-Visvanathan circuit exhibits the best performance among the four circuits.

The performance of the CMOS DO-OTA circuits proposed is also demonstrated on a design example of a current-mode BP filter shown in Figure 15. The test filter is a current-mode version of the voltage mode OTA-C filter given previously in the literature [4, 7, and 8].

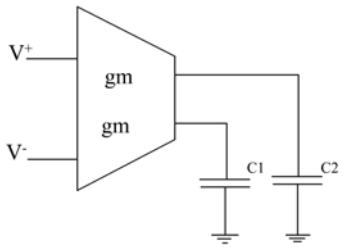

Figure 13. Integrator circuit

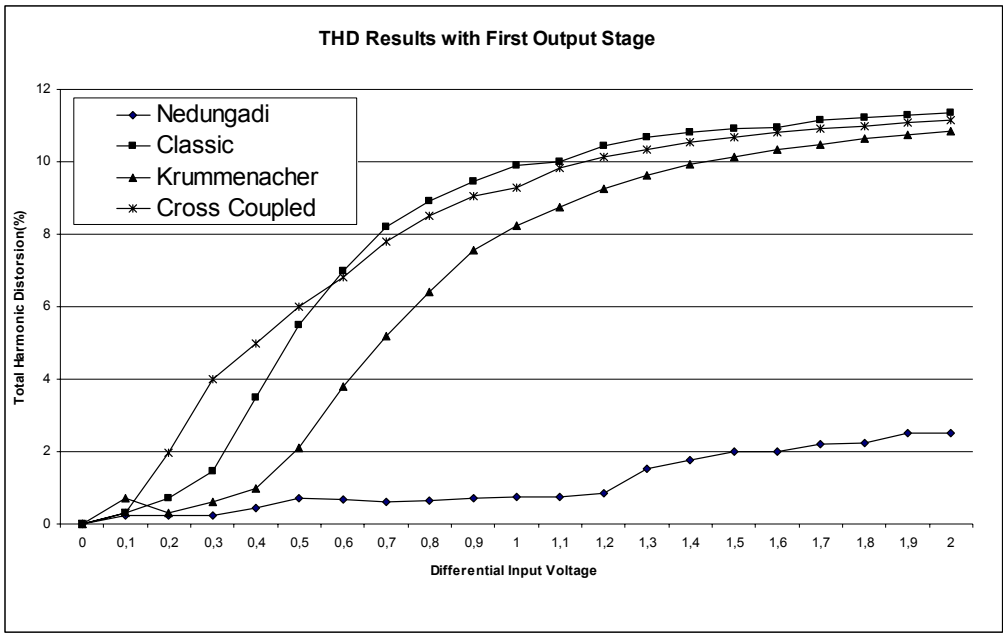

Figure 14. Dependence of total harmonic distortion THD on input voltage obtained for conventional, Nedungadi-Visvanathan, Krummenacher and cross-coupled input stages.

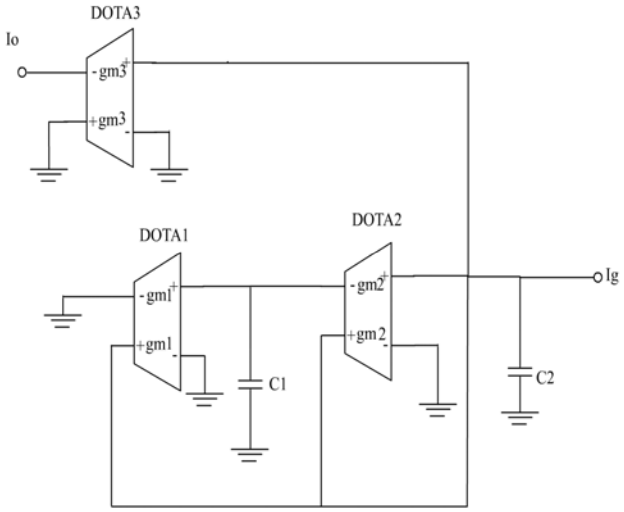

Figure 15 Current mode BP Filter

The transfer function of the filter is given by

$$H(s) = \frac{a_1 s}{s^2 + b_1 s + b_0} \quad (29)$$

where

$$\frac{g_{m1}}{C_1} = \frac{b_0}{b_1}, \qquad \frac{g_{m2}}{C_2} = b_1, \qquad \frac{g_{m3}}{C_2} = a_1 \quad (30)$$

$$b_1 = \frac{\omega_p}{Q_p} \qquad b_0 = \omega_p{}^2 \quad (31)$$

$$\omega_p = \frac{\sqrt{g_{m1}} \cdot \sqrt{g_{m2}}}{\sqrt{C_1} \cdot \sqrt{C_2}} \quad Q_p = \frac{\sqrt{g_{m1}} \cdot \sqrt{C_2}}{\sqrt{g_{m2}}\sqrt{C_1}} \quad (32)$$

SPICE simulations were performed by using the DO-OTAs employing the output stage illustrated in Figure 7. Besides the conventional differential input stage, Nedungadi-Visvanathan, Krummenacher and cross-coupled input stages are also used for simulations. Resulting frequency responses of BP filters are investigated. Each of the filters realizes Butterworth response with a pole frequency of 1 MHz. For simulations the basic quantities are chosen as: g_m=150μA/V, C1 =30pF and C2= 15 pF. Figure 16 illustrates the frequency responses of BP filters realized with conventional symmetrical CMOS-DO-OTA in Figure 1b and the CMOS DO-OTA in Figure 8. To provide simplicity, only the results of one new CMOS-DO-OTA realization are shown in Figure 16. The other CMOS-DO-OTA realizations yield similar improved results. It is observed that all of the filter characteristics agree with the ideal filter responses in a wide frequency range. The deviations at high frequencies can be considered the result of limited DO-OTA bandwidth. The deviations at low frequencies in BP filter characteristics are caused by the limited DO-OTA output resistances. However, these deviations appear below noise level and have no importance from the point of view of filter function. It can be easily observed that the topologies proposed provide an extended improvement due to the increased output resistance.

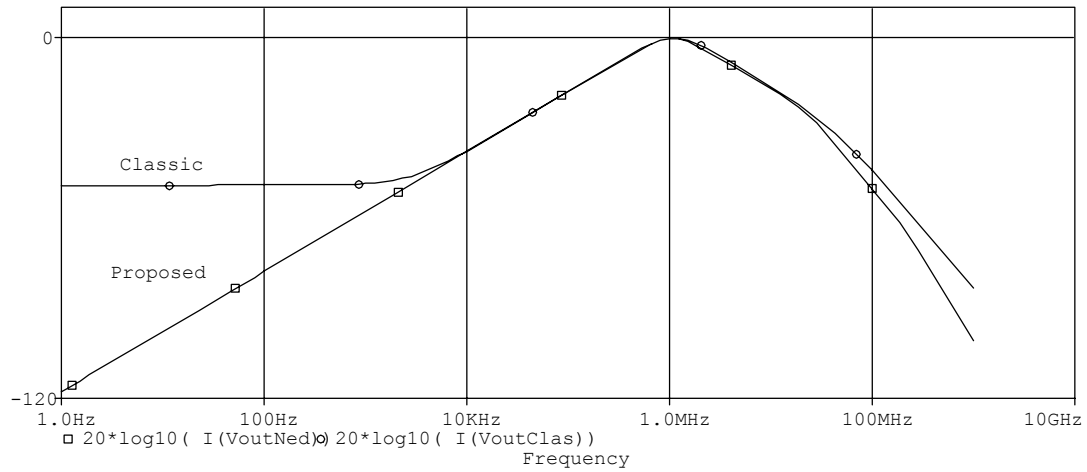

Figure 16 Simulated frequency responses of BPF circuits constructed with classical and proposed DO-OTA structures.

5. CONCLUSION

The aim of this study is to propose high performance dual OTA (DO-OTA) structures providing extended linearity range with extremely high output impedance together. For this reason three different linearization techniques and two different output stages are combined. From simulation results it is easy to say that the linearity range can be extended four times compared to traditional input circuit. The high performance of the proposed DO-OTA circuit introduce new possibilities for the IC designer for realization of high performance DO-OTA-based active filters, oscillators, immittance simulators etc. so that their usage area is extended for further applications.

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