

ANALYSIS OF THE RESISTIVITY IN POLYSILICON THIN FILM TRANSISTORS

Study of film thickness effect

Y.Bourezig¹, B.Bouabdallah¹, F.Gaffiot²

¹Laboratoire de d'Elaboration et de Caractérisation de matériaux,
Université Djilali Liabès, de Sidi Bel Abbès.22000, Algeria

²Laboratoire d'Electronique, d'Optoélectronique et Microsystèmes
Ecole centrale de Lyon, UMR, CNRS 5512 , Ecully, France

ABSTRACT

Polycrystalline silicon thin film transistors have been widely investigated as active element in liquid crystal flat panel displays. The present work consists of an analysis of experimental transfer characteristics for different active layer and a calculation of the layer resistivity in flat band regime. In order to explain the fall of this parameter in the range of 70 to 90nm, a two-dimensional simulation program is presented. It is based on the resolution of Poisson's equation.

The results show that the behaviour of this parameter as a function of film thickness can be attributed to several mechanisms, and that its decrease between 70 and 90nm is related to the simultaneous variation of the average carrier concentration and the channel mobility.

Keywords : Thin–Film Transistor, chemical vapour deposition, electrostatic coupling, modelling

1. INTRODUCTION

Polysilicon transistors have received significant attention. Their use is now the subject of intensive industrial activity because of its applications, particularly, the application to active matrix addressing of LCDs [1].

The performance of devices in polysilicon thin films is inherently inferior to that of the bulk silicon MOSFET. This is due to the presence of grain boundaries, which result in large turn voltage, lower channel mobilities and higher leakage current. In this work, the layer's resistivity of polysilicon transistors is treated in function of the thickness. Several authors have studied the layer resistivity, but only for high thicknesses [2]-[3]-[4] and their conclusions are not sufficient to explain the behaviour of the resistivity for our studied thicknesses. For that, we must consider several mechanisms as impurity segregation, carrier trapping, and effects of coupling between polysilicon/oxide interfaces. Also, we have developed a two dimensional program to explain the variation of this parameter between 70 and 90nm.

In our simulation, the layer is modelled by a series of monosilicon crystallites, separated by grain boundaries which are parallel and perpendicular to polysilicon/oxide interfaces. The simulation allows us to calculate the average carrier concentration and the channel mobility.

Thus, in the next section, the studied structure is described. Section 3 presents the experimental results, then, the resistivity is analyzed in section4. The geometrical and the physical model used is presented in section5. Results of simulation follow in section 6. Finally, conclusions are drawn in section7

2. THE STUDIED STRUCTURE

Fig (1) shows a schematic cross section of accumulation mode MOSFET. The starting material for device fabrication was silicon wafers. A 100nm SiO₂ layer was thermally grown on RCA cleaned substrates. Polysilicon thin films were deposited using low pressure chemical vapour deposition (LPVCD) technique. Channel doping was carried out by ion implantation of boron with dose of $6e12cm^{-2}$ ($1e17cm^{-3}$). Source and drain were formed by $3e20cm^{-3}$ boron implantation, and are assumed to extend in the whole thickness of polycrystalline layer. The gate oxide was grown to a thickness of 100nm. At the end, contact regions were opened for AL metallization. The different thicknesses are obtained by reactive ion etching process.

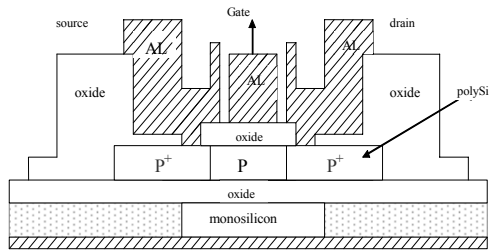


Fig 1: Polycrystalline silicon thin film transistor structure used in this study

3. EXPERIMENTAL RESULTS

The experimental I-V characteristics are illustrated in fig (2). It shows that:

1- In accumulation regime, we can observe a first zone (zone1) where the current increases rapidly according to the gate bias, and a second zone (zone2) which corresponds to “on state” of the transistor.

2- In depletion regime, “off state”, the behavior of the structure is different. It is characterized by the leakage current I_L coming from: the ohmic conduction of polycrystalline layer between source and drain contacts (zone3); and the generation current which is field assisted [5] (zone4). Its variation as a function of gate voltage is related to a POOLE-FRENKEL effect [6].

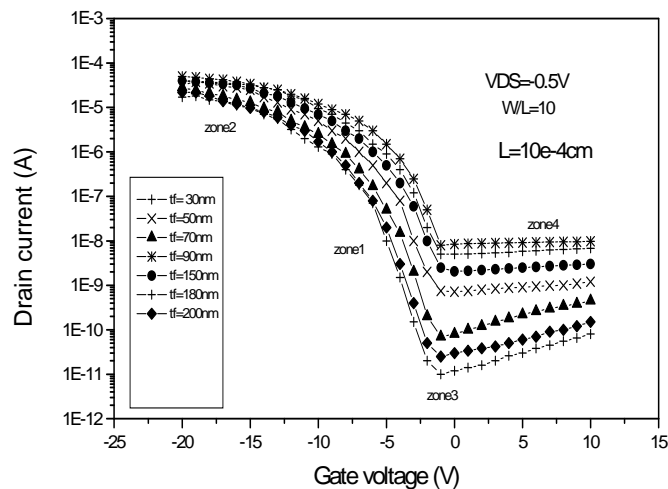


Fig 2 : Experimental transfer characteristics for different thicknesses

In addition,
The large threshold voltage observed in accumulation – mode transistors can only be justified by assuming the existence of both acceptor and donor states at grain boundaries. This conclusion is consistent with the generally agreed result that grain boundaries basically behave as majority- carrier traps.

4. ANALYSIS OF THE LAYER'S RESISTIVITY

Using the value of the drain current in flat band regime, we have calculated the layer resistivity for each thickness. The variation of this parameter as a function of film thickness is shown in Fig (3).

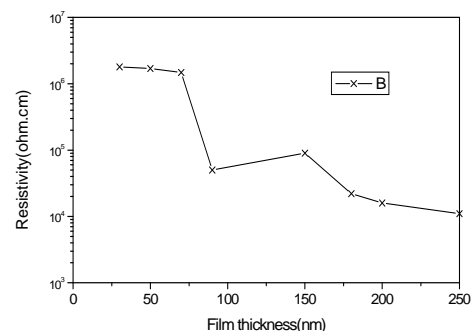


Fig (3): Experimental resistivity versus film thickness

As previously mentioned, several authors studied the resistivity of the polycrystalline layers, but their conclusions cannot interpret the behaviour of the resistivity in the range of the studied thicknesses. Indeed, Kamins studied the resistivity when the film is APCVD deposited and highly doped when the

thickness ranges from 3000 to 24000nm. He attributed the decrease of the resistivity when the film thickness raises to the increase of the carrier's mobility.

Mei and al suggested that, in the case of APCVD deposited and heavily doped films, but with thickness lower than 250nm, the impurity segregation phenomenon is the major cause for the observed increase of the resistivity when the film thickness increases.

Lu and al demonstrated that the variation of the resistivity versus film thickness depends strongly on the level doping and on the lateral grain sizes L_L . Their analysis is based on the carrier trapping mechanism. Thus, for low and moderate doping and large L_L , the resistivity varies slightly with the film thickness t_f and tends to become constant when t_f increases. Our simulated curve shows the same behaviour when the thickness is higher than 180nm.

Thus, the authors conclusions remain insufficient to explain the particular variation of the resistivity when the thickness is inferior to 180nm. It seems that it is closely related to the structure of the films. For that, we must consider all known mechanisms as: impurity segregation, carrier trapping, and effects of coupling between polysilicon/oxide interfaces or between the high interface and the parallel grain boundary.

Beyond 150nm, the resistivity is practically constant. This is consistent with the fact that for doping and L_L used, the resistivity depends slightly on the thickness.

When the thickness is lower than 70nm, the layers present a high resistivity (about $2 \times 10^6 \Omega \cdot \text{cm}$). Indeed, the small grain size and the low doping level induce the depletion of the crystallites.

Between 90 and 150nm, the resistivity increases. Indeed, Micrographic observations indicate that, in this range, the film contains a high density of grain boundaries which is responsible of the magnitude of the resistivity in this one.

If the previous mechanisms can explain the behaviour of the resistivity as a function of film thickness in the preceding ranges. The observed decrease of this parameter in the range of 70 to 90nm can't be related to one of the precedent mechanisms. This is probably due to an enrichment out of carriers and/ or to

an increase of the mobility of this ones, controlled not only by the physical properties of the films, but also, by the intensity of electrostatic coupling between the two polysilicon / SiO_2 interfaces, or between the higher interface and a parallel grain boundary.

5. MODELLING AND NUMERICAL SIMULATION

We use the diagram of fig (4), in order to calculate, at small voltage bias of drain, and at $V_{GS} = -1V$, the distribution of the potential, then the average carrier concentration defined as:

$$P_{av} = \frac{\int_0^{t_f} \int_0^L p(x, y) dx dy}{\int_0^{t_f} \int_0^L dx dy} \quad (1)$$

Where $p(x, y)$ is the local majority carrier concentration, L and t_f are respectively the channel length and the polysilicon film thickness.

In this computation, we consider that layer is composed of identical grains, the size of which is about 200nm. Monoenergetic traps are supposed to be uniformly distributed at the grain boundaries which are assumed as parallel and perpendicular to the interfaces, with a thickness equal to 1nm [7].

To study this structure, the following Poisson's equations is considered, it is given by:

$$\text{Div} (\epsilon \text{grad} \phi) = -q(p - n + \text{dop} + \sum N_T) \quad (2)$$

Used symbols are:

ϵ the permittivity of the material,

n (p) the free electrons (holes) density,

ϕ , the electrostatic potential,

Dop the net doping of the channel,

$\sum N_T$ the sum of the different trap centers present in the material.

The ionized trap densities are given by Schokley-Read-Hall model [8].

Partial differential equation (2) is discretized by the use of the finite differences method [9].

The obtained linear system is solved by the Gauss method.

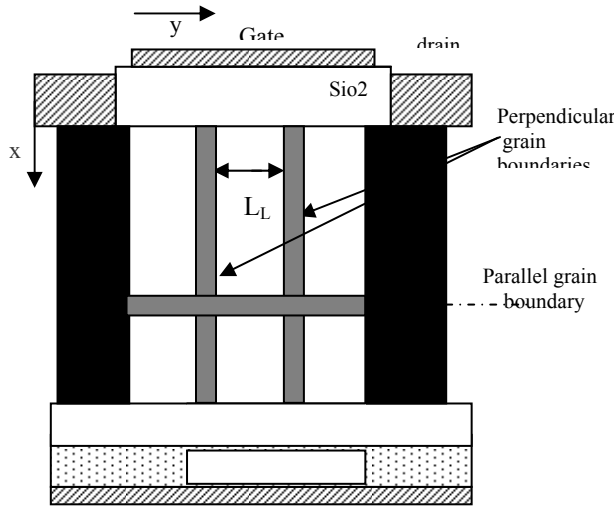


Fig4 :Geometrical model for the studied structure

6. RESULTS OF SIMULATION AND DISCUSSIONS

It is evident that in polysilicon layers, the grain size and the density of intergranular traps can influence the coupling intensity between the interfaces and modify the concentration of the free carriers.

Thus, using the precedent expression, we have calculated $P_{av}(t_f)$ for different grain sizes, and for various intergranular trap densities. The results are presented in Fig (5) and in Fig (6) respectively.

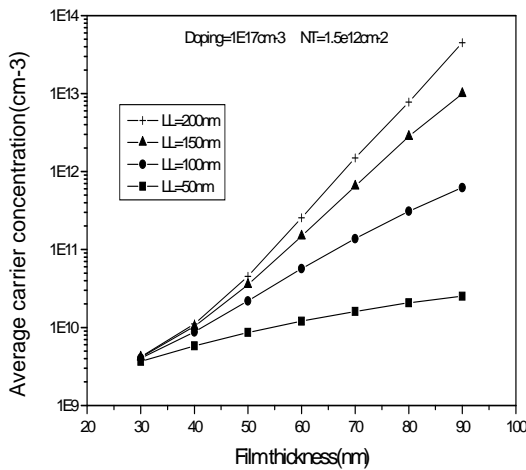


Fig 5: Average carrier concentration versus film thickness, for different grain sizes

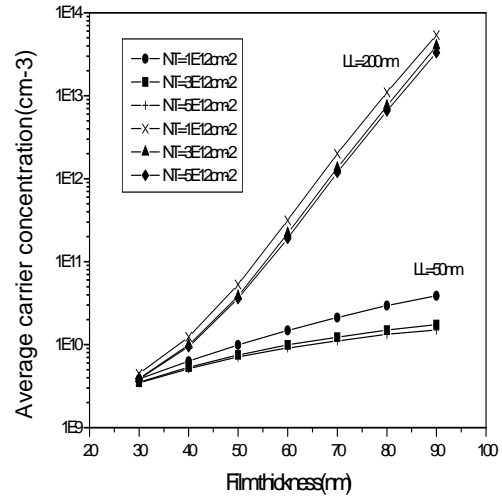


Fig 6: Average carrier concentration versus film thickness for two grain sizes and different trap densities

1- One notices that for the studied doping $N_A = 1E17 \text{ cm}^{-3}$, the crystallites are fully depleted of carriers ($P_{av} < 1E14 \text{ cm}^{-3}$) for any values of N_T and L_L used in the simulation.

2- The average carrier concentration increases with film thickness t_f .

3- The variation rate of $P_{av}(t_f)$ is insensitive to the changing N_T , but varies strongly with L_L , in particular for the layer thickness > 50 nm.

The simulation shows that, in the thickness range between 70 and 90nm, the average carrier concentration varies in a ratio inferior to 10 for any value of traps density.

It appears that in the case of as-deposited polysilicon layers, only the variation of the average carrier concentration is insufficient to explain the variation of the resistivity in this range. We should also consider the variation of the carrier mobility in the same range

which is also an important parameter as the carrier's concentration.

At small gate bias, the effect of electric field on carrier's mobility is negligible. The mobility in the channel μ_{CH} is influenced only by the potential energy barriers. However, taking into account of the different scattering mechanisms, this one is considerably lower than the mobility in the bulk.

By replacing the calculated values of the field effect mobility and of E_B in the following formula:

$$\mu_{FE} = \mu_{CH} \left(1 + \frac{E_B}{KT} \right) \quad (3)$$

We can deduce the corresponding values of μ_{CH} for each thickness.

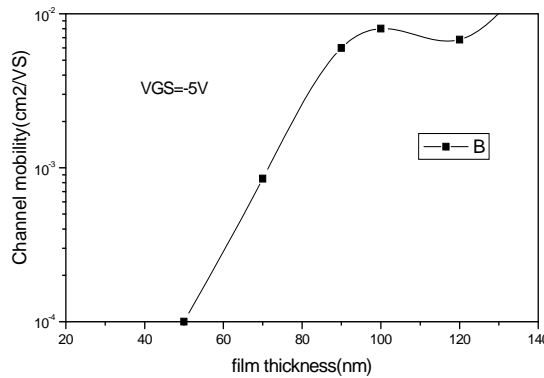


Fig 7: Behavior of carrier mobility versus film thickness at small V_{GS}

As shown in fig (7) which illustrates the variation of channel mobility versus film thickness, the channel mobility increases with increasing t_f . This is consistent with the conclusions of Levinson and al[10] which demonstrated that, in As-deposited polycrystalline silicon layers, the traps density decreases with increasing t_f , thereby increasing the carrier's mobility.

The behaviours of P_{av} and μ_{CH} thus analyzed, show that the decrease of the resistivity in the range of 70-90nm is interpretable by the simultaneous variation of the average carrier concentration and of the carrier's mobility in the channel.

7. CONCLUSION

The analysis of the layer resistivity as a function of film thickness demonstrated that the behaviour of this parameter can be related to several mechanisms. The electrical characterization of amorphous silicon layers allow to study the variation of the resistivity versus the thickness of these ones.

Beyond 150nm, the resistivity varies slightly with the increase of the thickness. This is consistent with the fact that for doping and L_L used, the resistivity depends slightly on the thickness as reported by Lu and al.

The high resistivity observed between 30 and 70nm is attributed to the small level doping of the crystallites. When the thickness ranges from 90 to 150nm, the resistivity increases, this can be justified by the existence of a strong density of traps which is responsible for the reduction of the mobility of free carriers.

To explain the variation of the resistivity between 70 and 90nm, a two dimensional program is used, in which the geometrical model considers that a polysilicon layer is constituted by a

succession of crystallites. The grain boundaries are parallel and perpendicular to the polysilicon- oxide interfaces and the traps are supposed uniformly distributed at each grain boundary. The simulation reveals that the simultaneous increase of the average concentration and of the mobility versus the thickness is responsible for the decrease of the layer's resistivity.

In this work, we have studied only the effect of film thickness on the resistivity of As-deposited polysilicon films. Others important parameters as a doping of the active layer, will make the object of eventual future studies.

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