Atmalı DC saçtırma ile hazırlanan Cr/n–Si Schottky engel diyotunun seri direnç ve arayüzey durum yoğunluğu özellikleri

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Özet

Atmalı DC saçtırma yöntemi ile bir Cr/n–Si Schottky engel diyotu elde edildi. Diyota ait idealite faktörü, engel yüksekliği ve seri direnç gibi elektriksel parametreler Cheung ve Norde tarafından önerilen fonksiyonlarla belirlendi. Diyotun 1,07 idealite faktörü ve 0,60 eV engel yüksekliğine sahip olduğu görüldü. Diyotun arayüzey durum yoğunluk dağılımı akım–gerilim (*I–V*) verileri kullanılarak hesaplandı. Ayrıca, diyotun kapasite–gerilim (*C–V*) ve kapasite–frekans (*C–f*) özellikleri analiz edildi.

Anahtar Sözcükler: Atmalı DC saçtırma, Schottky diyot, Seri direnç, Arayüzey durum yoğunluğu, Engel yüksekliği

The series resistance and the interface state density properties of a Cr/n–Si Schottky barrier diode prepared by pulsed DC sputtering

Abstract

A Cr/n–Si Schottky barrier diode was obtained by pulsed DC sputtering technique. The electrical parameters of the diode such as ideality factor, barrier height and series resistance values were determined using the functions proposed by Cheung and Norde. It was seen that the diode has an ideality factor of 1.07 and a barrier height of 0.60 eV. The interface state density distribution of the diode was calculated using the current–voltage (*I–V*) data. In addition, the capacitance–voltage (*C–V*) and the capacitance–frequency (*C–f*) characteristics of the diode were analyzed.

Keywords: Pulsed DC sputtering, Schottky diode, Series resistance, Interface state density, Barrier height

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1.Introduction

Rectifying metal semiconductor (MS) contacts are the common devices in technology and the most widely used in the electronic industry. Much of semiconductor electronic devices such as solar cells, field effect transistors, frequency multipliers and mixers, microwave diodes and photo detectors are the basic structures using Schottky barrier diodes (SBDs) [1-4]. Their electrical characteristics should be well understood owing to the technological importance. Despite one's attentive fabrication, SBDs possess a thin interfacial native oxide layer between the metal and the semiconductor and this thin native oxide layer converts metal semiconductor contacts to metal insulator semiconductor (MIS) devices [5].

Barrier height (BH) which is the energy separation between the Fermi level and the edge of the majority carrier band at the interface is the most characteristic parameter of a metal semiconductor contact [4-6]. In a MS system, the formation of the BH is determined by the Fermi level within the semiconductor band gap [7,8]. Usually, the forward bias current voltage (*I-V*) characteristics show linear dependencies in the semi logarithmic scale at low voltages but deviate considerably from linearity because of some effects of parameters such as the series resistance R_S, the interfacial layer and the interface states at sufficiently large applied voltage [9,10]. While parameters such as the ideality factor (n) and the barrier height (Φ_b) are effective in both the linear and nonlinear regions of these characteristics, accompanying the change of the Schottky barrier height (SBH), the parameter RS is only effective in the downward curvature region (non linear region) of the forward I V characteristics at sufficiently high applied voltage [11,12].

Many metallization methods have been used in the fabrication of MS diodes including thermal evaporation, e beam evaporation, magnetron sputtering and electrochemical deposition techniques [4, 13-15]. Pulsed DC magnetron sputtering method have recently attracted lots of attention owing to their higher deposition rate, capability of inhibiting arc discharge to enhance plasma density to rise the ionization energy with improved coating efficiency [16-18].

The aim of this work is to fabricate a Cr/n-Si MS structure using pulsed DC sputtering method and determine the series resistance and interface state density properties of the junction using the current voltage (*I-V*) data. Furthermore, the capacitance voltage (*C-V*) and the capacitance frequency (*C-f*) properties of the device are examined.

2. Experimental procedures

The Cr/n–Si Schottky barrier diode was prepared using one side polished n–Si wafer with (100) orientation and 1-10 Ω cm resistivity. The wafer was boiled in trichloroethylene and exposed to ultrasonic vibration in acetone and isopropanol for 5 minutes to remove organic contaminations prior to formation of structures. The wafer was dipped into solution of H_2O/HF (10:1) for 30 s in order to remove native oxide layers on the surfaces and form H terminated surfaces. Preceding each step, the wafers were rinsed in 18 MΩ deionized water. After the cleaning procedures, the wafers were dried under N_2 atmosphere. To make an ohmic back contact, gold (Au) was sputtered on the unpolished side of n-Si substrate and the structure was annealed at 450 ^{0}C for 15 minutes under N_2 atmosphere. After formation of the ohmic back contact, the native oxide layer formed during previous processes was removed by solution of H_2O/HF (10:1) and dried under N_2 atmosphere. The structure was then immediately loaded into a vacuum chamber. Cr/n–Si/Au Schottky barrier diode was formed by pulsed DC sputtering of Cr on Si substrates. The sputtering details are listed in the table 1 and the diode diameter was 1.5 mm. The *I–V* measurement of the diode was performed by Keithley 2400 sourcemeter in dark and the *C–V* and the *C–f* measurements were executed by Agilent 4294A impedance analyzer.

Table 1. Pulsed DC sputtering parameters for Cr/n–Si Schottky diode

Sputtering Parameters	Values
Lowest Pressure	$3x10^{-6}$ Torr
Pressure during sputtering	$5x10^{-3}$ Torr
Distance between target to wafer	10 cm
Bias to substrate	0 W
Bias to target	100 W
Sputter time	15 min
DC pulse frequency	5 kHz
Gas introduced the system	Argon

3. Results and discussion

3.1. Series Resistance Determination of Cr/n–Si Schottky Diode

The *I–V* characteristics of the Cr/n–Si Schottky barrier diode at room temperature in dark are displayed in Fig. 1. The diode has a good rectifying behavior as shown in the figure 1. The deviation of *I–V* characteristics from the linear region at high voltages is due to the series resistance and the interface states at MS interface. When the series resistance is taken into account the electrical properties of MS diodes can be calculated using the well–known Cheung method expressed as follows [18]

$$\frac{\mathrm{dV}}{\mathrm{d}(\ln I)} = IR_S + n\left(\frac{kT}{q}\right) \quad (1)$$

and

$$H(I) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\phi_b \quad (2)$$

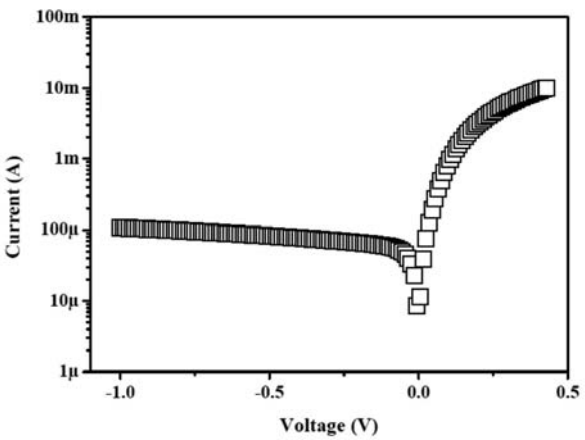

Figure 1. Semilog I–V plot of Cr/n–Si Schottky diode

where k is the Boltzmann constant, *T* is the absolute temperature, *q* is the electronic charge, *V* is the applied voltage, *A* is the diode area and *A** is the Richardson constant equal to 110 $Acm^{-2}K^{-2}$ for n–Si. The plots of d*V*/d*lnI–I* and *H(I)–I* of the diode are shown in Fig 2. Both plots give straight lines in the series resistance region as expected. The R_s and *n(kT/q)* values are determined from the slope and the y–axis intercept of the graph *dV/d*(ln *I*) *–I*, respectively. Similarly, the R_s and Φ_b values are obtained from the slope and the y–axis intercept of the *H(I)–I* graph, respectively. Checking the consistency of the method, the series resistances obtained from both *dV/d*(ln *I*)*–I* and *H(I)–I* plots are used. The ideality factor and the barrier height values of Cr/n–Si diode were found to be 1.07 and 0.60 eV using the d*V*/d*lnI–I* and *H(I)–I* plots, respectively. For an ideal diode, the ideality factor should be unity. When the image force lowering take into account the ideality factor is around 1.03. The calculated ideality factor is higher than the ideal case may be caused by the effects of the very thin oxide layer at the interface. The calculated R_s values of the diode were as 29.4 and 28.9 Ω from y–axis intercepts of d*V*/d*lnI–I* and *H(I)–I* plots, respectively.

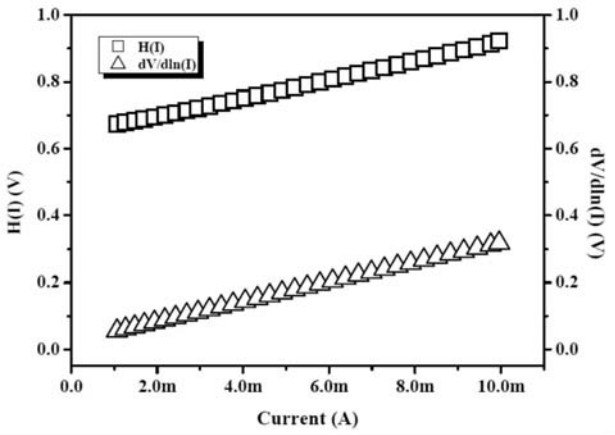

Figure 2 Plots of d*V*/d*lnI–I* and *H(I)–I* for Cr/n–Si Schottky diode

The barrier height and the series resistance of a MS can be also determined using the method proposed by Norde [19]

$$F(V) = \frac{V}{2} - \frac{1}{\beta}\left(\frac{I(V)}{AA^{*}T^{2}}\right) \quad (3)$$

where *I(V)* is the current obtained from *I–V* data and β is the described as q/kT. After determining the minimum value of *F* vs. *V* plot, the barrier height can be calculated from the equation,

$$\phi_b = F(V_0) + \frac{V_0}{2} - \frac{kT}{q} \quad (4)$$

where *F(V0)* is the minimum value of *F* vs. *V* and *V0* is the corresponding voltage value. The figure 3 depicts the *F(V)–V* graph of the Cr/n–Si Schottky diode. The series resistance (R_S) of the contact can be defined through the relation,

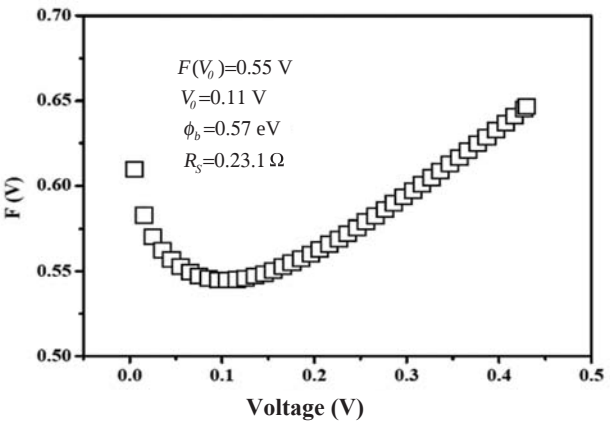

Figure 3. *F* vs. *V* graph for Cr/n–Si Schottky diode

$$R_S = \frac{kT(2-n)}{qI_{\min}} \quad (5)$$

where I_{min} is the corresponding current value at *V0*. The *F(V0)* and *V0* values were determined as 0.55 V and 0.11 V, respectively. The Φ_b and R_s values were calculated as 0.57 eV and 23.1 Ω, respectively. The calculated barrier height and series resistance of the diode using Norde functions are a bit lower than the values obtained from the Cheung functions. The differences can be attributed to the nature of the applied methods.

Furthermore, the plots of series resistance as a function of voltage at different frequencies are shown in Fig.4. The observed peaks might be related to the interface states [20]. The peak intensity is reduced with an increase in frequency, confirming that the distribution of density of interface states varies from lower to higher frequencies. The peaks are disappeared at high frequencies. This indicates that the interface states cannot follow the fast alternating current signal.

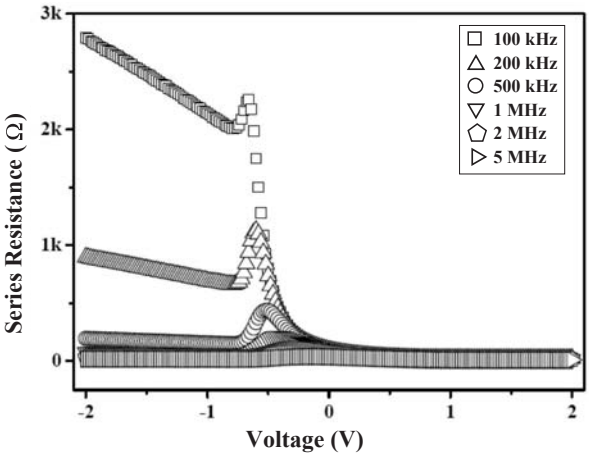

Figure 4. R_S–*V* measurements for Cr/n–Si Schottky diode at various frequencies

3.2. Analysis of Interfacial Properties of Cr/n–Si Schottky Diode

For a real MS contact presenting interface states, the ideality factor n becomes greater than unity. The relation between the ideality factor and the interface state density (N_{SS}) was proposed by Card and Rhoderick as [21],

$$N_{SS} = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}\left(n(V)-1\right) - \frac{\varepsilon_S}{W}\right] \quad (6)$$

where W is the space charge width, ε_S and ε_i are the permittivity of the semiconductor and the interfacial layer respectively, δ is the thickness of the interfacial layer and n(V) the voltage dependent ideality factor value. For the n type semiconductors, the interface states energy (E_{ss}) with respect to the bottom of conduction band at the surface of the semiconductor is given by [22,23]

$$E_C - E_{SS} = q\phi_e - qV \qquad (7)$$

where V is the voltage drop across the depletion layer and Φ_e is the effective barrier height. From experimental data of the forward bias I–V plot, the energy distribution curve of the interface states can be extracted. The NSS variation against $E_C - E_{SS}$ was calculated by substituting the voltage dependent n (V) values and the other parameters in Eq.7 as sketched in figure 5 As seen from the figure, the energy distribution of interface states of Cr/n–Si Schottky diode varies from $1.79\text{x}10^{14}$ to $1.1\text{x}10^{13}$ $eV^{-1}cm^{-2}$.

3.3. The Capacitance–voltage and the Capacitance –frequency Properties of Cr/n–Si Diode

The capacitance–voltage (C–V) measurements of the diode at various frequencies are plotted in Fig.6a. If the capacitance–voltage measurements are carried out at sufficiently high frequencies, the charge at the interface states cannot follow an alternating current (AC) signal. This will occur when the time constant is too long to permit the charge to move in and out of the states in response to an applied signal [5,21,24]. These situations are clearly shown in the figure 6a. The C–V characteristics of the diode can be analyzed by the following relation [5]

$$\frac{1}{C^2} = \frac{2(V_{bi} + V)}{A^2 \varepsilon_s q N_d} \qquad (8)$$

where V_{bi} is the built in potential, ε_S is the dielectric constant of semiconductor (ε_S=11.8) and N_d is the donor concentration. In order to determine V_{bi} and N_d values for the diode, C^{-2} –V of the diode at 500 kHz was plotted in Fig.6b. The V_{bi} and N_d values were determined to be 0.40 eV and $4.56\text{x}10^{15}$ cm^{-3}, respectively. The barrier height Φ_b of the diodes can be determined by the following relation [5]

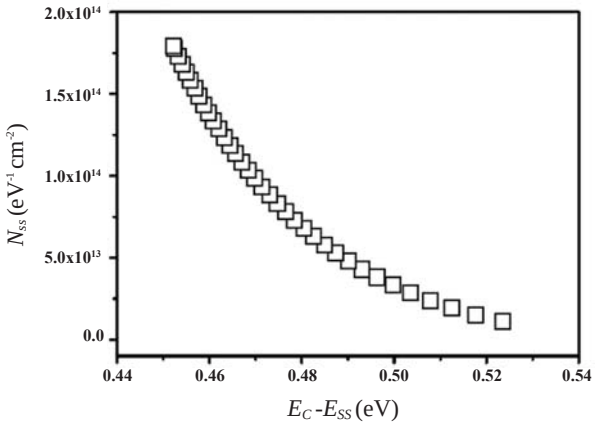

Figure 5. Interface state density distribution of Cr/n–Si Schottky diode

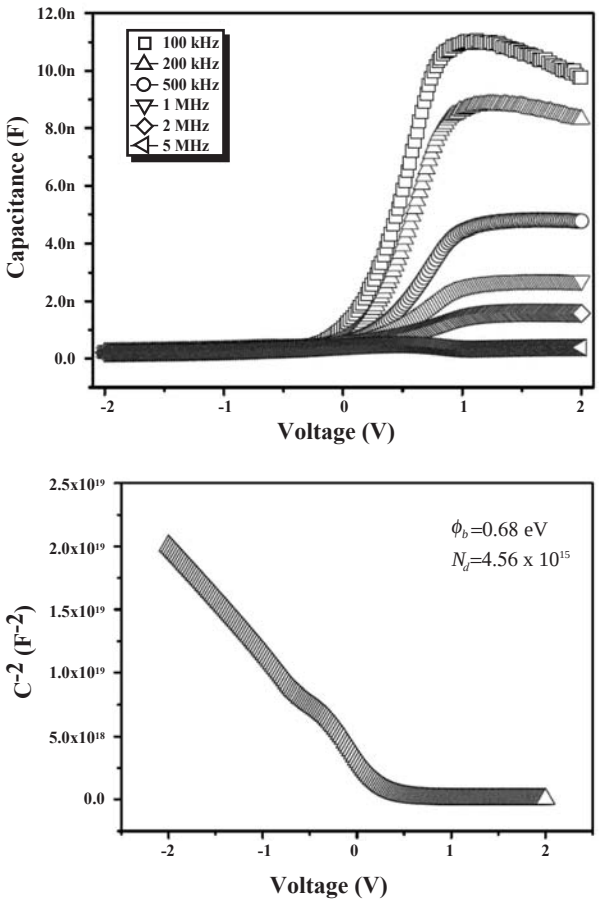

Figure 6 a) C–V measurements at various frequencies and **b)** C^{-2}–V plot at 500 kHz for Cr/n–Si Schottky diode

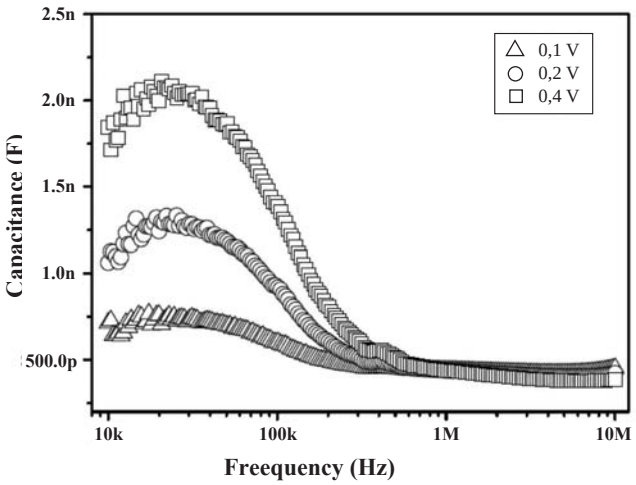

Figure 7. *C–f* measurements of the diode between 10 kHz to 10 MHz

$$\phi_b(C-V) = V_{bi} + V_p \qquad (9)$$

where V_p is the potential difference between the bottom of the conduction band in the neutral region of n–Si and the Fermi level. The V_p value for n–Si can be calculated when the carrier concentrations N_d is known. The value of V_p has been calculated as 0.279 eV for n–Si semiconductor. Therefore, the barrier height value of Cr/n–Si MS diode were calculated as 0.68 eV calculated using Eq. (9). A discrepancy in Φ_b of 0.08 eV is observed between the results obtained from *I–V* and *C–V* plots. This discrepancy may be due to the presence of the thin native oxide between the metal and the semiconductors. The existence of barrier height inhomogeneity can be another explanation [25].

Moreover, Fig.7 presents the capacitance frequency (*C–f*) measurements of Cr/n–Si Schottky barrier diode between 10 kHz to 10 MHz at different voltages. As seen from the figure, the capacitance decreases with an increase in frequency and then remains nearly constant. The higher capacitance values of the diode at lower frequencies show the excess capacitance resulting from the interface states in equilibrium with the n–Si that can follow the AC signal [26–28]. It means that while the interface states at lower frequencies follow the alternating current signal, they cannot follow the alternating current signal at higher frequencies. This suggests that the contribution of the interface states capacitance to the total capacitance is small which may be neglected [26,27]. Therefore, the values of the capacitance at the high frequency region are only the space charge capacitance [28].

4. Conclusions

A Cr/n–Si MS contact was fabricated using pulsed DC sputtering process. It was revealed that the contact has a good rectification with 1.07 ideality factor and 0.60 eV barrier height values. The series resistance values of the diode were calculated as 29.4 and 28.9 Ω from Cheung functions and 23.1 Ω from Norde functions. Series resistance versus voltage measurements at different frequencies implies the effects of interface states on the electrical properties of the diode. The interface state density distribution of the diode was determined using the current–voltage data. In addition, the capacitance–voltage and the capacitance–frequency properties of Cr/n–Si diode were measured. It was also seen that the barrier height value obtained from the current–voltage measurements is 0.08 eV smaller than the value obtained from the capacitance–voltage measurements.

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