F.KAÇAR AND Y. ÖZÇELEP / IU-JEEE Vol. 11(1), (2011), 1327-1332

CDBA Based Voltage-Mode First-Order All-pass Filter Topologies

Fırat KAÇAR, Yasin ÖZCELEP

Istanbul University, Dept. of Electrical and Electronics Engineering,
Engineering Faculty, 34320, Avcilar, Istanbul, Turkey
Tel: +90-212-473-7070, Fax: +90-212-473-7180

{fkacar,ycelep}@istanbul.edu.tr

Abstract: *Five new configurations realizing canonical first-order voltage-mode all-pass filter configurations using a single current differencing buffer amplifier (CDBA) are given. Two of these filter configurations, which were also canonical all-pass filters, contained four passive elements, while the others contained five passive elements. The circuits are suited for CMOS implementation. The SPICE simulation results for frequency response as well as transient response are incorporated to verify the theory.*
Keywords: *CDBA, Active Filters, All Pass Filter.*

1. Introduction

As an active building block, operational amplifier played a predominant role in the last two decades and an enormous number of publications exist in the literature on various circuit examples so that the design engineer can make choice of them. However, opamp-based circuits exhibit several drawbacks in their performance arising from the limited bandwidth and slew-rate of these active elements. Therefore, current-mode approach has been increasingly recognized as a way to overcome the opamp drawbacks and to realize high speed systems. In the last decade and especially in recent years new current-mode active building blocks like second generation current conveyors (CCII+ and CCII−), current-feedback opamps (CFOA) received considerable attention due to their larger dynamic range and wider bandwidth [1, 2]. In addition, different types of active elements like electronically controlled current-conveyor (ECCII), differential voltage current conveyor (DVCC), differential difference current conveyor (DDCC), third generation current conveyor(CCIII), dual output operational transconductance amplifier (DO-OTA) and four terminal floating nullor (FTFN) are presented in the literature [3–8].

In recent years, a new active building block, which is called as current differencing buffered amplifier (CDBA) is introduced by Acar and Ozoguz to provide further possibilities in the circuit synthesis and to simplify the implementation [9]. The CDBA can offer such as high-slew rate, wide bandwidth and simple implementation for internally grounded input terminals [11]. Many applications based on CDBA were reported in the literature. Some of them are fully integrated signal process circuits [10], current-mode filters [11-15], voltage-mode filters [16, 17], resistance controlled sinusoidal oscillators [18], fully integrated gyrator circuits [19]. They have been demonstrated that the CDBA is a versatile active building block for voltage-mode and current-mode signal processing applications.

First- and high-order all-pass filters are widely used in analogue signal processing in order to shift the phase of an electrical signal while keeping the amplitude constant to implement frequency selective circuits with high quality factor. Cicekoglu et al. and Toker et al. proposed all-pass filters using single CCII+ [20-21]. Cam et al. proposed all-pass filters using single FTFN [22].

In this paper, five CDBA based voltage-mode first order all-pass filter configurations are presented. All proposed circuits use only a single CDBA. However some of them use five passive components, some of them use four passive components. PSPICE simulations were performed with a CMOS realization of the CDBA. Simulation results show that filter characteristics are in good agreement with theory.

2. Circuit description of CDBA

The circuit symbol of the current differencing buffered amplifier (CDBA) is shown in Figure 1, where

Received on: 04.02.2011
Accepted on: 07.06.2011

p and n are input terminals, w and z are output terminals.

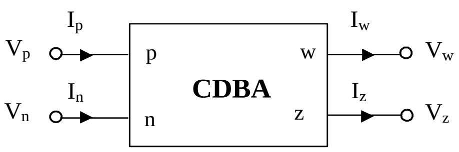


Figure 1. Symbol of the CDBA

The equivalent circuit of the CDBA is given in Figure 2. The current differencing buffered amplifier is characterized by equation (1) [9].

$$\begin{bmatrix} i_z \\ v_w \\ v_p \\ v_n \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 \\ 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} v_z \\ i_w \\ i_p \\ i_n \end{bmatrix} \quad (1)$$

According to the above matrix equation and equivalent circuit of shown Figure 1 the current through z-terminal is the difference of the currents through p-terminal and n-terminal, hence, the z-terminal is called current output; p- and n-terminals are non-inverting and inverting input terminals, respectively. Since the voltage at the w-terminal follows the voltage of z-terminal, it is called voltage output. Note that the input terminals, through which i_p and i_n flows, are internally grounded, where ideally the input impedance of the terminals p and n are internally zero.

3. CDBA-based all-pass filter topologies

All-pass filters are one of the most important building blocks of many analog signal-processing applications and therefore have received much attention. They are generally used for introducing a frequency dependent delay while keeping the amplitude of the input signal constant over the desired frequency range. Other types of active circuits such as oscillators and high-Q band-pass filters are also realized by using all-pass filters [23].

Proposed first order all-pass filter circuits and their voltage transfer functions are given in Figure.2. The transfer functions of the allpass filters which is given in Figure.2 are expressed as:

$$\frac{V_{out}}{V_{in}} = \frac{1 - sCR}{1 + sCR} \quad (2)$$

4. Simulation results

In order to demonstrate the applicability of the proposed all-pass filter circuit shown in Figure.2a. The simulations were performed using a CMOS realization of CDBA shown in Figure.3 [10]. The Model parameters were obtained from the MIETEC 0.5-m CMOS process. Supply voltages are taken as 2.5 V and -2.5 V. To verify the theoretical results, the first order all-pass filter was constructed and simulated with PSPICE program. For this purpose, passive components were chosen as $R_1 = 10k\Omega$, $R_2 = 20k\Omega$ and $C_1 = C_2 = 10pF$ which results in a 1.59 MHz center frequency. Simulation results of the filter response given in Figure.4 which follows theoretical results. Figure.5 shows the time-domain response of the filter. A sinusoidal input at the frequency of 1.59MHz was applied to the all-pass network constructed with above mentioned passive element values.

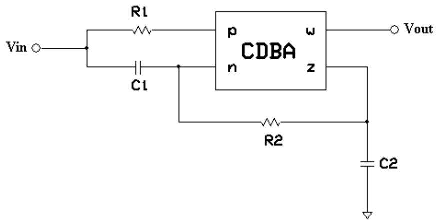
The large signal behavior of the proposed circuit all-pass filter of Fig.2a is tested by applying a 1 MHz sinusoidal signal with amplitude of 1 V to the input. The dependence of the output harmonic distortion of all-pass filter on input voltage amplitude is illustrated in Figure. 6. The T.H.D. remains in acceptable limits i.e. 5% thus confirming the practical utility of the proposed circuit.

5. Conclusions

CDBA, current differencing buffered amplifier, is a multi-terminal active component with two inputs and two outputs. The CDBA is simplifying the implementation, free from parasitic capacitances, able to operate in the frequency range of more than hundreds of MHz.

All-pass filters are one of the most important building blocks of many analog signal-processing applications and therefore have received much attention. They are generally used for introducing a frequency dependent delay while keeping the amplitude of the input signal constant over the desired frequency range. Other types of active circuits such as oscillators and high-Q band-pass filters are also realized by using all-pass filters.

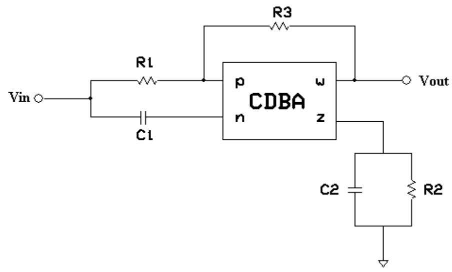
In this paper, five CDBA based voltage-mode first order all-pass filter configurations are presented. All proposed circuits use only a single CDBA. However some of them use five passive components, some of them use four passive components. PSPICE simulations were performed with a CMOS realization of the CDBA. Simulation results show that filter characteristics are in good agreement with theory.



(a)

$$\frac{V_{out}}{V_{in}}=\frac{R_2}{R_1}\left(\frac{1-sC_1R_1}{2+sC_2R_2}\right)$$

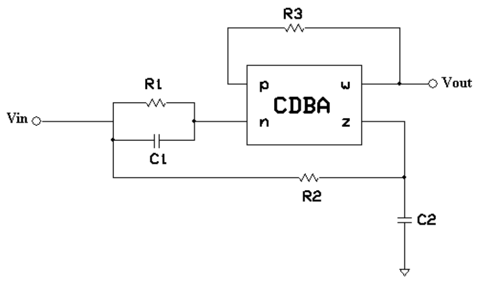
$$R_1=\frac{R_2}{2}=R \text{ and } C_1=C_2=C$$



(b)

$$\frac{V_{out}}{V_{in}}=\frac{R_2R_3}{R_1}\left(\frac{1-sC_1R_1}{R_3-R_2+sC_2R_2R_3}\right)$$

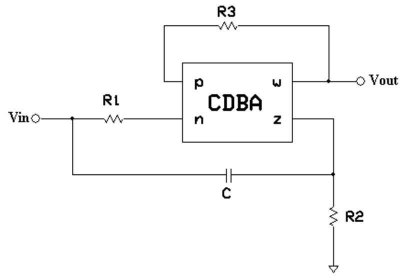
$$R_1=2R_2=R_3=R \text{ and } C_1=C_2=C$$



(c)

$$\frac{V_{out}}{V_{in}}=\frac{R_3}{R_1}\left(\frac{R_1-R_2-sC_1R_1R_2}{R_3-R_2+sC_2R_2R_3}\right)$$

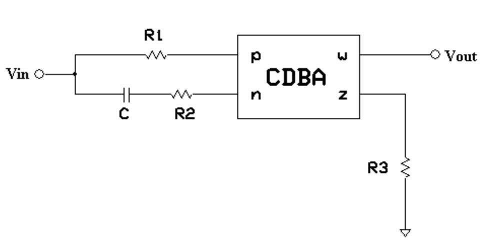
$$R_1=2R_2=R_3=R \text{ and } C_1=C_2=C$$



(d)

$$\frac{V_{out}}{V_{in}}=-\frac{R_2R_3}{R_1}\left(\frac{1-sCR_1}{R_3-R_2+sCR_2R_3}\right)$$

$$R_1=2R_2=R_3=R$$



(e)

$$\frac{V_{out}}{V_{in}}=\frac{R_3}{R_1}\left(\frac{1-sCR_1+sCR_2}{1+sCR_2}\right)$$

$$\frac{R_1}{2}=R_2=\frac{R_3}{2}=R$$

Figure 2. First order all-pass filter topologies

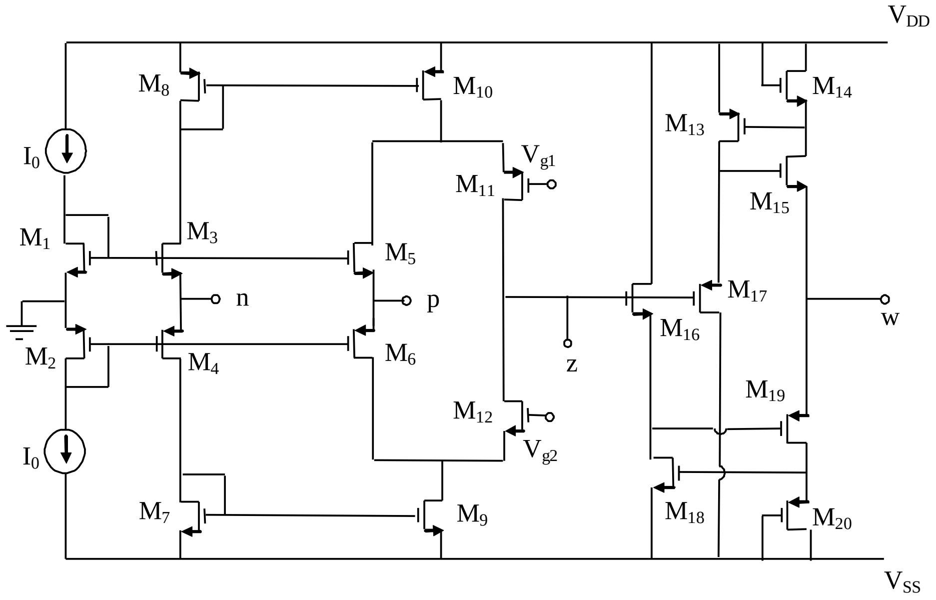


Figure 3. A CMOS implementation of the CDBA

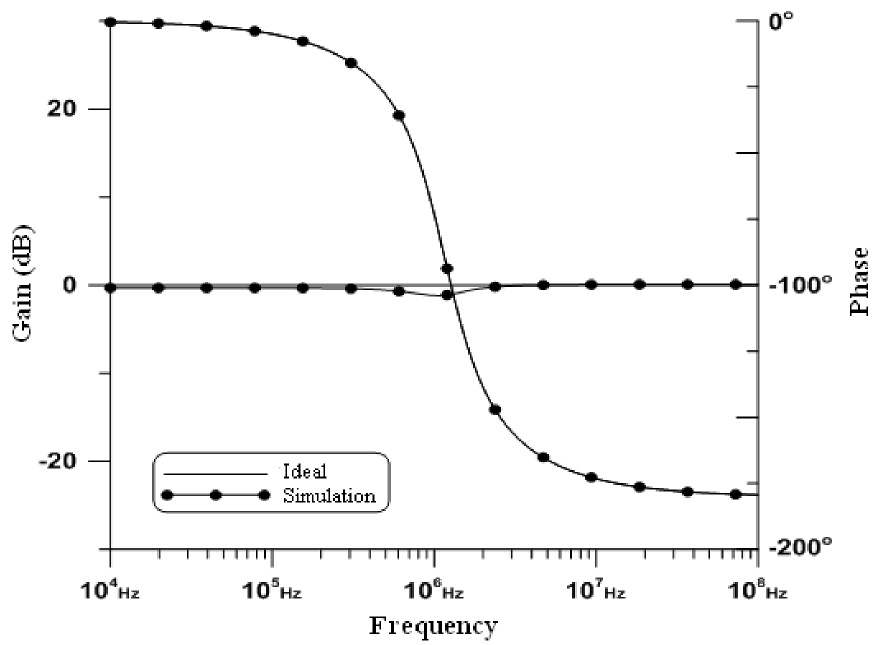


Figure 4. PSPICE simulation results of the proposed all-pass filter (amplitude —, phase ---)

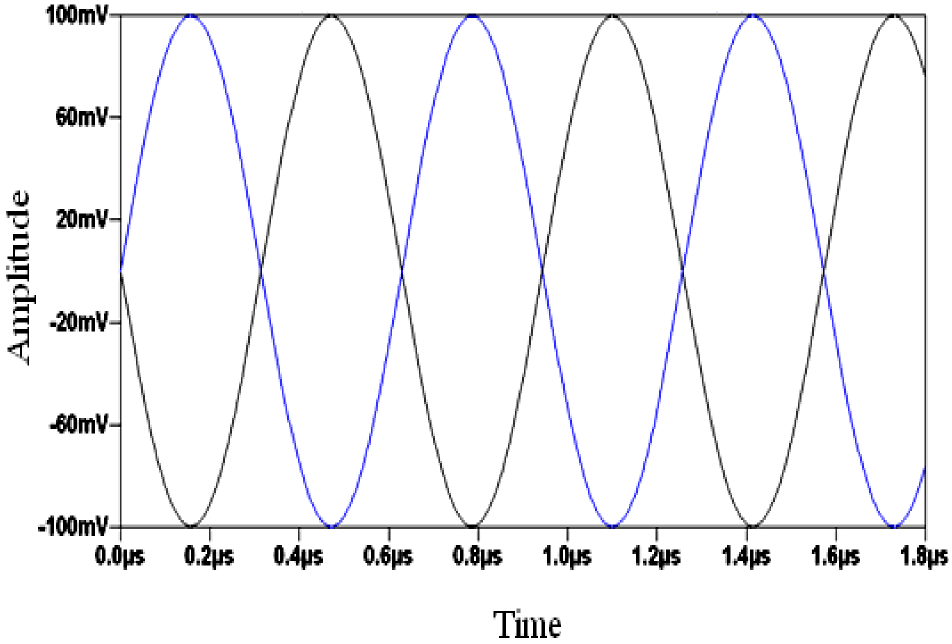


Figure 5. Simulated time-domain response of the proposed all-pass filter

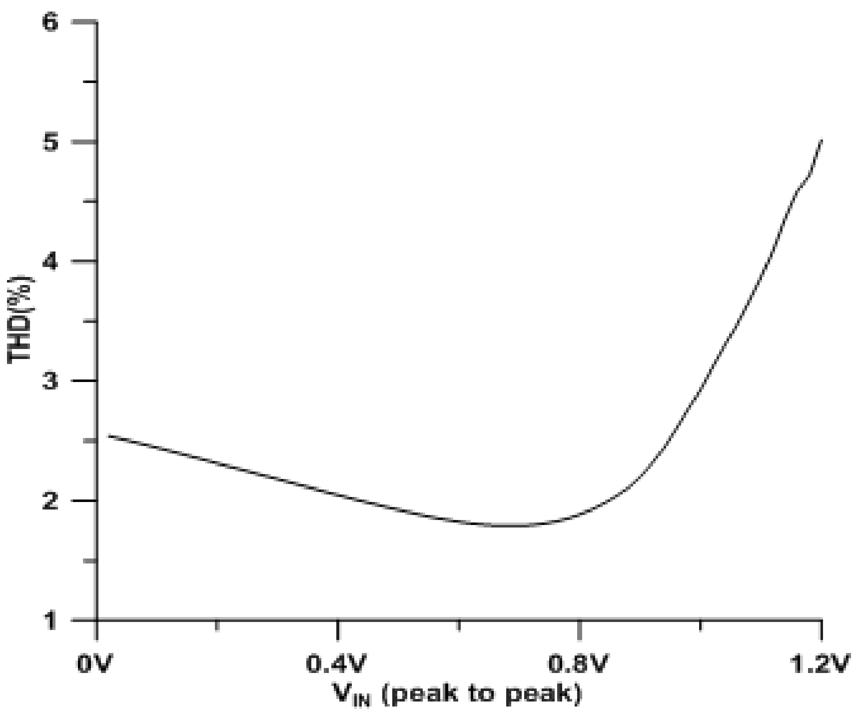


Figure 6. THD analysis results of the presented circuit in Fig.2a in all-pass filter configuration.

6. References

[1] M. C. H. Cheng, C. Toumazou, "3V MOS current conveyor cell for VLSI technology", Electr Lett vol. 29, pp. 317-318, 1993.

[2] AD Inc., "AD844 current feedback op-amp", Data Sheet.

[3] W. Surakampontorn, P. Thitimajshima, "Integrible electronically tunable current conveyors", IEE Proceedings Pt. G., pp. 71–77, 1988.

[4] H. O. Elwan, A. M. Soliman, "Novel CMOS differential voltage current conveyor and its applications", IEE Proceedings Pt. G. pp.195–200,1997.

[5] W. Chiu, S. I. Liu, H. W. Tsao, J. J. Chen, "CMOS differential difference current conveyors and their applications", IEE Proceedings Pt, pp. 91–96, 1996.

[6] A. Fabre, "3rd-generation current conveyor – a new helpful active element", Electronics Letters, vol. 31, pp. 338–339, 1995.

[7] J. H. Huijsing, J. De Korte, "Monolithic nullor: A universal active element", Solid State Circuits vol. 12, pp.50–64, 1997.

[8] H. Kuntman, A. Özpinar, "On the realization of the DO-OTA-C oscillators", Microelec J, vol.29, pp. 991–997, 1998.

[9] C. Acar, S. Özoguz, "A new versatile building block: Current differencing buffered amplifier suitable for analog signal processing filters", Microelec J, vol.30, pp.157–160, 1999.

[10] S. Özoguz, A. Toker, M. A. İbrahim, C. Acar, "A new versatile building block: Current differencing amplifier and its applications", In Proceedings of The European Conference on Circuit Theory and Design, ECCTD'99,pp. 90-93, 1999.

[11] S. Özoguz, A. Toker, C. Acar, "A new current-mode continuous time fully integrated universal filters", Elect Lett, vol. 35, pp. 97–98,1999.

[12] A. Toker, S. Özoguz, O. Çiçekoğlu, C. Acar, " Current mode allpass filters using CDBA and a new high Q bandpass filter configuration", IEEE Transactions on Circuits and Systems, vol.47, pp. 949-954,2000.

[13] C. Acar, H. Sedef, "Realization of nth-order current transfer function using current differencing buffered amplifiers", Int J Electron, vol.90, pp.277-283,2003.

[14] A. Toker, S. Ozoguz, C. Acar, "Current-mode KHN-equivalent biquad using CDBAs", Elect Lett vol. 35, pp.1682-1683,1999.

[15] W. Tangsrirat, W. Surakampontorn, N. Fujii, "Realization of leapfrog filters using current differencing buffered amplifiers", IEICE Trans Fundamentals, (Japan), vol.86, pp.318-326,2003.

[16] H. Sedef, C. Acar, "On the realization of voltage-mode filters using CDBA", Frequenz, vol.54, pp.198-202,2000.

[17] K. N. Salama, A. M. Soliman, "Voltage mode Kerwin-Huelsman-Newcomb circuit using CDBAs", Frequenz, vol.54, pp. 90-93,2000.

[18] S. Özcan, A. Toker, C. Acar, H. Kuntman, O. Çiçekoğlu, "Single resistance controlled sinusoidal oscillators employing current differencing buffered amplifier", Microelec J, vol.31, pp.169-174,2000.

[19] A. Toker, S. Ozoguz, C. Acar, "CDBA-based fully-integrated gyrator circuit suitable for electronically tunable inductance simulation", Int. J. of Electronics (AEÜ), vol.54,pp.293-296,2000.

[20] O. Çıçekoğlu, H. Kuntman, S. Berk, "Allpass Filters using a single current conveyor", Int J of Electronics, vol.86, pp.947-955, 1999.

[21] A. Toker, S. Özcan, H. Kuntman, O. Çiçekoğlu, "Supplementary all-pass sections with reduced number of passive elements using a single current conveyor", Int J of Electronics, vol.88, pp.969-976,2001.

[22] U. Çam, O. Çiçekoğlu, M. Gülsoy, H. Kuntman, "New voltage and current mode first-order all-pass filters using single FTFN", Frequenz, vol.7-8, pp.177-179,2000.

[23] R. Schauman, M. E. Valkenburg, "Design of analog filters", Oxford University Press, New York, 2001.

Fırat KAÇAR received his B.Sc., M.Sc. and Ph.D. degrees from Istanbul University in all in Electrical and Electronics Engineering 1998, 2001 and 2005. He is currently an Assistant Professor at the Electrical and Electronics Engineering Department of Istanbul University. His current research interests include analog circuits, active filters, synthetic inductors, CMOS based circuits electronic device modeling and hot-carrier effect on MOS transistor. He is the author or co-author of about 50 papers published in scientific journals or conference proceedings.

Yasin ÖZCELEP received B.Sc., M.Sc. and Ph.D. degrees from Istanbul University in 2002, 2004 and 2009, respectively. In 2002 he joined the Electrical and Electronics Engineering Department of Istanbul University. Since 2002 he is a research assistant in the same department. His research interest include electronic circuits, reliability analysis of electron devices and electronic-biomedical systems.