Practical Synthesis Of Irrational Impedance Based On Solutions Of The Quadratic Equation

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Abstract: *This article presents the rational approximations of recursively obtained solutions of the quadratic equation which lead to networks with lattice or tree structure. The impedance of a similar electrical circuit, composed of resistors and capacitors, has a module, depending on the square root of the frequency and its phase is equivalent to -45°.*

After considering the effect that the number of elements and their tolerances have on the accuracy of the impedance function of the networks, an eight section lattice cascade was constructed. The deviation between the theoretically and experimentally obtained magnitude and phase characteristics of such a device in the frequency interval 0,05÷1MHz did not exceed -1,2% and -1,3° respectively. Furthermore, it was found that the lattice network performance had impedance close to the expected one but in parallel with a capacity.

Keywords: *Circuit, Irrational impedance, Synthesis, Continued fraction, Lattice structure, Tree structure*.

1. Introduction

Numerous detailed approaches have been discussed in the literature for the realizations of irrational impedances $Z(s)$ [1-6]. This is due to the many applications of such network functions in areas like signal processing circuits, robotics, PID controllers, macro-modeling and so forth [7-11]. For analysis, synthesis and implementation of such objects, the need often arises for some approximation of $Z(s)$ which yields simple lumped network realizations with known component values. Particularly interesting for the purposes of approximation are polynomials, rational functions and continued fractions.

A real polynomial function of the variable s is one that has the form:

$$Z_{RF}(s) = p_0 + p_1.s + ... + p_\mu.s^\mu, \qquad (1)$$

where $p_0, p_1, p_2, ... p_\mu$, $p_\mu \neq 0$ are real numbers and μ denotes a non-negative integer that defines the degree of the polynomial [12]. A polynomial with a degree of 0 is simply a constant. Polynomials are among the most frequently used fitting functions.

They are popular because of their simple form, well known and understood properties.

A real rational function is simply the ratio of two real polynomial functions:

$$Z_{RF}(s) = \frac{P_\mu(s)}{Q_v(s)} = \frac{p_0 + p_1.s + ... + p_\mu.s^\mu}{q_0 + q_1.s + ... + q_k.s^v}, \qquad (2)$$

where $p_0, p_1, p_2, ... p_\mu$, $q_0, q_1, q_2, ... q_v$, $p_\mu \neq 0$, $q_v \neq 0$ are real numbers, μ denotes a non-negative integer that defines the degree of the numerator and v is a non-negative integer that defines the degree of the denominator. A rational function contains a polynomial as a subset (i.e., the case when the denominator is a constant). Rational functions are sometimes superior to polynomials because of their ability to model functions with poles or some other singularity [13,14]. They are often used to model a complicated structure with a fairly low degree in both the numerator and denominator. This, in turn, means that fewer coefficients will be required compared to the polynomial model [13].

Another related tool used to find good rational approximations are truncated continued fractions (CF). They are an excellent choice if the practical realization of irrational impedance is needed because:

-CF frequently converge much more rapidly than power series expansions, and converge in a much larger domain in the complex plane [13]. In this case, the final circuit will contain fewer elements, since the required accuracy of approximation can be achieved with low order convergents;

-Rational approximation in the form of a truncated CF can be directly used to build one-port electrical network with impedance Z_{RF} [14,16];

-In addition, periodic continued fractions lead to circuits in which the range of values of the elements is less [16,17]. This is an important advantage because the provision of a large number of elements with different values (especially when these values are not standard) can be difficult and expensive.

As distinguished from most known studies [1-6], this work presents a time- and cost- effective method of synthesis that combines the advantages mentioned above. In Section 2 are presented two solutions of quadratic equation used to synthesize a circuit with an irrational impedance. The effect that the structure of the circuit realization, the number of elements and their tolerance has on the impedance of the circuit is subject to consideration of Section 3. Experimental results are presented and discussed in Section 4. Finally, conclusions are summarized in Section 5.

2. Syntesis of irrational impedance based on solutions of quadratic equations

Continued fractions, which represent recursively obtained solutions of the quadratic equations, can be very useful for synthesis of circuits with specific impedance. Let impedances $Z_a=Z_a(s)$ and $Z_b=Z_b(s)$ are positive real functions [17]:

-Z_a and Z_b are real when s is positive and real;

-Re[$Z_a(s)$]≥0 and Re[$Z_b(s)$]≥0 when Re[s]≥0.

It is our intention to present the synthesis of a passive one-port circuit with driving point impedance (DPI) equivalent to their geometrical mean:

$$Z = \sqrt{Z_a.Z_b} \tag{3}$$

where Z is a solution of the equation:

$$Z^2 = Z_a.Z_b \tag{4}$$

which can be solved in a number of different ways. Let's consider some of them. Multiplying both sides of Eqn (4) by two and after that adding the terms $(Z_a + Z_b).Z$:

$$2.Z^2 + (Z_a + Z_b).Z = (Z_a + Z_b).Z + 2.Z_a.Z_b, \tag{5}$$

the Eqn (5) can be rewritten as it follows:

$$(2.Z + (Z_a + Z_b)).Z = (Z_a + Z_b).Z + 2.Z_a.Z_b,$$

$$Z = \frac{(Z_a + Z_b).Z + 2.Z_a.Z_b}{2.Z + (Z_a + Z_b)}$$

or

$$Z = Z_b + \cfrac{1}{\cfrac{2}{Z_a - Z_b} + \cfrac{1}{Z_b + Z}}. \tag{6}$$

Recursively substituting this expression for Z back into itself yields a continued fraction:

$$Z = Z_a + \cfrac{1}{\cfrac{2}{Z_b - Z_a} + \cfrac{1}{Z_a + Z_a + \cfrac{1}{\cfrac{2}{Z_b - Z_a} + \cfrac{1}{Z_a + ...}}}} \tag{7}$$
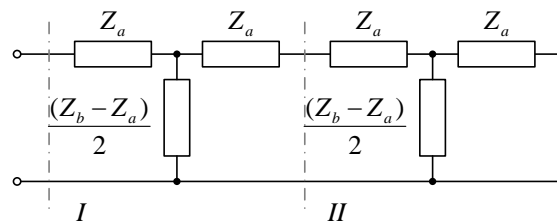

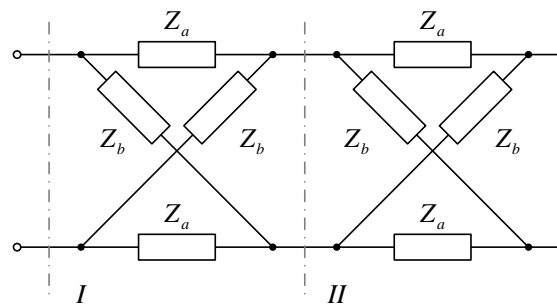**Figure 1.** Circuit of two cascaded T-sections

Figure 2. Circuit of two cascaded lattice sections

Table 1. Total number of impedances in a lattice network

DPI of a lattice network in the general case	Section	TNI
$Z_a + \dfrac{1}{\dfrac{2}{Z_b\text{-}Z_a} + \dfrac{1}{Z_a + Z_a + \cdots}}$	I	4
	II	8
	$\vdots$	$\vdots$
$+ \dfrac{1}{\dfrac{2}{Z_b\text{-}Z_a} + \dfrac{1}{Z_a}}$	N	4.N

Now let's consider the circuit shown in Fig.1. It presents two cascaded T-sections. When the right port is a short circuit the driving point impedance $Z_{PF}(s)$ of the entire network can be found easily by considering it in the right-to-left direction:

$$Z_{RF} = Z_a + \cfrac{1}{\cfrac{2}{Z_b - Z_a} + \cfrac{1}{Z_a + Z_a + \cfrac{1}{\cfrac{2}{Z_b - Z_a} + \cfrac{1}{Z_a}}}} \tag{8}$$

Each T-section can be transformed into a lattice section using Bartlett's theorem [18] as shown in Fig.2. It is easy to demonstrate that truncation of the continued fraction (7) at a suitable point will result in an approximation of the impedance Z which leads to a finite cascade lattice network. As shown in Table 1 the total number of impedances (TNI) necessary to implement a network of N symmetric lattices will be equivalent to 4N.

The presented form of a solution of the quadratic Eqn (4) is not unique. Taking into account Eqn (4), from Eqn (5) it is obtained:

$$2.Z^2 + (Z_a + Z_b).Z = Z^2 + (Z_a + Z_b).Z + Z_a.Z_b, \tag{9}$$

$$\left(2.Z + (Z_a + Z_b)\right).Z = (Z_a + Z).(Z_b + Z),$$

$$Z = \frac{(Z_a + Z).(Z_b + Z)}{(Z_a + Z) + (Z_b + Z)} \text{ or}$$

$$Z = \cfrac{1}{\cfrac{1}{(Z_a + Z)} + \cfrac{1}{(Z_b + Z)}} \tag{10}$$

Now we can apply the last equation to itself recursively to obtain the infinite continued fraction in the limit:

$$Z = \cfrac{1}{\cfrac{1}{Z_a + \cfrac{1}{\cfrac{1}{Z_a + ...} + \cfrac{1}{Z_b + ...}}} + \cfrac{1}{Z_b + \cfrac{1}{\cfrac{1}{Z_a + ...} + \cfrac{1}{Z_b + ...}}}} \tag{11}$$

The truncation of the continued fraction (11) at a suitable point will result in an approximation of the impedance Z which leads to a finite binary tree. This can be demonstrated using the example shown in Fig.3. The network begins with a bifurcation into two branches with impedances $Z_a(s)$ and $Z_b(s)$, which build the first generation. Each branch in the first generation then bifurcates into two new branches in the following generation. This bifurcation repeats for each generation. By moving from bottom to top into the network we will get the following:

$$Z = \cfrac{1}{\cfrac{1}{Z_a + \cfrac{1}{\cfrac{1}{Z_a} + \cfrac{1}{Z_b}}} + \cfrac{1}{Z_b + \cfrac{1}{\cfrac{1}{Z_a} + \cfrac{1}{Z_b}}}} \tag{12}$$

As shown in Table 2 the DPI of M-generational tree network consists of 2M+1-2 separate impedances.
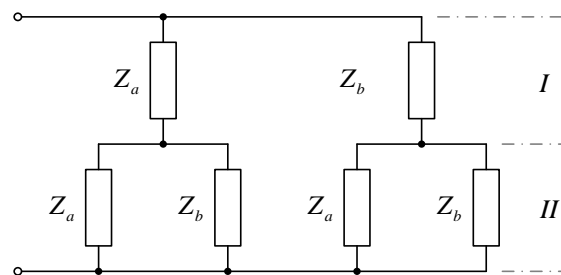

Figure 3. Circuit of two generational binary tree

Table 2. Total number of impedances in a tree network

DPI of a tree network in the general case	Generation	TNI
$\cfrac{1}{\cfrac{1}{Z_a+\cfrac{1}{\cfrac{1}{Z_a+\cdots}+\cfrac{1}{Z_b+\cdots}}}+\cfrac{1}{Z_b+\cfrac{1}{\cfrac{1}{Z_a+\cdots}+\cfrac{1}{Z_b+\cdots}}}}$	I	2
	II	6
	$\vdots$ N	$\vdots$ $2^{N+1}-2$

Figure 4. Magnitude error refers to specific realization of the lattice network.

Figure 5. Phase error refers to specific realization of the lattice network.
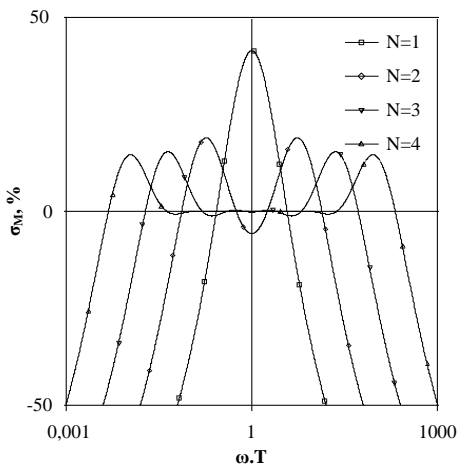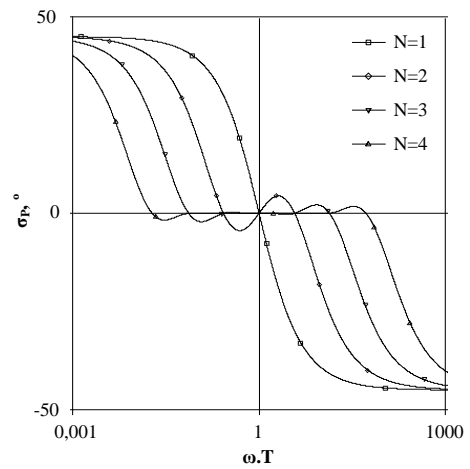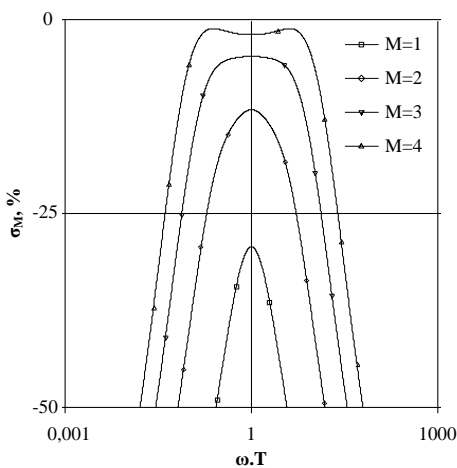

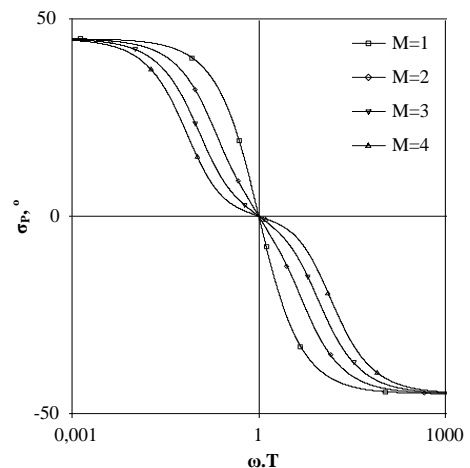**Figure 6.** Magnitude error refers to specific realization of the tree network.

Figure 7. Phase error refers to specific realization of the tree network.

3. Properties of Lattice and Tree structure network realization

Obtained in the previous section results are interesting from a theoretical point of view. The expressions:

$$Z(s) = A.\sqrt{s} \qquad (13)$$

and

$$Z(s) = \frac{1}{A.\sqrt{s}}, \qquad (14)$$

where A is a real number, represent some of the simplest irrational impedances. According to Eqn (3) infinite lattice or infinite tree structure network composed of resistances $Z_a = R$ and capacitors $Z_b = (s.C)^{-1}$ will have DPI as in Eqn (14) where:

$$A = \sqrt{\frac{C}{R}}. \qquad (15)$$

Unfortunately, real circuits contain a finite number of elements. When we are looking for proper practical realization it's important to know:
-the accuracy of approximation with a definite number of impedances (or elements);

Table 3. Magnitude and phase error when the circuit elements have a nominal value

σ'_M	σ'_P	Type	TNI
%	º		
68.5	39.3	Tree	2
41.4	39.3	Lattice	4
39.8	31.5	Tree	6
18.9	19.5	Lattice	8
18.4	22.8	Tree	14
15.0	3.16	Lattice	12
5.64	15.4	Tree	30
5.56	2.14	Lattice	16
0.95	1.52	Lattice	20
0.83	0.44	Lattice	24
0.47	0.12	Lattice	28
0.09	0.10	Lattice	32

Table 4. Magnitude and phase error when the circuit elements have a tolerance of 2%

σ'_M	σ'_P	Type	TNI
%	º		
69.2	39.5	Tree	2
43.8	39.5	Lattice	4
40.9	31.9	Tree	6
20.8	20.1	Lattice	8
19.6	23.3	Tree	14
16.5	3.70	Lattice	12
7.07	2.51	Lattice	16
6.94	15.9	Tree	30
2.48	1.86	Lattice	20
2.26	0.77	Lattice	24
1.93	0.49	Lattice	28
1.73	0.41	Lattice	32

Table 5. Magnitude and phase error when the circuit elements have a tolerance of 1%

σ'_M	σ'_P	Type	TNI
%	º		
68.9	39.4	Tree	2
42.6	39.4	Lattice	4
40.4	31.7	Tree	6
19.8	19.8	Lattice	8
19.1	23.1	Tree	14
15.7	3.40	Lattice	12
6.30	2.32	Lattice	16
6.23	15.7	Tree	30
1.65	1.71	Lattice	20
1.48	0.63	Lattice	24
1.15	0.32	Lattice	28
1.01	0.29	Lattice	32

Table 6. Magnitude and phase error when the circuit elements have a tolerance of 0,5%

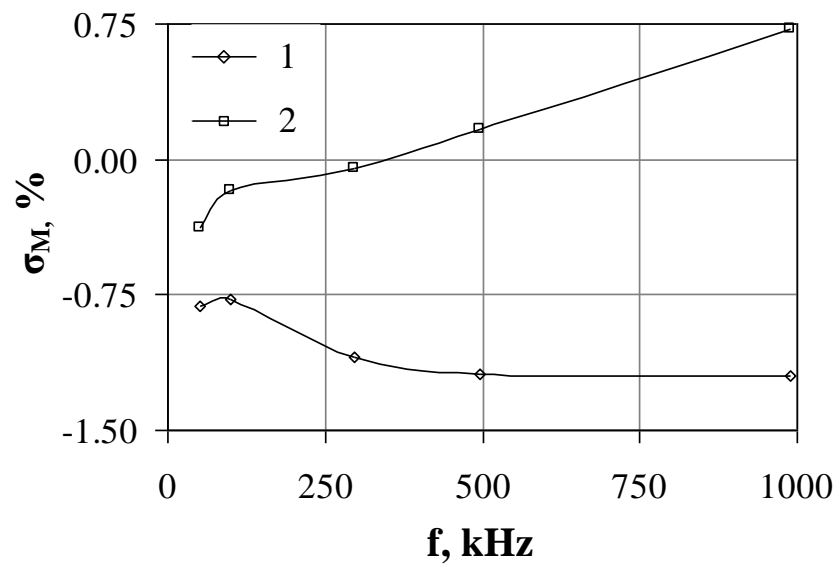| σ'_M	σ'_P	Type	TNI
%	º		
68.7	39.3	Tree	2
42.0	39.3	Lattice	4
40.1	31.6	Tree	6
19.4	19.4	Lattice	8
18.7	22.9	Tree	14
15.4	3.30	Lattice	12
5.94	15.6	Tree	30
5.91	2.23	Lattice	16
1.25	1.61	Lattice	20
1.13	0.53	Lattice	24
0.78	0.22	Lattice	28
0.46	0.19	Lattice	32

Figure 8. Curves 1 and 2 represent the magnitude error of the circuit realization before and after the impedance of C_i is subtracted from the $Z(s)$.
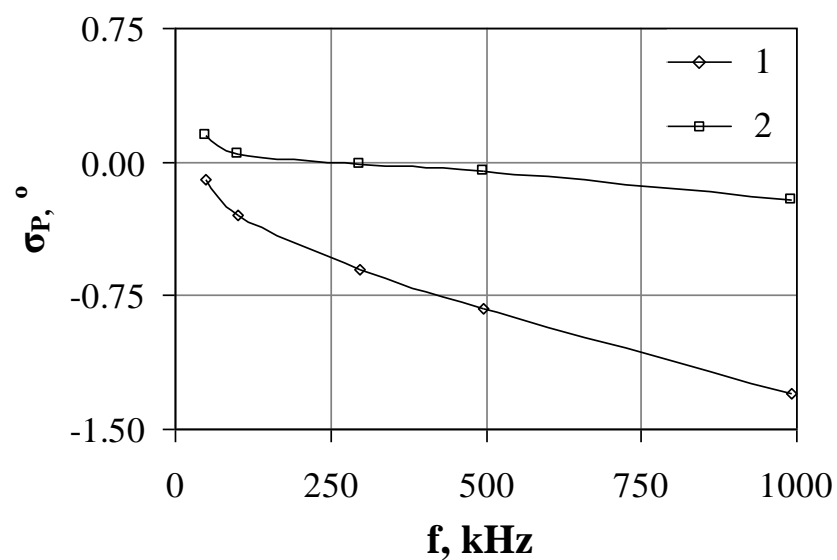

Figure 9. Curves 1 and 2 represent the phase error of the circuit realization before and after the impedance of C_i is subtracted from the $Z(s)$.

-the sensitivity of the network to changes of the impedance parameters.

Increasing the number of sections in the lattice structure or the number of generations in the tree structure will result in a DPI more close to Eqn (14). But this process is not the same for both structures. In Fig.4-7 are depicted the magnitude error

$$\sigma_M = \frac{|Z_{RF}| - |Z|}{|Z|} .100, \% \qquad (16)$$

and the phase error

$$\sigma_P = \angle Z_{RF} - \angle Z \qquad (17)$$

of some specific realization. These results were obtained using the PSpice. The maximum absolute value of σ_M and σ_P:

$$\sigma'_M = \max |\sigma_M| \qquad (18)$$

$$\sigma'_P = \max |\sigma_P| \qquad (19)$$

in the frequency interval $0,1 \leq \omega.T \leq 10$, $T = R.C$ is given in Table 3. It can be seen that the considered networks have the following features:
-when TNI does not exceed 32, the number of possible realizations is eight for a lattice and four for a tree network;
-when TNI is equal to eight or more, the lattice network achieves better σ'_M and σ'_P than the tree network at a smaller number of elements.

Manufacturing tolerances of the resistors and capacitors also affect the accuracy of realization. Monte Carlo analysis is perhaps the most well-known method for evaluating this influence. It is a purely statistical method in which the tolerance values are varied by a random algorithm over a number of simulation runs. Using PSpice Monte Carlo analysis the maximum value of σ'_M and σ'_P for a set of 300 runs is obtained. The results for the different tolerances are listed in Table 4-6.

4. Experimental results

Following previous recommendations the circuit of eight lattice section has been implemented. The resistors and capacitors have a nominal value of 4,3kΩ and 68pF respectively, and a tolerance of 0,5%. The input impedance of the circuit is measured by means of the impedance analyzer Agilent 4294A in a frequency interval 0,05÷1MHz. As shown in Fig.8 and Fig.9 the experimentally obtained errors σ'_M and σ'_P increase

with the increase in frequency and they are several times greater than the errors in Table 6. This is due to the frequency-dependent effects in the real resistors and capacitors, together with the strain immittance in the circuit performance. These phenomena are complex and difficult to predict. Taking into account that $\sigma_M < 0$ and $\sigma_P < 0$, we fit the experimental data to a simple model composed of impedance (14) and capacitor $C_i \approx 1.4pF$ in parallel. The value of C_i is found by minimizing the functional of weighted errors σ'_M and σ'_P

$$\psi = \sum_i \left[\left(\frac{\sigma'_M(f_i)}{0,46} \right)^2 + \left(\frac{\sigma'_P(f_i)}{0,19} \right)^2 \right], \qquad (20)$$

in the given frequency interval. If the impedance of C_i is subtracted from the input impedance of the circuit, the errors (16) and (17) will have almost the same values as those in Table 6.

5. Conclusion

Papers [19,20] describe synthesis of irrational impedance

$$\frac{1}{A.s^\alpha} \qquad (21)$$

of arbitrary order $0 \leq \alpha \leq 1$. Unfortunately, practical application of this method is difficult because the elements of the scheme have very different values. The lattice circuit and the tree circuit are constructed of identical resistors and capacitors. Both circuits present a solution of the same equation but have different properties. The lattice circuit can be implemented in more different variants and when the number of elements is equal to eight or more, it offers better accuracy. Experimental data showed that in the frequency interval 0,05÷1MHz the lattice circuit realization has an input impedance close to the irrational impedance $A^{-1}.s^{-0,5}$ in parallel with some capacitor C_i. The impact of C_i can be ignored if it does not need an accuracy presentation (in this case the magnitude and phase error do not exceed -1,2% and -1,3° respectively).

The results in this work were successfully used to research the effect that a constant phase element has on charge transfer processes in capacitive transducers and validation of measurement methods suitable for this case [20-22].

6. References

[1] B. Vinagre, I. Podlubny, A. Hernandez, "Some approximations of fractional order operators used in control theory and applications", Fractional Calculus and Applied Analysis, Vol. 3, No. 3, pp.231–248, 2000.

[2] A. Djouambi, A. Charef, A. Besançon1, "Approximation and synthesis of non integer order systems", 2nd IFAC

Workshop on Fractional Differentiation and its Applications, Porto, Portugal, pp.1-4, 2006.

[3] B. Krishna, Reddy K., "Active and passive realization of fractance device of order 1/2", Journal of Active and Passive Electronic Components, vol. 2008, p.5, 2008.

[4] L. Dorčák1, J. Terpák1, I. Petráš1, F. Dorčáková, "Electronic realization of the fractional-order systems", Acta Montanistica Slovaca, vol.12, pp.231-237, 2007.

[5] A. Djouambi, A. Charef, A. Besançon1, "Optimal approximation, simulation and analog realization of the fundamental fractional order transfer function", Int. J. Appl. Math. Comput. Sci., vol.17, No.4, p.455–462, 2007.

[6] A. Charef, "Modeling and analog realization of the fundamental linear fractional order differential equation", Nonlinear Dynamics, vol.46, pp.195-210, 2006.

[7] P. Sotiriadis, Y. Tsividis, "Integrators using a single distributed RC element", IEEE International Symposium on Circuits and Systems, Arizona, USA, vol.2, pp.21-24, 2002.

[8] A. Radwan, A. Soliman, A. Elwakil, "First order filters generalized to the fractional domain", Journal of Circuits Systems & Computers, vol.17, pp.55-66, 2008.

[9] M. Lima, J. Machado, M. Crisostomo, "Experimental signal analysis of robot impacts in a fractional calculus perspective", Journal of Advanced Computational Intelligence and Intelligent Informatics, vol.11, No.9, pp.1079–1085, 2007.

[10] I. Podlubny, "Fractional-order systems and fractional-order controllers", Slovak Academy of Sciences, Slovakia, UEF-02-94, 1994.

[11] F. Soulier, P. Lagonotte, "Modeling distributed parameter systems with discrete element networks", Proceedings of 15th International Symposium on the Mathematical Theory of Networks and Systems, University of Notre Dame, Indiana, USA, p.7, 2002.

[12] R. Burden, J. Faires, *Numerical analysis*, 8th edition, Cengage Learning, USA, p.864, 2005.

[13] W. Press, S. Teukolsky, W. Vetterling, B. Flannery, *Numerical Recipes in C: The Art of Scientific Computing*, Second Edition, Cambridge University Press, USA, p.994, 2002.

[14] J. Stoer, R. Bulirsch, *Introduction to numerical analysis*, Springer, USA, p.744, 2002.

[15] A. Sudhakar, S. Palli, *Circuits and Networks*, Tata McGraw-Hill Education, India, p.965, 2006.

[16] J. Chitode, Dr. Jalnekar, *Network Analysis and Synthesis*, Technical Publications, India, p.853, 2009.

[17] O. Wing, Chitode, Dr. Jalnekar, *Network Analysis Classical Circuit Theory*, Springer, USA, p.296, 2008.

[18] T. Iyer, *Circuit theory*, McGraw-Hill, p.520, 2006.

[19] Pl. Nikovski, N. Katrandziev, "Modelling of phase-constant element in PSpice environment", Scientific conference with international participation – Food science, Engineering and Technologies, Plovdiv, Bulgaria, pp. 430-435, 2009.

[20] Pl. Nikovski, "Improving the metrological characteristics of capacitive charge transfer transducers in the presence of constant phase element in the input", PhD thesis, Technical University, Sofia, Bulgaria, p.128, 2011.

[21] Pl. Nikovski, "A transfer function of a capacitive transducer in the presence of a phase constant element", Engineering Sciences, No.3, pp.12-21, 2010.

[22] Pl. Nikovski, I. Maslinkov, "Analysis of an equivalent CCPE connection diagram of the one-port circuit by square-wave voltage", International Scientific and Applied Science Conference Electronics, Sozopol, Bulgaria, p.197-199, 2009.

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