



A NOVEL CASCADED H- BRIDGE MULTILEVEL INVERTER BASED ON OPTIMAL PWM TECHNIQUE

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Abstract: In this paper, a novel cascaded H- bridge multilevel inverter has been proposed using less number of switches. A standard cascaded multilevel inverter requires $4h$ number of switches for $(2h + 1)$ levels whereas h is the number of dc sources. This proposed scheme allows less number of switches for the same level. A novel cascaded H- bridge multilevel inverter fed induction motor shows better performance due to fundamental frequency switching scheme using optimal PWM Technique (OPWM). High quality output is derived due to the absence of lower order harmonics. High conversion efficiency is also achieved for induction motor drive when it is operated with the proposed method. When the levels are increased, the number of switches used is very less compared to the conventional cascaded H-bridge multilevel inverter. The performance of three phase cascaded H- bridge multilevel inverter with equal dc sources is simulated by using MATLAB platform. Harmonic analysis is done on a novel cascaded H- bridge multilevel inverter with various levels.

Keywords: Equal dc sources, Fundamental frequency switching scheme, multilevel inverter, Total Harmonic Distortion (THD).

1. Introduction

The recent development in solid-state electronics is widely used in industries to control motor drives, computers and communications, power systems, switching mode power supplies, automotives etc. The inverter is one of the most extensive assemblies in power electronics. The main aspects for the development of multilevel inverters are multilevel voltage waveform, low total harmonic distortion and division of voltage to the switching devices [1]. Multilevel inverters have received high attention because of their reliable operation, high efficiency and low electromagnetic interference (EMI). The desired output of a multilevel converter is synthesized by several sources of dc voltages [2]–[8]. The use of multilevel inverters for high-voltage applications such as static var compensators [9], [10], active power filters [11] and adjustable-speed drives (ASDs) for medium-voltage induction motors [12]–[14] are increased in industries. Adjustable-speed drives have been used in several industry sectors such as the petrochemical, mining, water/waste, pulp and paper, cement, chemical, power generation, metal, and marine sectors. They are employed in equipment such as pumps, fans, compressors, blowers, extruders, conveyors, crushers and mills, rolling mills, mixers, propulsion, test beds, synchronous condensers, hoists and winders [15]. With an increasing number of dc voltage sources, the

inverter output voltage approaches nearly sinusoidal waveform while adopting a fundamental frequency switching scheme. Transformerless multilevel inverters are uniquely suited for this application because of the high VA ratings possible with these inverters [2].

Structure of the multilevel voltage source inverters allow them to reach high voltages with low harmonics without the use of transformers or series-connected synchronized switching devices. Multilevel inverters also have several advantages with respect to hard switched two level pulse width-modulation (PWM) variable-speed drives. Motor damage and failure have been reported by industry as a result of some variable-speed drives operated by the inverters having high rate of change of voltage (dv/dt), which produced a common-mode voltage across the motor windings. High frequency switching creates many problems because common-mode voltage is impressed numerous times upon the motor at each cycle. The main problems of high frequency switching are “failure of motor bearing” and “insulation breakdown in motor winding” because of dielectric stresses, circulating currents, voltage surge and corona discharge [16]–[18]. Multilevel inverters will be able to overcome these problems because their individual devices have a much lower stress per switching action. They can also operate at high efficiencies because they can switch at a much lower frequency than PWM-controlled inverters.

There are varieties of topologies available in multilevel inverters. They are diode-clamped, flying capacitor and H-

bridge cascaded multilevel inverter. Compared to flying capacitor multilevel inverter and diode-clamped multilevel inverter, the cascaded multilevel inverter needs less number of components and simple control methods. In high voltage fields, the cascaded multilevel inverters are widely used. The advantages of cascaded multilevel inverters are good output waveform, low switching stress. Its structure is suitable for modularization. Now a day, the existing PWM inverters are replaced by cascaded multi-level inverters [19]–[20]. In multilevel inverters, cascaded H-bridge multilevel inverter with unequal dc voltage sources is smart because it is not affected by capacitor voltage unbalancing. But switching devices are subjected to unequal voltage stress [21]–[22]. Multilevel inverter which uses bulk capacitors, need an adequate control or modulation strategy to balance the voltage in the capacitors [23]. Comparative studies regarding power loss comparison between three and four-level diode-clamped inverters [24], and involving a series-connected H-bridge cell inverter and a two-level inverter [25] have been reported. There are comparisons among flying-capacitor, diode-clamped and cascaded multilevel inverters [26]–[27] and among the three-level NPC, two-level, three-level and four-level flying-capacitor and five-level series connected H-bridge cells inverter [28]. Another study has compared two hybrid multilevel inverters with the same number of cells connected in series [29]–[30]. Hybrid asymmetrical and symmetrical multilevel inverters are compared in [31] with the same number of output voltage levels.

This paper presents a new topology of multilevel inverter which uses less number of switching devices and eliminates the need for capacitors. It exhibits several attractive features such as less components, simple circuit, modular structure. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. In this proposed work, a method is used to compute the switching angles for a multilevel converter so as to produce the required output voltage while at the same time cancel out specified higher order harmonics. Harmonic analysis is done on five level, seven level and eleven level less switch cascaded H-Bridge inverter. The proposed circuit generates a high-quality output voltage waveform and harmonic components of output voltage are low. It can also be extended to any number of levels.

2. A Novel Cascaded H- Bridge Multilevel Inverter Topology

A novel cascaded H-Bridge multilevel inverter topology has been proposed to reduce the number of switching devices in conventional cascaded H-Bridge multilevel inverter topologies. The general function of a multilevel inverter is to synthesize a desired voltage from separate dc sources, which may be obtained from fuel cells, batteries or ultracapacitors [32]. A generalized circuit configuration of a novel cascaded H- bridge multilevel inverter topology is shown in

Figure.1. The switches are arranged in the manner as shown in the figure. It has four main switches in H-bridge configuration S_1, S_2, S_3 and S_4 , and auxiliary switches (SA_1, SA_2, \dots, SA_n). The proposed topology need to add only one switch for every increase in levels. The number of dc sources is similar as in the symmetrical cascaded H-bridge multilevel inverter. A novel topology can be extended to any required number of levels like other conventional multilevel inverter topologies. The inverter output voltage waveforms of five level, seven level and eleven level are shown in Figure.2.

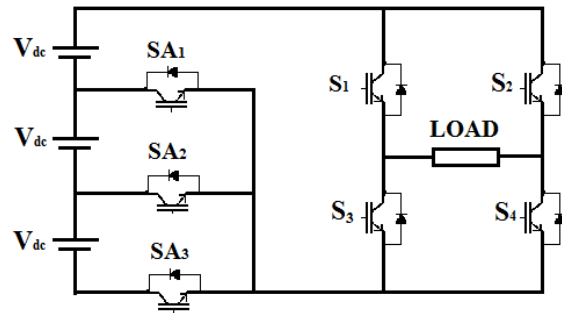


Figure 1. Single phase structure of a novel cascaded H- bridge multilevel inverter

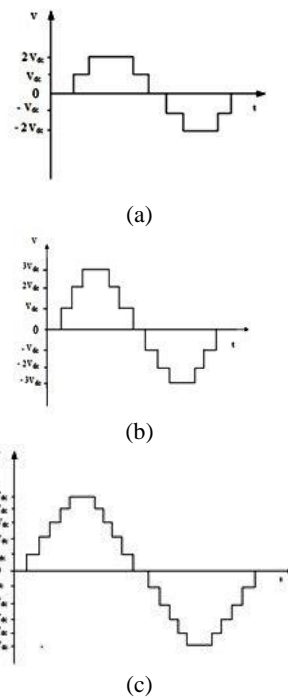


Figure 2. Output voltage waveform of (a) Five level inverter (b) seven level inverter (c) Eleven level inverter

For a novel cascaded H- bridge multilevel inverter with h number of equal dc sources, the following equations can be written:

$$N_L = 2h + 1 \tag{1}$$

$$V_{omax} = hV_{dc} \tag{2}$$

where, N_L, V_{omax} denote the number of output voltage levels, maximum output voltage respectively.

The proposed inverter consists of less number of switches when compared to the other topologies. The initial

cost reduces because of the switch reduction. So it is suitable for industrial applications.

3. Optimal PWM Technique

Pulse width modulation control or space vector PWM methods are widely used techniques in the multilevel inverter control. These conventional methods will cause extra losses due to high frequency switching. To overcome this problem, low switching control methods [33]–[34] are used. In this proposed method, fundamental frequency switching is used.

3.1 Five Level Inverter

Output voltage waveform given in the Figure.2 (a) can be evaluated by Fourier series expansion as given,

$$V(\omega t) = \frac{4 V_{dc}}{\pi} \times \sum_{n=1,5}^{\infty} \frac{1}{n} (\cos(n\theta_1) + \cos(n\theta_2)) \sin(n\omega t) \quad (3)$$

From equation (3), it is clear that 5th order harmonic can be eliminated. The triplen harmonics will get cancelled automatically in the three phase system. V_1 is the desired fundamental voltage. To determine the values of switching angles θ_1 and θ_2 , replace $V(\omega t)$ in equation (3) as $V_1 \sin(\omega t)$. In practice, it can be done approximately. In this case, the desire is to cancel the 5th order harmonics as they tend to dominate the total harmonic distortion. Mathematically, the statement of these conditions are expressed as,

$$\frac{4 V_{dc}}{\pi} (\cos \theta_1 + \cos \theta_2) = V_1 \quad (4)$$

$$\cos(5\theta_1) + \cos(5\theta_2) = 0 \quad (5)$$

3.2 Seven Level Inverter

Output voltage waveform given in the Figure.2 (b) can be evaluated by Fourier series expansion as given,

$$V(\omega t) = \frac{4 V_{dc}}{\pi} \times \sum_{n=1,5,7}^{\infty} \frac{1}{n} (\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3)) \sin(n\omega t) \quad (6)$$

From equation (6), it is clear that 5th and 7th order harmonics can be eliminated. Here V_1 is the desired fundamental voltage. To determine the values of switching angles θ_1 , θ_2 , and θ_3 , replace $V(\omega t) = V_1 \sin(\omega t)$ in the equation (6). In this case, the desire is to cancel the 5th and 7th order harmonics as they tend to dominate the total harmonic distortion. Mathematically, the statement of these conditions are expressed as,

$$\frac{4 V_{dc}}{\pi} (\cos \theta_1 + \cos \theta_2 + \cos \theta_3) = V_1 \quad (7)$$

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) = 0 \quad (8)$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) = 0 \quad (9)$$

3.3 Eleven Level Inverter

Output voltage waveform given in the Figure.2(c) can be evaluated by Fourier series expansion as given,

$$V(\omega t) = \frac{4 V_{dc}}{\pi} \times \sum_{n=1,5,7,11,13}^{\infty} \frac{1}{n} (\cos(n\theta_1) + \cos(n\theta_2) + \cos(n\theta_3) + \cos(n\theta_4) + \cos(n\theta_5)) \sin(n\omega t) \quad (10)$$

From equation (10), it is clear that 5th, 7th, 11th and 13th order harmonics can be eliminated. To determine the switching angle values θ_1 , θ_2 , θ_3 , θ_4 and θ_5 , substitute $V(\omega t) = V_1 \sin(\omega t)$ in equation (10). In this case, the desire is to cancel the 5th, 7th, 11th and 13th order harmonics as they tend to dominate the total harmonic distortion. Mathematically, the statement of these conditions are expressed as,

$$\frac{4 V_{dc}}{\pi} (\cos \theta_1 + \cos \theta_2 + \cos \theta_3 + \cos \theta_4 + \cos \theta_5) = V_1 \quad (11)$$

$$\cos(5\theta_1) + \cos(5\theta_2) + \cos(5\theta_3) + \cos(5\theta_4) + \cos(5\theta_5) = 0 \quad (12)$$

$$\cos(7\theta_1) + \cos(7\theta_2) + \cos(7\theta_3) + \cos(7\theta_4) + \cos(7\theta_5) = 0 \quad (13)$$

$$\cos(11\theta_1) + \cos(11\theta_2) + \cos(11\theta_3) + \cos(11\theta_4) + \cos(11\theta_5) = 0 \quad (14)$$

$$\cos(13\theta_1) + \cos(13\theta_2) + \cos(13\theta_3) + \cos(13\theta_4) + \cos(13\theta_5) = 0 \quad (15)$$

The transcendental equation set can be solved to get the unknowns θ_1 , θ_2 , θ_3 , θ_4 and θ_5 . The widely used methods are resultant theory method, iterative method such as the Newton-Raphson method [35]. MATLAB nonlinear solver can also be used to solve the above set of equations. Among all the methods, resultant theory method which produces possible solutions is selected to find the solutions of the above set of equations [33], [36]. The transcendental equations characterizing the harmonic content can be converted into polynomial equations. The resultant method is used to find the solutions when they exist. Total harmonic distortion (THD) is calculated for the arrived set of solutions to select the set which generates the lowest harmonic distortion (mostly due to the 11th and 13th harmonics). Switching angles for different levels of inverter used in the simulation is given in the Table 1. Percentage of voltage total harmonic distortion (THD) is defined by,

$$\text{THD}\% = \frac{\sqrt{V_3^2 + V_5^2 + V_7^2 + \dots + V_{19}^2}}{V_1} \times 100 \quad (16)$$

Table 1. Switching angles for different levels

Switching	Five Level	Seven	Eleven
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Angles		Level	level
θ_1	16.328°	8.7665°	6.571°
θ_2	52.328°	28.688°	18.944°
θ_3	-	54.939°	27.189°
θ_4	-	-	45.153°
θ_5	-	-	62.249°

The current total harmonic distortion (THD) is defined by,

$$THD\% = \frac{\sqrt{I_{rms}^2 + I_1^2}}{I_1} \times 100 \tag{17}$$

where I_{rms} and I_1 are the rms values of the output current and its fundamental component, respectively. The quality of the multilevel waveform depends on the selection of switching angles. Varying the switching angle to control the magnitude of rms value of output waveform also affects the total harmonic distortion (THD).

4. Simulation Study

The simulation of three phase novel cascaded H- bridge multilevel inverter fed three phase induction motor has been done using MATLAB/Simulink. The MOSFET switches are used as a switching device because of its high switching speed and low switching time. In the simulation study all the switches are considered to be ideal. The frequency of output voltage is 50 Hz. In practice, these dc voltage sources are available via distributed energy resources like photovoltaic panels. If the available source is an ac source, then the required dc voltage sources can be obtained by a transformer with multiple secondary windings and rectifiers [37]–[40]. There are different modulation strategies that can be applied for multilevel inverters. In this paper the fundamental frequency switching scheme is used. In this method, the switching angles can be obtained to eliminate some selected harmonics or minimization of total harmonic distortion. The spectrum of the output voltage is taken to determine the Total Harmonic Distortion (THD) of three phase induction motor drive. The main advantage of the multilevel inverter over conventional two level inverter is the voltage stress on each switch which has been reduced by the series connection of the switches. Simulation diagram of a novel cascaded H- Bridge inverter fed three phase induction motor is shown in Figure.3.

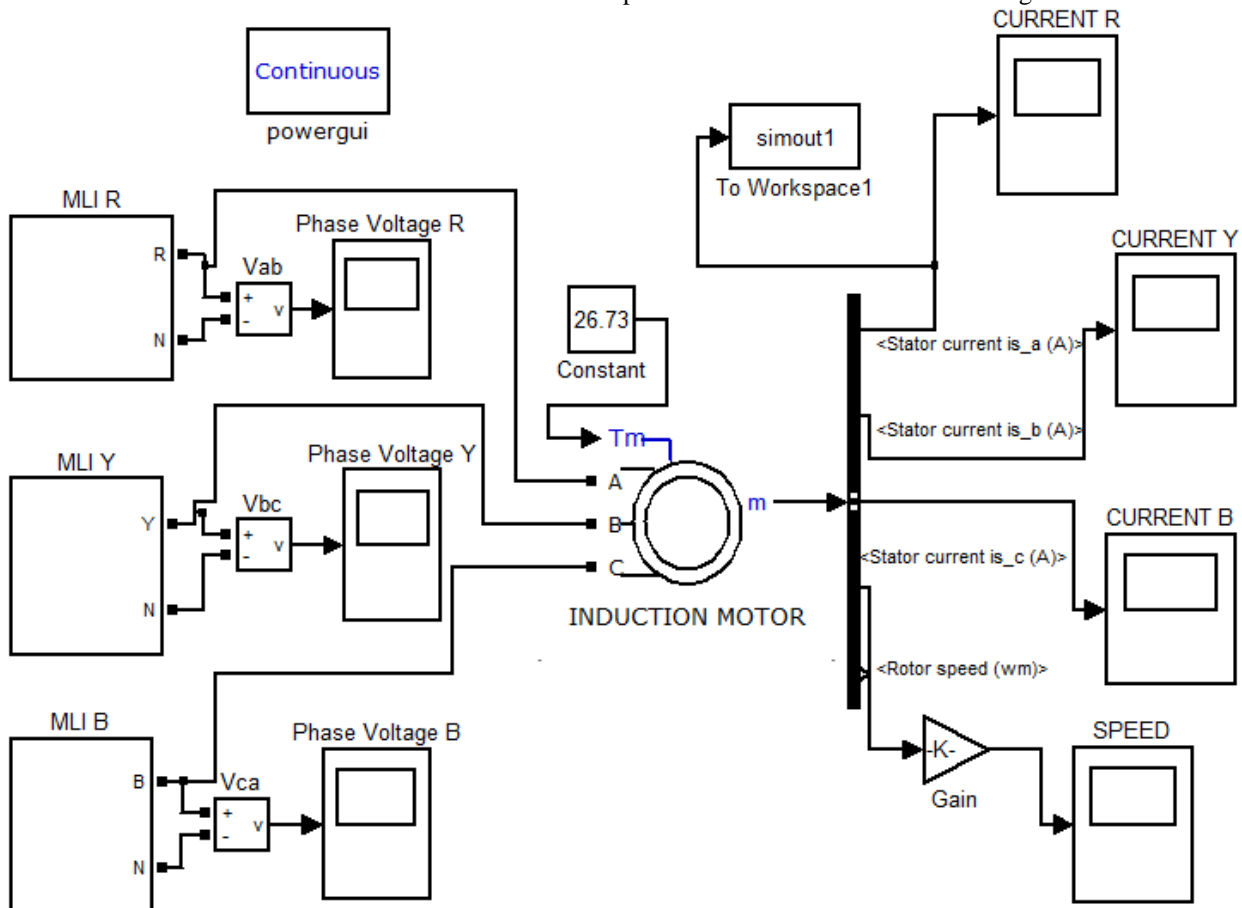
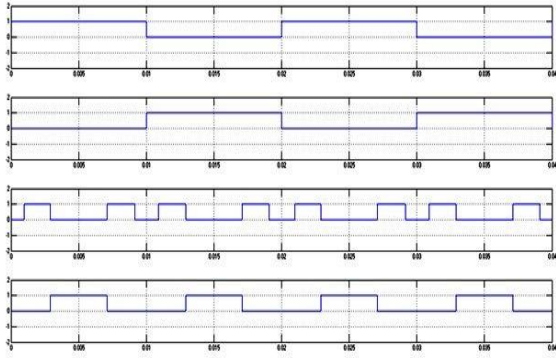


Figure 3. Simulation diagram of a novel cascaded H- Bridge multilevel inverter fed three phase induction motor

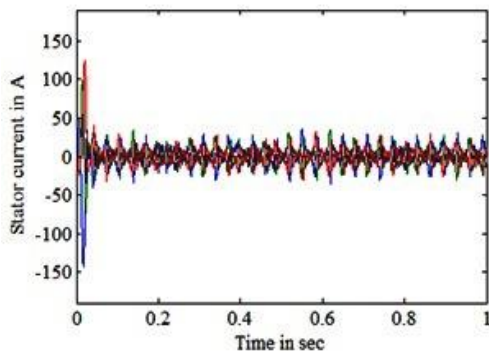
A novel cascaded H-Bridge multilevel inverter uses less switches to obtain the output voltage. More switches are required to achieve the same output

voltage in the symmetrical topology. The dc voltage sources used in the proposed topology are equal in magnitude. The simulation result of pulse waveform, stator current, three phase voltage and FFT spectrum of phase

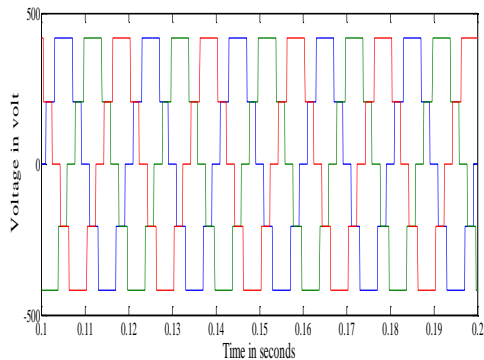
voltage for five level inverter, seven level inverter and eleven level inverter are presented in the Figure.4, Figure.5 and Figure.6. They clearly show that all of the desired voltage levels are generated. From the normalized FFT analysis shown in Figure.4(d) Figure.5(d) and Figure.6(d), it can be seen that the magnitude of lower order harmonics are very low and the magnitude of higher order harmonics are nearly equal to zero.



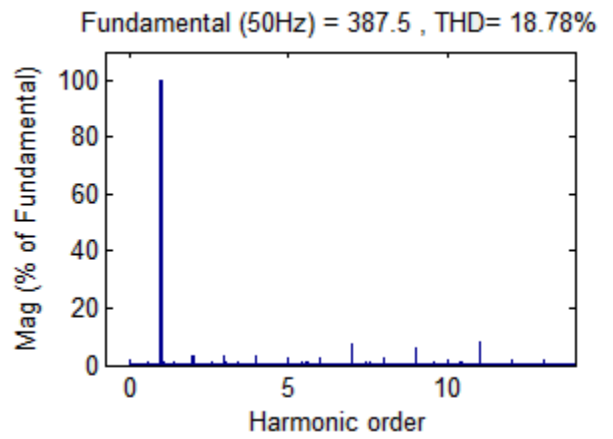
(a)



(b)

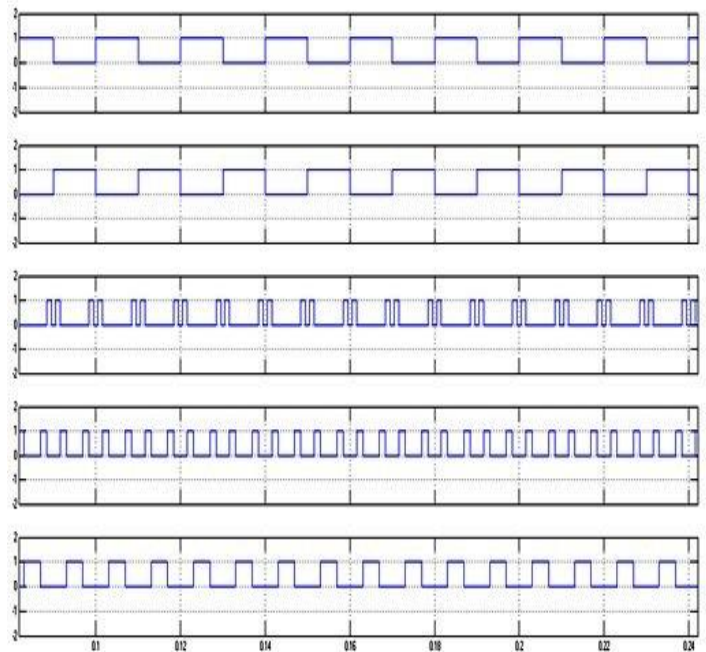


(c)

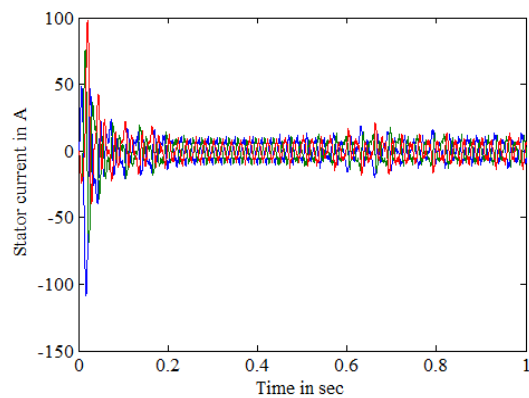


(d)

Figure 4. (a) Pulse waveform of a novel cascaded five level inverter (b) Stator current waveform (c) Three phase voltage waveform of five level inverter (d) FFT spectrum



(a)



(b)

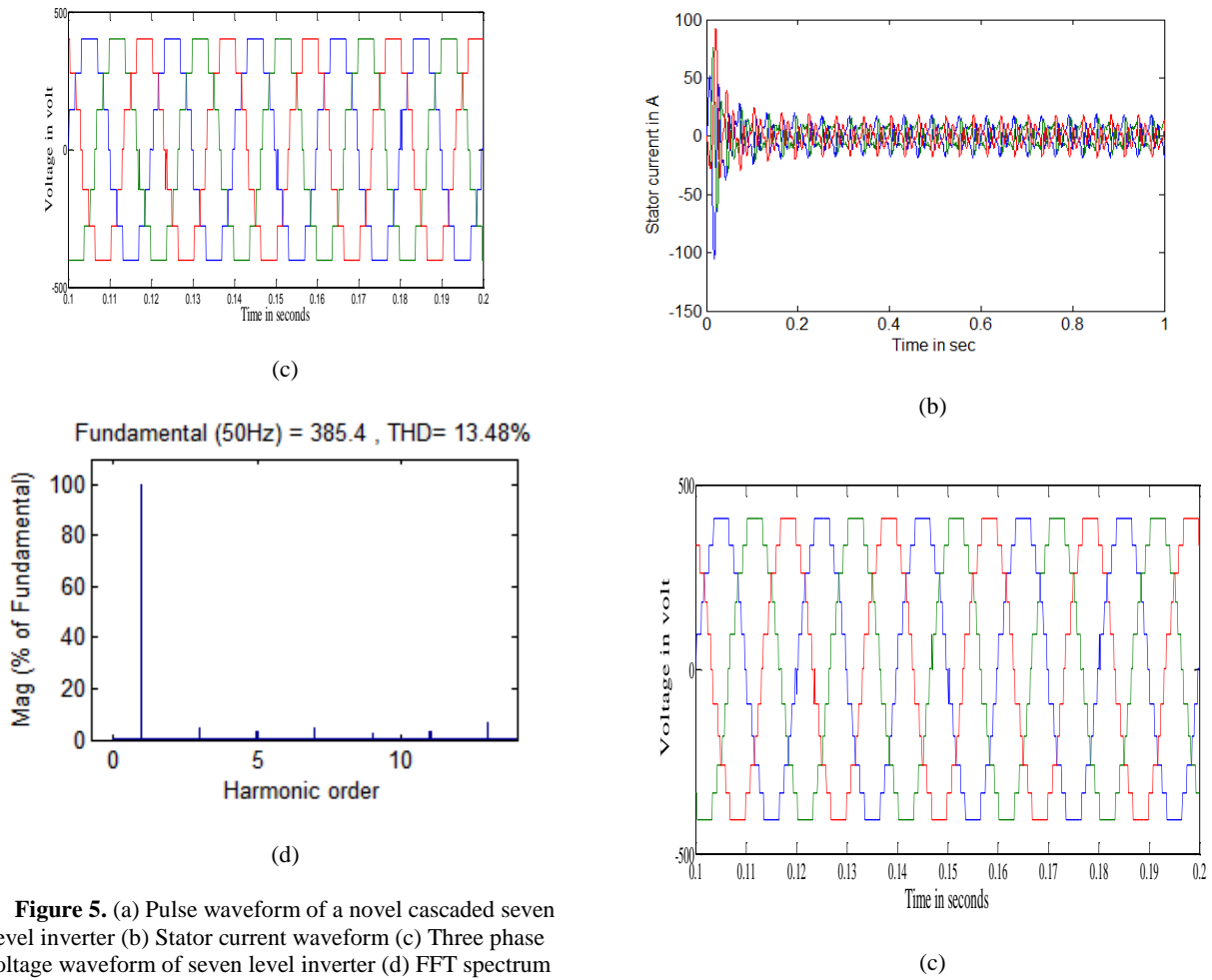


Figure 5. (a) Pulse waveform of a novel cascaded seven level inverter (b) Stator current waveform (c) Three phase voltage waveform of seven level inverter (d) FFT spectrum

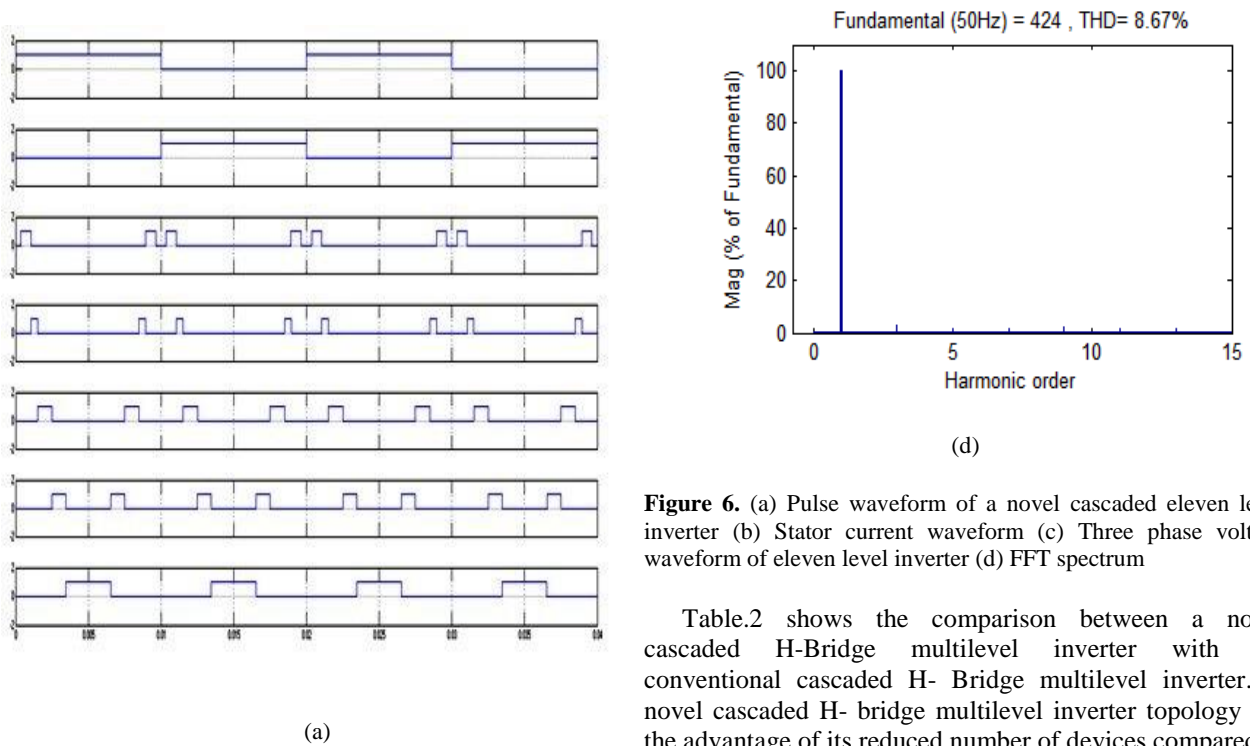


Figure 6. (a) Pulse waveform of a novel cascaded eleven level inverter (b) Stator current waveform (c) Three phase voltage waveform of eleven level inverter (d) FFT spectrum

Table.2 shows the comparison between a novel cascaded H-Bridge multilevel inverter with the conventional cascaded H- Bridge multilevel inverter. A novel cascaded H- bridge multilevel inverter topology has the advantage of its reduced number of devices compared to conventional cascaded H-bridge multilevel inverter and it can be extended to any number of levels.

Table 2. Comparison between a novel cascaded H- Bridge multilevel inverter and conventional cascaded H- Bridge multilevel inverter

Level	Number of switches		Percentage reduction of switches	THD %	
	Conventional cascaded H- Bridge Multilevel inverter	Novel cascaded H- Bridge Multilevel inverter		Conventional cascaded H- Bridge Multilevel inverter	Novel cascaded H- Bridge Multilevel inverter
5 - level	8	6	25%	19.36%	18.78%
7 - level	12	7	41.7%	14.45%	13.48%
11- level	20	9	55%	11.23%	8.67%

5. Conclusion

A novel cascaded H- bridge multilevel inverter fed three phase induction motor uses equal dc power sources for producing desired multilevel voltage is simulated. A fundamental frequency switching control algorithm was developed and implemented. The FFT analysis of phase voltage shows that the lower order harmonics have been reduced and also higher order harmonics are eliminated. The total harmonic distortion is reduced considerably. From the FFT spectrum, if number of levels is increased then considerably THD value gets reduced. Harmonic elimination reduces the heat generated in the stator winding of the induction motor. The torque of the induction motor is improved to a remarkable level due to the reduction of the harmonics which is the main cause for the production of negative torque. This proposed topology reduces the initial cost and complexity.

The proposed cascaded H- bridge multilevel inverter can be used for industries where the variable speed drives (conveyors, rolling mills, printing machines) are required and considerable amount of energy can be saved as the proposed system has lower harmonics.

6. References

- [1] Malinowski M, Gopakumar K, Jose Rodriguez & Marcelo A Perez, "A survey on Cascaded Multilevel inverters", *IEEE Trans.Ind.Elect.*, vol.57, pp.2197 – 2206, 2010.
- [2] J. S. Lai and F. Z. Peng, "Multilevel converters—A new breed of power converters", *IEEE Trans.Ind. Appl.*, vol.32, no.3, pp. 509–517, May/June 1996.
- [3] L.M. Tolbert, F. Z. Peng, and T. G. Habetler, "Multilevel converters for large electric drives", *IEEE Trans. Ind. Appl.*, vol.35, no. 1, pp.36–44, Jan./Feb. 1999.
- [4] M. Klabunde, Y. Zhao, and T. A. Lipo, "Current control of a 3 level rectifier/inverter drive system", in *Conference Record 1994 IEEE IAS Annual Meeting*, 1994, pp. 2348–2356.
- [5] W. Menzies, P. Steimer, and J. K. Steinke, "Five-level GTO inverters for large induction motor drives", *IEEE Trans.Ind.Appl.*, vol. 30, no. 4, pp.938–944, July 1994.
- [6] G. Sinha and T. A. Lipo, "A four level rectifier-inverter system for drive applications", in *Conference Record IEEE IAS Annual Meeting*, Oct 1996, pp. 980–987.
- [7] J. K. Steinke, "Control strategy for a three phase AC traction drive with three level GTO PWM inverter", in *IEEE Power Electronics Special Conference (PESC)*, 1988, pp.431– 438.
- [8] J. Zhang, "High performance control of a three level IGBT inverter fed AC drive", in *Conference Record IEEE IAS Annual Meeting*, 1995, pp. 22–28.
- [9] D. Soto and R. Peña, "Nonlinear control strategies for cascaded multilevel STATCOMs," *IEEE Trans. Power. Elect.*, vol. 19, no. 4, pp. 1919–1927, Oct. 2004.
- [10] Y. Liu, A. Q. Huang, W. Song, S. Bhattacharya, and G. Tan, "Small signal model-based control strategy for balancing individual DC capacitor voltages in cascade multilevel inverter-based STATCOM," *IEEE Trans. Ind. Elect.*, vol. 56, no. 6, pp. 2259–2269, Jun. 2009.
- [11] W. Ligiao, L. Ping, and L. Z. Zhongchao, "Study on shunt active filter based on cascade multilevel converter," in *Proceedings IEEE Power Electronics Special Conference Applications*, 2004, pp. 3512–3516.
- [12] M. Veenstra and A. Rufer, "Control of a hybrid asymmetric multilevel inverter for competitive medium-voltage industrial drives", *IEEE Trans.Ind. Appl.*, vol. 41, no. 2, pp. 655–664, Mar./Apr.2005.
- [13] A. Das, K. Sivakumar, R. Ramchand, C. Patel, and K. Gopakumar, "A combination of hexagonal and 12-sided

polygonal voltage space vector PWM control for IM drives using cascaded two-level inverters," *IEEE Trans. Ind. Elect.*, vol. 56, no. 5, pp. 1657–1664, May 2009.

- [14] A. Maheswari, S. Mahendran, I. Gnanambal, "Implementation of fundamental frequency switching scheme on multilevel cascaded H-bridge inverter fed three phase induction motor drive", *Wulfenia journal*, vol.19, no. 8, pp.10-23, Aug 2012.
- [15] A Guide to Standard Medium Voltage Variable Speed Drives: Part 1, ABB, Turgi, Switzerland, 2004.
- [16] S. Bell and J. Sung, "Will your motor insulation survive a new adjustable frequency drive?", *IEEE Trans. Ind. Appl.*, vol. 33, pp. 1307–1311, Sept./Oct. 1997.
- [17] J. Erdman, R. Kerkman, D. Schlegel, and G. Skibinski, "Effect of PWM inverters on AC motor bearing currents and shaft voltages", *IEEE Trans. Ind. Appl.*, vol. 32, pp. 250–259, Mar./Apr. 1996.
- [18] A. H. Bonnett, "A comparison between insulation systems available for PWM-inverter-fed motors", *IEEE Trans. Ind. Appl.*, vol.33, pp.1331–341, Sept./Oct. 1997.
- [19] Hurng-Liang Iou, Wen-Lung Chiang, et al., "Voltage-mode grid-connected solar inverter with high frequency isolated transformer", *IEEE International Symposium on Industrial Electronics*, 2009, pp.1087-1092.
- [20] Xianglian Xu, Qing Zhang, Qian Cheng, Youxin Yuan, Yiping Xiao, "An Auto-disturbance Rejection Controller for STATCOM Based on Cascaded Multilevel Inverters", *IEEE 6th International Power Electronics and Motion Control Conference*, Wuhan, China, DS11.4, 2009, 2349-2353.
- [21] Manjrekar MD, Lipo TA. "A hybrid multilevel inverter topology for drive applications", *Proceeding IEEE International Conference*, 1998, 2:523–9.
- [22] Manjrekar MD, Steimer PK, Lipo TA. "Hybrid multilevel power conversion system: a competitive solution for high-power applications", *IEEE Trans. Ind. Appl.*, vol.36, no.3, pp. 834–841, 2000.
- [23] Marchesoni M, Tenca P. "Diode-clamped multilevel converters: a practicable way to balance DC-link voltages", *IEEE Trans. Ind. Electron.*, vol. 49, no.4, pp.752–65, 2002.
- [24] T. J. Kim, D. W. Kang, Y. H. Lee, and D. S. Hyun, "The analysis of conduction and switching losses in multi-level inverter system," in *Proceedings, 32nd Power Electronics Special Conference Applications*, 2001, pp. 1363–1368.
- [25] A. M. Massoud, S. J. Finney, and B. W. Williams, "Multilevel converters and series connection of IGBT evaluation for high-power, high-voltage applications," in *Proceedings, 2nd Power Electronics Machines Drives Conference*, 2004, pp. 1–5.
- [26] S. Bernet, D. Krug, S. S. Fazel, and K. Jalili, "Design and comparison of 4.16 kV neutral point clamped, flying capacitor and series connected H-bridge multi-level converters," in *Conference Record 40th IEEE IAS Annual Meeting*, 2005, pp. 121–128.
- [27] S. S. Fazel, S. Bernet, D. Krug, and K. Jalili, "Design and comparison of 4-kV neutral-point-clamped, flying-capacitor, ad series-connected H-bridge multilevel inverters," *IEEE Trans. Ind. Appl.*, vol.43, no. 4, pp. 1032–1040, Jul. 2007.
- [28] J. Rodríguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Elect.*, vol. 54, no.6, pp. 2930–2945, Dec. 2007.
- [29] D. Krug, S. Bernet, S. S. Fazel, K. Jalili, and M. Malinowski, "Comparison of 2.3-kV medium-voltage multilevel converters for industrial medium-voltage drives," *IEEE Trans. Ind. Elect.*, vol. 54, no. 6, pp. 2979–2992, Dec. 2007.
- [30] D. A. B. Zambra, C. Rech, and J. R. Pinheiro, "Selection of DC sources for three cells cascaded H-bridge hybrid multilevel inverter applied to medium voltage induction motors," in *Proceedings 8th Brazilian Power Electronics Conference*, 2005, pp. 211–216.
- [31] D. A. B. Zambra, C. Rech, and J. R. Pinheiro, "A comparative analysis between the symmetric and the hybrid asymmetric nine-level series connected H-bridge cells inverter," in *Proceedings 12th European Conference on Power Electronics Applications*, 2007, pp. 1–10.
- [32] F. Z. Peng, J. S. Lai, J. W. McKeever, and J. Van Covering, "A multilevel voltage-source inverter with separate dc sources for static var generation", *IEEE Trans. Ind. Appl.*, vol.32, pp.1130–1138, Sept./Oct. 1996.
- [33] Chiasson, J. N., Tolbert, L. M., Mckenzie, K. J. & Du Z., (2003), "Control of a Multilevel Converter Using Resultant Theory", *IEEE Trans. Cont. Sys. Theory*, Vol.11, No.3, pp. 345-354.
- [34] Z. Du, L.M.Tolbert and J. N. Chaisson, "Modulation extension control for multilevel converters using triplen harmonic injection with low switching frequency", in *Proceedings, IEEE Power Electronics Conference*, Austin, TX, Mar. 6-10, 2004, pp. 419- 423.
- [35] Patel, H. S. & Hoft, R. G., "Generalized Techniques of Harmonic Elimination and Voltage Control in Thyristor Inverters: Part I – Harmonic Elimination", *IEEE Trans. Ind. Appl.*, 3, pp. 310-317, 1973.
- [36] J. Chiasson, L. Tolbert, K. McKenzie, and Z. Du, "Elimination of harmonics in a multilevel converter using the theory of symmetric polynomials", *IEEE Trans. Cont. Sys. Tech.*, vol. 13, no. 2, pp. 216–223, Mar. 2005.
- [37] J. Ebrahimi, E. Babaei, G.B. Gharehpetian, "A new multilevel converter topology with reduced number of power electronic components", *IEEE Trans. Ind. Elect.*, vol.59, no.2, pp.655–667, 2010.
- [38] J. Dixon, J. Pereda, C. Castillo, S. Bosch, "Asymmetrical multilevel inverter for traction drives using only one dc supply", *IEEE Trans. Vehi. Tech.*, vol.59, no.8, pp.3736–3743, 2010.
- [39] J. Pereda, J. Dixon, "High-frequency link: a solution for using only one dc source in asymmetric cascaded multilevel inverters", *IEEE Trans. Ind. Elect.*, vol.58, no.9, pp.3884–3892, 2011.
- [40] J. A. Sayago, T. Brückner, and S. Bernet, "How to select the system voltage of MV drives—A comparison of semiconductor expenses", *IEEE Trans. Ind. Elect.*, vol. 55, no.9, pp.3381–3390, Sep. 2008.



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