

DESIGN AND IMPLEMENTATION OF HYBRID SPWM CONTROL FOR CASCADED H-BRIDGE MULTI LEVEL INVERTER FOR MOTOR DRIVES



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Abstract: In this paper, present the performance of hybrid modulation technique for soft switched cascaded five level inverters. The proposed modulation schemes are hybrid alternative phase opposition, hybrid phase shift carrier, hybrid single carrier sinusoidal PWM schemes. It inherits the switching loss reduction along with reduced harmonic performance of cascaded multilevel inverter fed drive system. The inverter topology used here has recently suggested in the area of high power medium voltage applications. The performance of this cascaded inverter has been analysed and compared with the results obtained from theory and simulation. Simulation study of the inverter employing the proposed HAPOD, HPSCPWM, HSCSPWM strategy has been done in MATLAB/SIMULINK. Among these three modulation schemes the efficient strategy is employed in the hardware implementation of hybrid multilevel inverter.

Keywords: Cascaded multilevel inverter, Hybrid alternative phase opposition disposition (HAPOD), Hybrid phase shift carrier (HPSC), Hybrid single carrier sinusoidal PWM (HSCSPWM), switching loss.

1. Introduction

Multilevel inverter has emerged recently in the area of high power medium voltage applications due to their advantages such as output waveform improvement which reduces the harmonic content in turn it reduces the size and cost of the filter and the level of electromagnetic interference (EMI) generated by switching operation. Multilevel inverters are of three types mainly; Diode clamped multilevel inverter, Flying capacitor multilevel inverter and Cascaded multilevel inverter [3-5]. Among these three topologies cascaded multilevel inverters are most preferable since it overcomes the disadvantages of the other inverters. The main features of CMLI are

- 1. The level of extension is easy.
- 2. No voltage unbalancing problem.
- 3. It has modular structure.

Received on: 18.04.2013 Accepted on: 25.03.2014 New modulations are newly developed to generate a stepped switched waveform with high power quality and minimum switching frequency [1]. In this paper we proposed a new hybrid alternative phase opposition disposition modulation scheme to produce an efficient output voltage. The proposed system can be also used in wind energy system applications like satisfy electrical demand in stand alone modes [9].

2. Sequential Switching Cascaded Five Level Inverter

The proposed five level inverter consists of two hybrid cells with separate DC source [7]. Each cell is made of full bridge inverter which has four sequential switching IGBT switches.

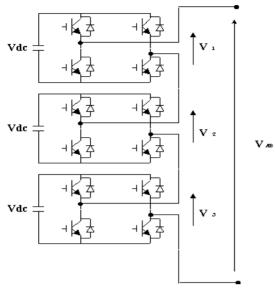


Figure 1. Cascaded five level inverter topology

Proper sequential switching of inverter produces five level output voltages (2V, V, 0,-V,-2V). Sequential switching states of this proposed hybrid inverter is given in the Table 1.

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OUTPUT VOLTAGE	S1	S2	S3	S4	S1`	S2`	S3`	S4`	
2V	1	0	0	1	1	0	0	1	
V	0	1	0	1	1	0	0	1	
0	0	1	1	0	1	0	0	1	
-Vss	0	1	1	0	1	0	1	0	
-2V	0	1	1	0	0	1	1	0	

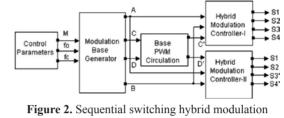
Table 1. Switching state of inverter

3. Hybrid Modulation Strategy

3.1. Modulation Scheme

The hybrid modulation meant in this paper is the combination of fundamental frequency modulation (FPWM) and multiple sinusoidal modulation (MSPWM).

The obtained output has both the features such as reduction in switching loss from FPWM and good harmonic performance from MSPWM. This proposed hybrid modulation along with sequential switching and simple base PWM circulation scheme produces balanced power dissipation among the power modules. It consists of base generator, base PWM circulation module and hybrid modulation controller as shown in Figure 2. The control parameters are fundamental frequency fo, carrier frequency fc and modulation index M=Am/KAc.



scheme

3.2. Base Modulation Design

Each cell needs three base modulation pulses and they are

- i. Sequential switching pulse (SSP) denoted as 'A' which is a square wave pulse with half of fundamental frequency.
- ii. Fundamental modulation pulse (FPWM) is a square wave signal synchronized with the modulation signal is denoted by 'B'.
- iii. Multiple sinusoidal modulation pulse (MSPWM)-In this paper we used three different modulation schemes.

In APOD all the carriers are phase opposition by 180 degree from its adjacent carrier as shown in Figure 3.

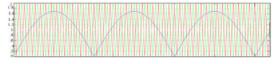


Figure 3. APOD waveform

For cell 1 APOD signal 'c' is generated by comparing the unipolar modulation waveform with the carrier. For cell 2 APOD signal 'D' is obtained from comparison between the carrier with dc bias of –Vc+2Ac and unipolar modulation signal. In PSC, sinusoidal reference waveforms for the two phase legs of each full bridge inverter are phase shifted by 180° then phase shift the carriers of each bridge as shown in Figure 4.

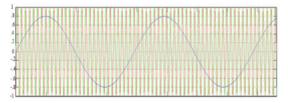


Figure 4. PSC waveform

Phase shift carrier signals are generated from the comparison of modulation waveform with corresponding PSC waveform. In N level SCSP-WM, there are K number of modulation signals with same frequency and amplitude and has a dc bias of Ac as a difference between these signals and one carrier signal as shown in Figure 5.

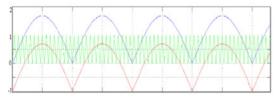


Figure 5. SCSPWM waveform

Simulink representation of generating SCSP-WM signal is given in below Figure 6.

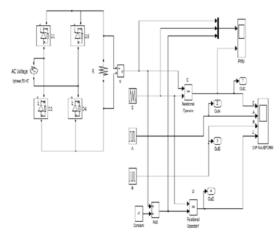


Figure 6. SCSPWM simulink representation

3.3. Base PWM Circulation

A simple base PWM circulation scheme is used to obtain hybrid PWM among the power modules. It consists of two 2:1 mux which select one of the two PWM signals based on the select clock signal. Clock frequency used here is fo/4 to circulate the PWM from one module to another. The order of the HPWM module is changed after each two fundamental frequency period (ie) first module becomes the second and the second module shifts to first.

3.4. Hybrid Modulation Controller

Sequential switching hybrid modulation pulses are generated by hybrid modulation controller by combining the SSP,FPWM and MSPWM signals. It is designed by a simple combination logic and it is expressed as,

$S1 = ABC' + \overline{A}B$		$S1' = ABD' + \overline{A}B$
$S2 = A\overline{B}C' + \overline{A}\overline{B}$	and	$S2' = A\overline{B}D' + \overline{A}\overline{B}$ $S3' = \overline{A}\overline{B}D' + A\overline{B}$
$S3 = \overline{A} \overline{B}C' + A\overline{B}$		$S3' = \overline{A} \overline{B} D' + A \overline{B}$
$S4 = \overline{A}BC' + AB$		$S4' = \overline{A}BD' + AB$

Where A is SSP signal, B is FPWM signal, C' is MSPWM signal for cell 1 and D' is MSP-WM signal for cell 2. The MATLAB/ SIMULINK model for HMC is designed as subsystem and it is given in Figure 7.

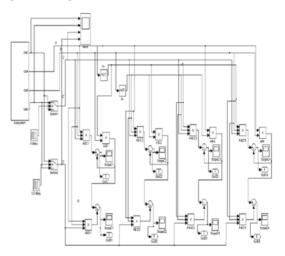


Figure 7. Simulink for combinational logic of HMC

4. Simulation Results

Cascaded five level inverter operation and its results at various load conditions are studied and discussed below. The block diagram of five level cascaded inverter with three different modulation schemes are shown in Figure 8.

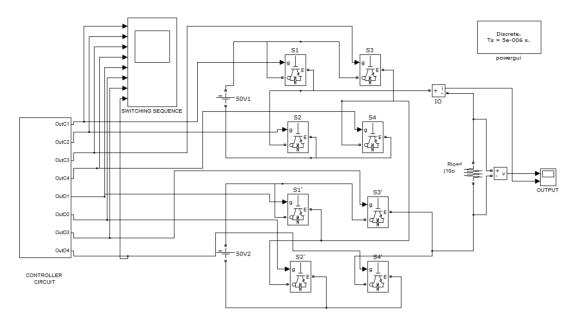


Figure 8. Simulink for cascaded five level inverter

The switching sequence waveform of each switch S1 through S4 and S1' through S4' is shown in Figure 9.

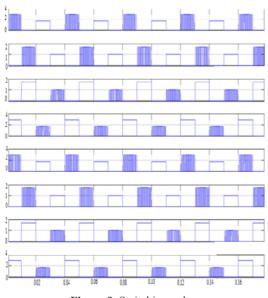


Figure 9. Switching pulses

From the waveform we can observe that gate pulse of each switch has both FPWM and MSP-WM signals. The input voltage applied is 50V and the load resistance is 10ohms, inductance 5mH, the corresponding output voltage and current of the proposed inverter is shown in Figure 10.

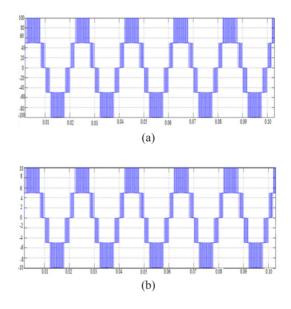
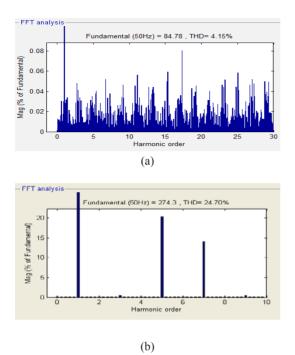


Figure 10. (a) output voltage (b) output current

For HAPOD, the total harmonic distortion THD for the output voltage using the R load is about 4.15% and for RL load it is about 13.06%. The Harmonic spectra of the output voltage waveform in the linear modulation region of (M=0.8) is shown in Figure 11.



For HSCSPWM, we are obtaining THD for R load is about 56.19% and for RL load is 59.24% The Harmonic spectra of output voltage waveforms are shown in Figure 13.

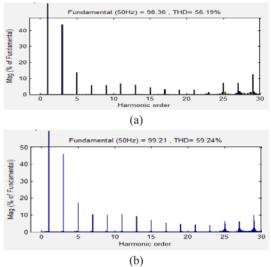
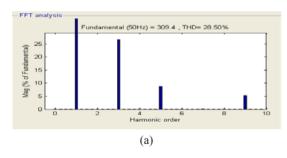


Figure 11. HAPOD Harmonic spectrum of output voltage using a) R load b) RL load

For HPSCPWM, we are obtaining THD for R load is about 28.50% and for RL load is 81.28% The Harmonic spectra of output voltage waveforms are shown in Figure 12.



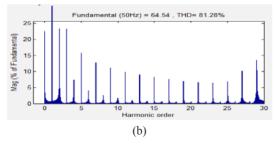


Figure 12. HPSCPWM Harmonic spectrum of output voltage using a) R load b) RL load

Figure 13. HSCSPWM Harmonic spectrum of output voltage using a) R load b) RL load

Varying the modulation index from 0.4 to1.2.

5. Hardware Implementation

The hardware implementation of cascaded five level inverter using the efficient hybrid alternative phase opposition disposition modulation scheme has been built using FGA25N120 IGBT for the full bridge inverter and CSD100060 diode as the switching devices and the gate pulses are generated using the PIC18F4550 microcontroller. The experimental setup is shown in Figure 14.

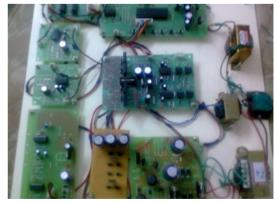


Figure 14. Hardware implementation of cascaded five level inverter

The load voltage of cascaded five level inverter for R load in the hardware setup is shown in Figure 15.

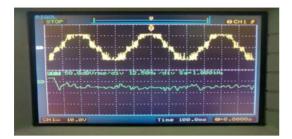


Figure 15. Five level output voltage

6. Conclusions

In this paper, a sequential switching hybrid modulation techniques for cascaded five level inverter are proposed. The output voltage and current waveforms are obtained for R and RL load. The Harmonic performance of this proposed scheme is analysed in the linear range of modulation index and it seems to be efficient for HA-POD. Hybrid modulations embedded with PWM circulation produces balanced power dissipation among the switches within the cell as well as series connected cells. This proposed efficient modulation scheme is implemented using FGA25N120 IGBT, CSD100060 Diode and gate signals are generated using PIC18F4550 microcontroller. It can be easily extended to higher voltage level.

7. References

 J. Rodriguez, S. Bernet, B. Wu, J. O. Pontt, and S. Kouro, "Multilevel voltage-source-converter topologies for industrial medium-voltage drives," *IEEE Trans. Ind. Electron., vol.* 54, no. 6, pp. 2930–2945, Dec.2007.

- [2] J. Rodr'ıguez, J. S. Lai, and F. Z. Peng, "Multilevel inverters: A survey of topologies, controls and applications," *IEEE Trans. Ind. Electron.*, vol. 49, no. 4, pp. 724–738, Aug. 2002.
- [3] M.Malinowski, K. Gopakumar, J. Rodr'Iguez, andM. A. Perez, "A survey on cascaded multilevel inverters," *IEEE Trans. Ind. Electron.*, vol. 57, no. 7, pp. 2197–2206, Jul. 2010.
- [4] R. Gupta, A. Ghosh, and A. Joshi, "Switching characterization of cascaded multilevel-inverter-controlled systems," *IEEE Trans. Ind. Electron., vol. 55, no. 3, pp. 1047–1058, Mar. 2008.*
- [5] C. Govindaraju and K. Baskaran, "Efficient hybrid carrier based space vector modulation for cascaded multilevel inverter," J. Power Electron., vol. 10, no. 3, pp. 277–284, May 2010.
- [6] S. Kouro, J. Rebolledo, and J. Rodriguez, "Reduced switching frequency modulation algorithm for high-power multilevel inverters," *IEEE Trans.Ind. Electron., vol. 54, no. 5, pp.* 2894–2901, Oct. 2007.
- [7] Martha Calais, Lawrence J. Borlel Vassilios, G. Agelidis "Analysis of Multicarrier PWM Methods for a Single-phase Five Level Inverter", IEEE Transactions on Power Electronics, July 2001, pp 1351-1356.
- [8] Zhou Jinghua and Li Zhengxi, "Research on Hybrid Modulation Strategies Based on General Hybrid Topology of Multilevel Inverter", International symposium on Power Electronics Electrical Drives, Automation & Motion, IEEE Conf. Rec: 978-1-4244-1664-6, pp.784-788, 2008.
- [9] Sasikumar M. and Chenthur Pandian S. (2011), 'Modeling and Analysis of Cascaded H-Bridge Inverter for Wind Driven Isolated Self – Excited Induction Generators,' *International Journal on Electrical Engineering and Informatics (IJEEI), ISSN: 2085-6830, Vol.3, No. 2, 2011, pp. 132-145.*



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