IMPLEMENTATION OF NEW H- BRIDGE MULTILEVEL INVERTER USING A COMBINATION OF HIGH FREQUENCY AND LOW FREQUENCY MODULATION

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Abstract: *This paper proposes a seven level inverter with photovoltaic system, for stand-alone applications with hybrid PWM control scheme. Three carrier signals that are identical to each other which are compared with unidirectional sinusoidal reference signal were used to generate the PWM signals. In this paper, a new topology with a combination of low frequency and high frequency switches is proposed to improve the performance of a multilevel inverter. This topology requires fewer components compared to existing inverters and requires fewer carrier signals and gate drives. Therefore, the overall cost and complexity are greatly reduced. The performance of proposed multilevel inverter with equal dc sources is simulated by using MATLAB platform. Harmonic analysis is done on H-Bridge seven level inverter and experimental results are presented to demonstrate the superiority of the proposed system.*
Keywords: *Equal dc sources, Fundamental frequency switching scheme, multilevel inverter, PWM, Total Harmonic Distortion (THD).*

1. Introduction

Due to lack of non-renewable energy sources, high cost and pollutions created by the power stations have made to move researchers towards renewable energy sources. One of the renewable energy sources is solar. By using photovoltaic system, solar energy is directly converted into electricity. This energy can be delivered to power grid through inverters. The main aspects for the development of multilevel inverters are multilevel voltage waveform, low total harmonic distortion (THD) and division of voltage to the switching devices [1]. Multilevel inverters have received high attention because of their reliable operation, high efficiency and low electromagnetic interference (EMI). The desired output of a multilevel inverter is synthesized by several sources of dc voltages [2]–[8]. A single phase grid connected photovoltaic systems uses multilevel converters for low power applications [9]. Varieties of photovoltaic based grid connected inverters are discussed in the literature [10].

There are varieties of topologies available in multilevel inverters. They are diode-clamped, flying capacitor and H-bridge cascaded multilevel inverters. Compared to flying capacitor multilevel inverter and diode-clamped multilevel inverter, the cascaded multilevel inverter needs less number of components and simple control methods. In high voltage fields, the cascaded multilevel inverters are widely used. The advantages of cascaded multilevel inverters are good output waveform, low switching stress. Its structure is suitable for modularization. Now a day, the existing PWM inverters are replaced by cascaded multi-level inverters [11]–[12]. In multilevel inverters, cascaded H-bridge multilevel inverter with unequal dc voltage sources is smart because it is not affected by capacitor voltage unbalancing. But switching devices are subjected to unequal voltage stress [13]–[14]. Multilevel inverter which uses bulk

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capacitors, need an adequate control or modulation strategy to balance the voltage in the capacitors [15]. Comparative studies regarding power loss comparison between three and four level diode-clamped inverters [16] and involving a series connected H-bridge cell inverter and a two-level inverter [17] have been reported. There are comparisons among flying-capacitor, diode-clamped and cascaded multilevel inverters [18]–[19] and among the three-level NPC, two-level, three-level and four-level flying-capacitor and five-level series connected H-bridge cells inverter [20]. Another study has compared two hybrid multilevel inverters with the same number of cells connected in series [21]. Hybrid asymmetrical and symmetrical multilevel inverters are compared in [22] with the same number of output voltage levels and three multilevel inverter topologies are compared in [23] with the same output filter.

This paper presents a new topology of multilevel inverter which uses less number of switching devices, equal dc sources and eliminates the need for capacitors. It exhibits several attractive features such as less components, simple circuit and modular in structure. However as the number of output level increases, the circuit becomes bulky due to the increase in the number of power devices. It is also more efficient since the inverter combines low frequency and high frequency switches. Therefore, only a part of switches work in high frequency which leads to more reliable and simpler control of the inverter. This proposed topology utilizes Phase disposition SPWM scheme to drive the inverter. The proposed circuit generates a high-quality output voltage waveform and low harmonic components of output voltage.

2. Proposed H-Bridge Multilevel Inverter Topology

Photovoltaic arrays are connected to the multilevel inverter through a dc-dc boost converter. The dc-dc boost converter is used to step-up the output voltage of photovoltaic array. This proposed topology combines low frequency and high frequency parts. A part which is responsible for generating voltage levels in positive polarity is named as high frequency part. The required levels are generated by using high frequency switches. A part which is responsible for generating the polarity of output voltage is named as low frequency part as shown in Fig.1. Low frequency switches are used to generate the polarity.

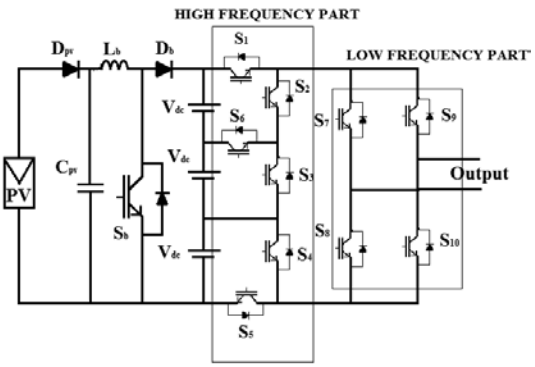


Fig.1 Proposed Seven Level Inverter Topology

The positive levels are generated by high frequency part, and then the output is fed to the low frequency H- bridge inverter part to generate the polarity for the output. Thus the multilevel output voltage is generated with the reduced number of switches by using the proposed topology. The proposed topology for seven level inverter is shown in Fig.1. It requires ten IGBT switches, ten diodes and three equal dc sources.

Low frequency part transfers the generated levels with the same direction or opposite direction according to the required output polarity. It has modular structure and it can be extended to higher levels by adding the middle part (V_{dc}, S_3, S_6) of the high frequency part. This topology eliminates fewer components compared with the conventional multilevel inverters. One of the advantage of the proposed topology is that it requires less high frequency components. High frequency components are expensive than the low frequency components. As per the MIL-HDBK-217F standard, number of components in the system is inversely proportional to the reliability of the system. As the number of high frequency components increased, the reliability of the inverter is decreased. In the proposed multi-level inverter, only half of the switches in the H-bridge are required to be switched on rapidly. Thus the reliability of the multilevel inverter is improved and expenses associated with the system are reduced. Control circuit complexity is reduced since the proposed topology generates only the positive levels.

For the Modified H-Bridge Multilevel inverter topology with h number of equal dc sources, the following equations can be written:

$$N_L = 2h+1 \quad (1)$$

$$V_{omax}=hV_{dc} \quad (2)$$

Where, N_L, V_{omax} denotes the number of output voltage levels and maximum output voltage, respectively.

The proposed inverter has less number of switches when compared with the other topologies presented in the literatures[24]. Hence, it is more suitable inverter for industrial applications.

3. Hybrid Modulation and Switching Sequence

A novel PWM technique is introduced to generate the switching signals. It requires half of the conventional carriers for SPWM controller. SPWM for seven level conventional inverter requires six carriers. But for the proposed topology only three carriers are sufficient. Since the multilevel inverter generates only positive polarity, the negative levels are generated by the low frequency part. Three carrier signals are compared with a reference signal. The carrier signals have the same frequency and amplitude and are in phase.

In this paper, Phase Disposition (PD) SPWM is utilized for its simplicity. Carriers in this method do not have any coincidence, and they have definite offset from each other. The reference signal and three carriers are shown in Fig.2.

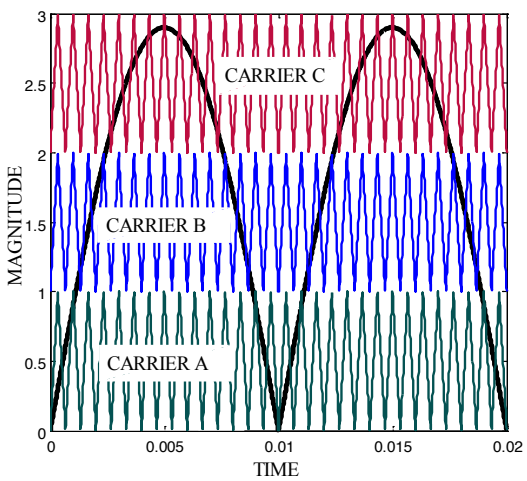
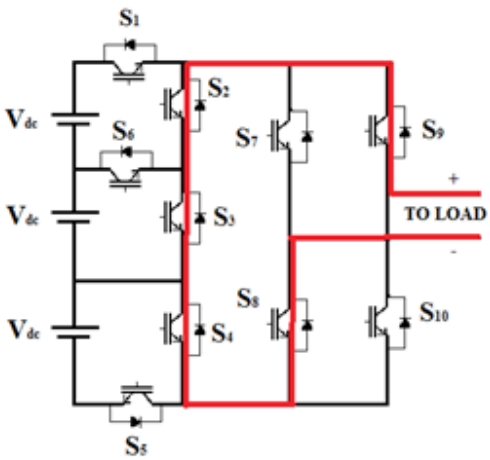
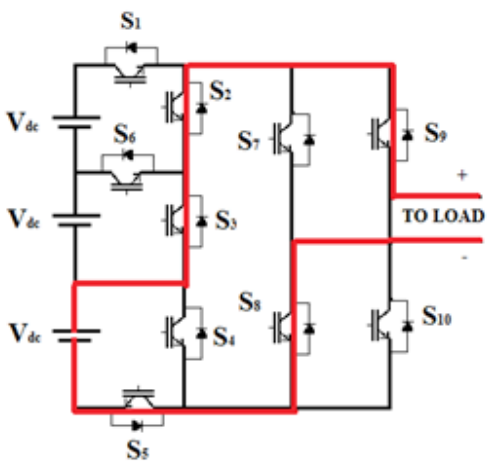


Fig.2 Carrier and Reference Waveform for Phase Disposition (PD) PWM

According to Fig.2, if the reference signal is exceeds the lowest carrier (Carrier A), middle carrier (Carrier B) is compared with reference signal until it exceeds the peak amplitude of the middle carrier signal. Then reference signal is compared with the highest carrier (Carrier C) until it reaches zero. In this proposed topology, it is not necessary to generate negative pulses for negative cycle. This task is done by the H-bridge inverter and the required level is generated by the high frequency part. Then this level is translated to positive or negative with the help of low frequency H-bridge inverter. It is possible to generate ten switching patterns to control the multilevel inverter. By considering the minimal switching transitions during each levels, the switch sequences (2-3-4), (2-3-5), (2-6-5) and (1-5) are chosen for positive levels. These switching sequences are shown in Fig.3.



(a) Level 0



(b) Level 1

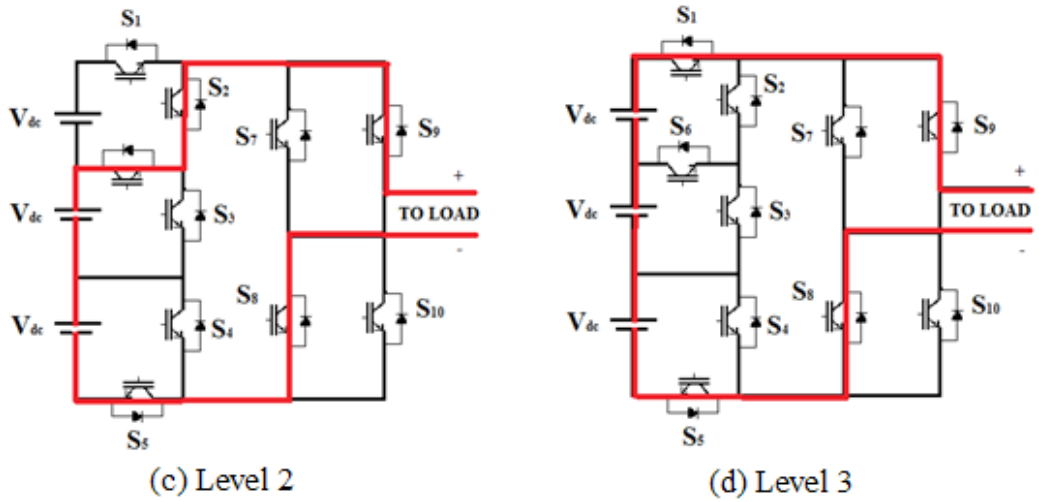


Fig.3 Switching Sequences for positive levels

The efficiency of the overall multilevel inverter is also decided by the number of switches that conducts current. The conventional seven level cascaded inverter requires twelve switches, and in each instance six switches conducts the current. In the proposed topology the number of switches that conduct current varies from four to five switches, out of which two switches are from the low frequency part. Therefore the number of switches that conducts current in the proposed topology is lesser compared with the conventional topology. Hence, it has better efficiency.

The gating signal for the low frequency part is simple and is synchronous with line frequency. Fundamental frequency switching scheme is used to generate the switching pulse for low frequency part.

Low frequency H-bridge inverter operates in forward and reverse modes to generate polarity. Switches S_8 and S_9, conducts in forward mode to generate positive direction. Switches S_7 and S_{10}, conducts in reverse mode to generate negative direction.

4. Simulation Study

The simulation of proposed three phase cascaded H- bridge multilevel inverter was done using MATLAB/Simulink. The IGBT switches are used as a switching device because of its lower switching loss and smaller snubber circuit requirement. In the simulation study all the switches are considered to be ideal. The frequency of output voltage is

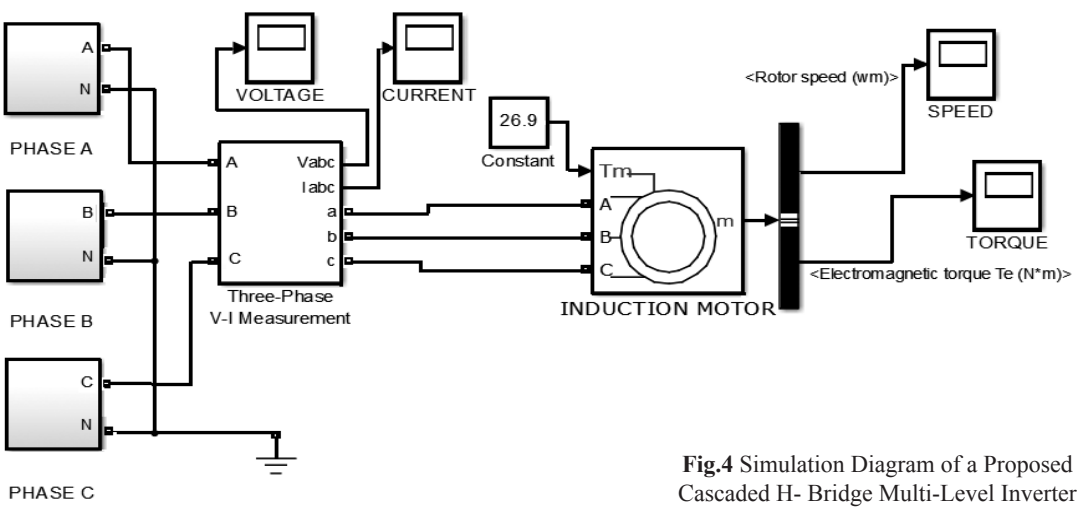


Fig.4 Simulation Diagram of a Proposed Cascaded H- Bridge Multi-Level Inverter

50 Hz. The dc voltage sources with a value of 133 V is used in the proposed topology. In practice, these dc voltage sources are available via distributed energy resources like photovoltaic panels, fuel cells, etc.,. The dc-dc boost converter is used to step-up the output voltage of photovoltaic array. Simulation diagram of a proposed cascaded H- bridge multi-level inverter is shown in Fig.4. The PWM switching patterns are produced by comparing three carrier signals against the unidirectional sinusoidal reference signal. This comparing process produces switching signals for switches S_1-S_6 . Pulse waveforms for the switches S_1-S_4 are shown in Fig.5.

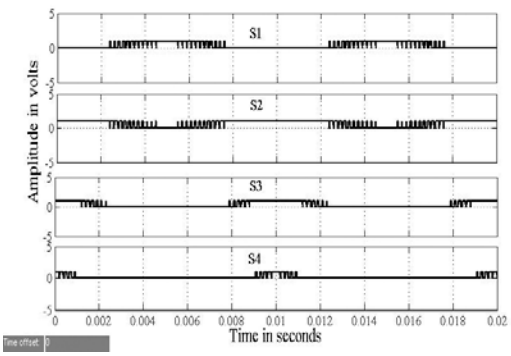
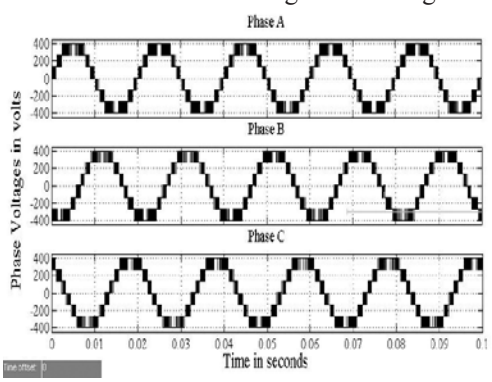
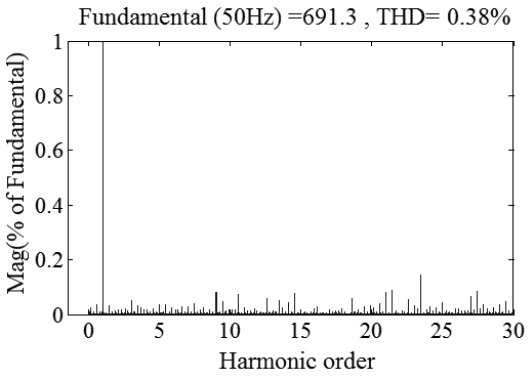


Fig.5 Pulse Waveform

The spectrum of the output line voltage and line current is taken to determine the Total Harmonic Distortion (THD) of the proposed inverter. The simulation result of output voltage, current and their corresponding FFT spectrum are presented in the Fig.6 and Fig.7. They clearly show that all of the desired voltage levels are generated.

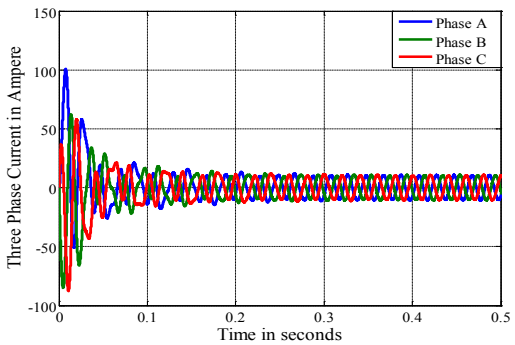


(a)

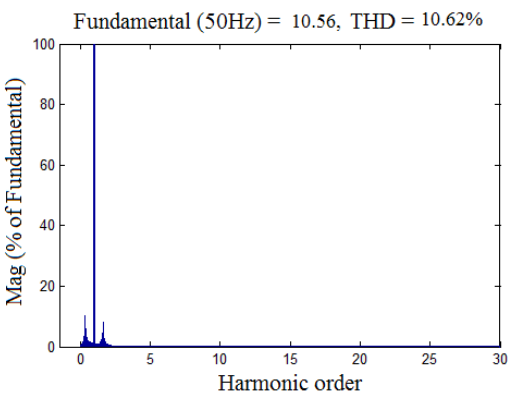


(b)

Fig.6 (a) Three phase voltage waveform of seven level inverter (b) FFT spectrum



(a)



(b)

Fig.7 (a) current waveform (b) FFT spectrum

From the normalized FFT analysis shown in Fig.6, it can be seen that the magnitude of lower order harmonics are very low and the magnitude of higher order harmonics are nearly equal to zero.

The Table.1 shows the comparison between a proposed H-Bridge multilevel inverter with the conventional multilevel inverters. The proposed H-Bridge multilevel inverter topology has the advantage of its reduced number of devices compared to conventional multilevel inverters and it can be extended to any number of levels. The comparison of proposed H-Bridge multilevel inverter with the conventional multilevel inverters for different levels is shown in Fig.8.

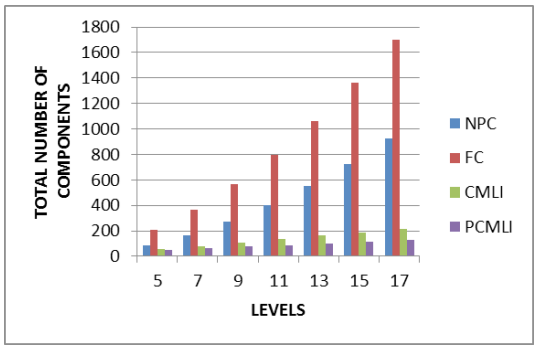


Fig.8 Comparison of proposed H- Bridge multilevel inverter with the conventional multilevel inverters for different levels

Table 1. Comparison of switching components for Different multilevel inverter topology

Inverter type	NPC Multilevel Inverter	Flying capacitor Multilevel Inverter	Cascaded H-bridge Multilevel Inverter	Proposed H-Bridge Multilevel Inverter
Main Switches	6(m-1)	6(m-1)	6(m-1)	3((m -1)+4)
Main diodes	6(m-1)	6(m-1)	6(m-1)	3((m -1)+4)
Clamping Diodes	3(m-1)(m-2)	0	0	0
DC bus Capacitors / isolated supplies	(m-1)	(m-1)	3(m-1)/2	3(m -1)/2
Flying capacitors	0	3/2 (m-1)(m-2)	0	0

5. Experimental Results

To experimentally validate the proposed multilevel inverter output voltage, hardware of single phase cascaded H-bridge multilevel inverter has been built using IGBT as the switching devices. Experimental setup of seven level Cascaded H bridge multilevel inverter is shown in Fig.9. PV arrays of 750W are used as a input to the multilevel inverter.

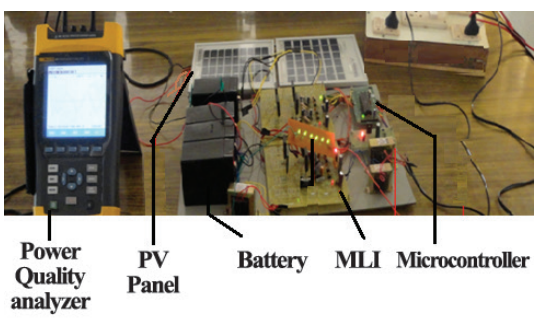


Fig.9 Experimental Setup

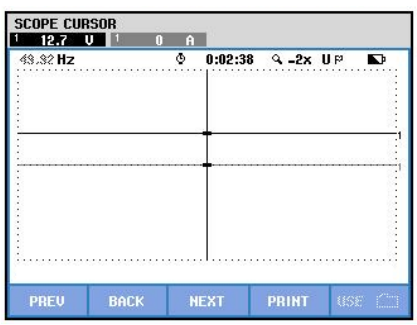


Fig.10 DC Output Voltage of Photovoltaic System

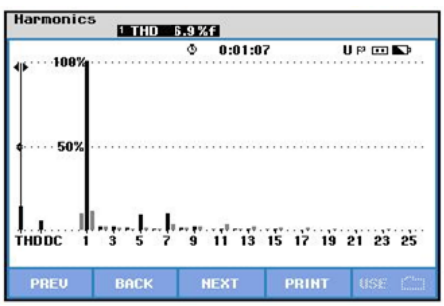


Fig.11 FFT analysis of Voltage Waveform

High-frequency switching ripples are removed by using LC filter and it is a combination of a 2-μF capacitor and a 10-mH inductor. This topology is used to generate seven levels of voltage for a resistive and inductive load. The switching frequency is 4kHz. ATmega16 Microcontroller is used to generate voltage pulses for IGBT gate. Control algorithm for the switching is written in the high level language and then it is embedded in the ATmega16 microcontroller. The voltage generated by the high-frequency part is fed to the low frequency part to define the polarity. Then the complete desired output waveform is created.

6. Conclusion

The proposed H- bridge multilevel inverter uses equal dc power sources for producing desired multilevel voltage is simulated and validated by hardware. The PD-SPWM control method is used to drive the high frequency part of the multilevel inverter. Fundamental frequency switching control algorithm is used to drive the low frequency part of the multilevel inverter. This proposed topology can be used in power applications such as FACTS, HVDC, PV systems integration with grids, UPS, etc. The switching operation is separated into high- and low-frequency parts. This will reduce the size and cost of the prototype.

The PD-SPWM for this topology only generates positive carriers for PWM control. The total harmonic distortion is reduced considerably. The FFT analysis of line voltage shows that the lower order harmonics have been reduced and also higher order harmonics are eliminated. From the FFT spectrum, if the number of level is increased then considerably THD value gets reduced. The results clearly show that the proposed topology can effectively work as a multilevel inverter with a reduced number of carriers for PWM. This proposed topology reduces the initial cost and complexity.

The proposed H- bridge multilevel inverter can also be used for industries where the variable speed drives (conveyors, rolling mills, printing machines) are required and considerable amount of energy can be saved as the proposed system has lower harmonics.

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