CMOS DESIGN OF A MULTI_INPUT ANALOG MULTIPLIER AND DIVIDER CIRCUIT

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Abstract: *This paper proposes a CMOS current-mode multi_input analog multiplier and divider circuit based on a new method. Exponential and logarithmic functions are employed to realize the circuit which is used in neural network and fuzzy integrated systems. The major advantages of this multiplier are ability of having multi_input signals, and low Total Harmonic Distortion (THD). The circuit is designed and simulated using MATLAB software and HSPICE simulator by level 49 parameters (BSIM3v3) in 0.35µm standard CMOS technology. The simulation results of analog multiplier demonstrate a linearity error of 0.9% and a THD of 0.42% in 1MHz. Moreover, the maximum power consumption of the circuit is found to be 0.89mW.*

Keywords: *Multi_input Multiplier, Divider Circuit, Low THD, High Linear.*

1. Introduction

The analog multiplier is a versatile cell with applications in the field of signal processing, signal processing circuits such as adaptive filters, modulators, automatic gain controllers, neural networks and all-analog compact control loops. Multipliers generate the linear product of two multiplicands resulting an output of $Out = K \times I_1 \times I_2$ where K is a coefficient with appropriate dimension.

In last decade, a large number of different architectures for the design of four quadrant analog CMOS multipliers have been proposed. Driven by the early work of *Gilbert* [1], a variety of multipliers have been designed for different optimization objectives [2]–[11].

Different techniques have been proposed for optimization of power consumption [2, 3], speed [4], accuracy [5, 6] and linearity [7, 8] in CMOS analog multiplier circuits. They use floating gate MOS [9], bulk-driven MOS [10], sub-threshold mode [11] or class-AB mode [5]. All of the reported works have ability of multiplication of only two signals, either voltage or current signals. In the field of signal processing sometimes, it is required to multiply or divide more than two signals simultaneously [12]-[14]. As a Conventional Procedure, to realize this requirement, it can be cascaded the multiplier or divider circuits. Unfortunately, this method increases error at the output, because multiplication naturally is an additive operation. Therefore the noise which is generated in the first stage of the multiplier will be amplified in the next stages [15]. In addition, nonlinearity and Total Harmonic Distortion (THD) which is directly related to the noise of the system will be undesirable.

In this paper, we present a new topology of the analog multiplier in a CMOS technology with emphasis on multi_input structure to overcome to this problem. However other features such as linearity and power consumption will be acceptable. We analyze various performance metrics of the multiplier and provide some design considerations. It is demonstrated in particular that this multiplier is much better than other structures in terms of THD and linearity, and because of having multi_input ability, is especially suitable for implementation of neural network and fuzzy integrated systems.

Proposed method is described in Section 2 followed by the presentation of approximation functions in section 3. In section 4, transistor-level design of the proposed method is discussed and the simulation results are presented to prove the efficiency of the approach. Finally, the paper is concluded in section 5.

2. Proposed Method

The proposed method uses exponential (exp) and logarithmic (Ln) functions presented in [16]. According to mathematical properties of these functions, one can write the following relationship:

$$e^{Ln(a)+Ln(b)} = a \times b \tag{1}$$

Similarly, we can use the subtraction property of Ln function to implement a divider:

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$$e^{Ln(a)-Ln(b)} = \frac{a}{b} \quad (2)$$

The main advantage of this method is the ability of multiplying more than two signals by summing the logarithmic form of signals. Therefore we have to implement circuits to generate exponential and logarithmic functions which are an area of challenge in circuit design, because these are not available in CMOS technology, since CMOS transistors follow a square-law characteristic in strong inversion. To implement this method in minimum complexity, we propose new and simple approximation of exponential and natural logarithmic functions using MATLAB software.

3. Proposed Approximations for Exponential and Logarithmic Functions

In this section a new and accurate approximations for implementing exponential and logarithmic functions is defined with an interval having a wider range in comparison to the reported works [17, 18]. Unlike the previous works, Taylor series expansion is not used. The proposed approximation is simple and easy to implement, because of using only "x", "x^2", and "$\sqrt{x}$" terms which are easily implemented with CMOS circuits. The coefficients of these terms are calculated in MATLAB software by using *linear least squares* method and *curve fitting toolbox* to have an accurate approximation.

The concluded approximation of the natural logarithmic function is:

$$|ln\ x| \approx -0.84\ x^2 + 4.8\ x - 8.4\sqrt{x} + 4.5 \quad (3)$$

Similarly Comparing with other works, the dynamic range of this function is wide, as can be seen in Figure. 1. This figure shows the simulation result of the logarithmic function and its comparison with the ideal curve by MATLAB software.

For values less than 1, the natural logarithm produces negative values, so the absolute value of the equation (3) obtained. Therefore applying this to the next exponential block, we can introduce the negative sign to its argument ($exp(-x)$).

The approximation of the exponential function without the "$\sqrt{x}$" term is:

$$exp(-x) \approx 0.19\ x^2 - 0.82x + 1 \approx\ (0.43x)^2 - 0.82x + 1 \quad (4)$$

Figure 2 shows the simulation result of the approximation of the exponential function and its comparison with the ideal curve by MATLAB software.

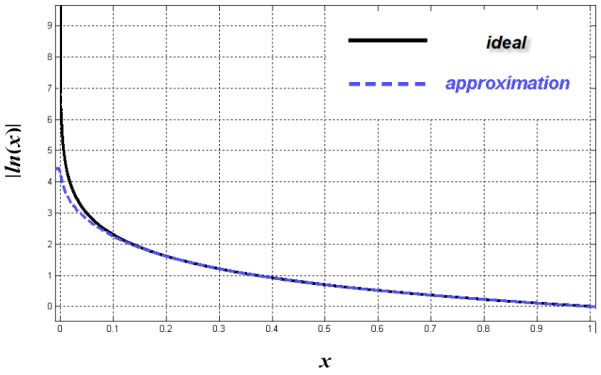

Figure 1. Approximation of natural logarithmic function using MATLAB

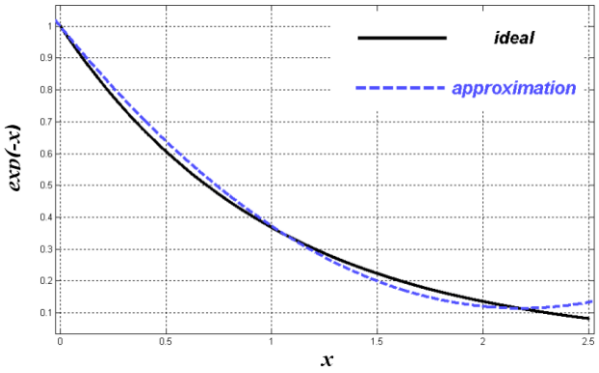

Figure 2. Approximation of the exponential function using MATLAB software

4. Circuit Design of Proposed Approximation

For hardware implementation of these functions in CMOS technology, we need two main circuits that are: 1-squarer (sq) 2-square-rooter (sq-rt).

Note that in circuit implementation of proposed structure, current of 10μA normalized to one, for example 5μA ≡ 0.5, therefore [0, 10μA] ≡ [0, 1].

4.1. Squarer Circuit

Figure 3 shows the current-mode squarer circuit based on the *"dual translinear loop"*[4]. Consider a loop of MOS transistor *M1* to *M4* (trans-linear loop) gives:

$$V_{GS1} + V_{GS2} = V_{GS3} + V_{GS4} \quad (5)$$

Assuming that MOS transistors *M1* to *M4* are biased in the saturation region and all transistors are well matched and have long channel length, rewriting equation (5):

$$\sqrt{I_1} + \sqrt{I_2} = \sqrt{I_3} + \sqrt{I_4} \quad (6)$$

Writing KCL at nodes *A* and *B*:

$$I_3 = I_{out} + I_{in} \quad (7)$$

$$I_4 = I_{out} - I_{in} \quad (8)$$

Considering $I_1=I_2=I_B$ and substituting equations (7) and (8) in equation (6) and squaring both sides twice:

$$16{I_B}^2 - 16I_B I_{out} + 4{I_{out}}^2 = 4{I_{out}}^2 - 4{I_{in}}^2 \quad (9)$$

The output current I_{out} can be written as:

$$I_{out} = \frac{{I_{in}}^2}{4I_B} + I_B \quad (10)$$

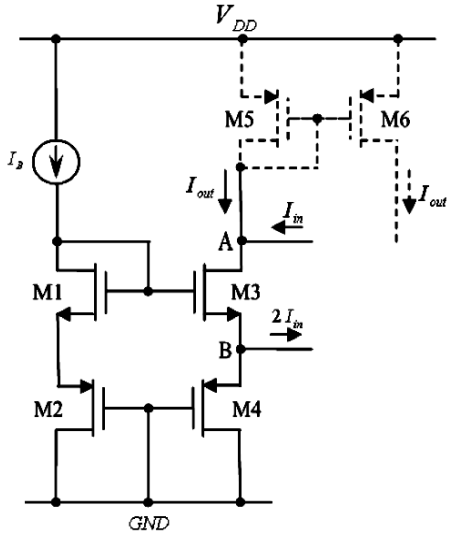

Figure 3. Current-mode squarer circuit

4.2. Squar Rooter Circuit

Figure 4 shows the current-mode square rooter circuit [7]. This circuit based on the *"up-down topology trans-linear loop"*. Applying KVL for trans-linear loop composed of NMOS transistors *M*1–*M*4 results in:

$$V_{GS1} + V_{GS3} = V_{GS2} + V_{GS4} \quad (11)$$

Knowing that these devices are perfectly matched having long channel lengths, and the drain current of a MOS transistor in saturation region has the following relation to gate-source voltage:

$$I_{DS} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{GS} - V_t)^2 \quad (12)$$

Then equation (11) can be rewritten as:

$$\sqrt{I_1} + \sqrt{I_3} = \sqrt{I_2} + \sqrt{I_4} \quad (13)$$

Applying KCL in the output node gives:

$$I_2 + I_4 = I_{out} + \frac{I_X + I_Y}{2} \quad (14)$$

Finally, the input and output currents of NMOS current mirror are equal:

$$I_X + I_Y + I_4 = I_X + I_Y + I_2 \quad (15)$$

Which results in $I_2 = I_4$. Squaring equation (13) and using equation (15) and the result of equation (14) give the desired relationship between the inputs and the output:

$$I_{out} = \sqrt{I_X I_Y} \quad (16)$$

Note that, because the normalized current is considered as 10uA, the output of the sq-rt circuit is in the form of $I_{out} = \sqrt{10\mu A \times I_x}$ and the output of the sq circuit is in the form of $I_{out}={I_{in}}^2/10\mu A$ in the main circuits, that is shown in Figures 5 and 9.

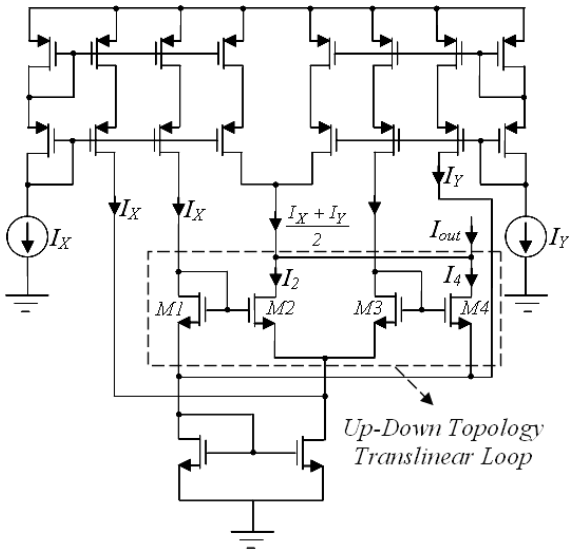

Figure 4. Current-mode square rooter circuit

4.1. Logarithmic Function Generator Circuit

The block diagram of the logarithmic function generator is shown in Figure 5. First, I_{in} is injected to a NMOS cascode current mirror and two copies of it flow in sq and sq-rt blocks. The upper branch provides $8.4\sqrt{x}$ mathematically, and the middle branch gives $0.84x^2$, and the bottom branch sinks a current of $4.8x$. Summation of these currents flow in node A and is subtracted from constant current of 45μA. I_{out} is natural logarithm function of I_{in}. For example, mathematically we have: $|Ln\ 0.4| \approx 0.92$ and in circuit implementation: $|Ln\ 4\mu A| \approx 9.5\mu A \equiv 0.95$ (because 10μA is normalized to 1)

Simulation result of this circuit using HSPICE is shown in Figure 7. Comparing this with the results in Figure 1 shows the efficiency of the proposed configuration.

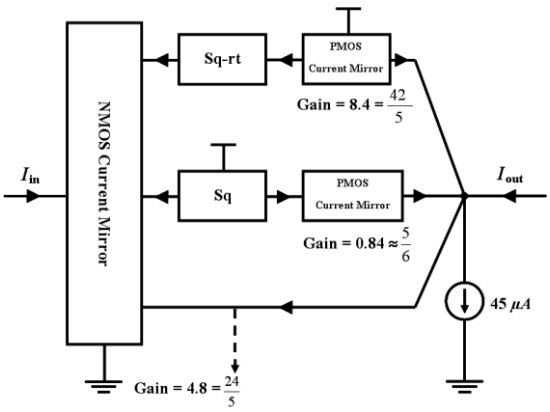

Figure 5. The block diagram of the natural logarithmic function generator

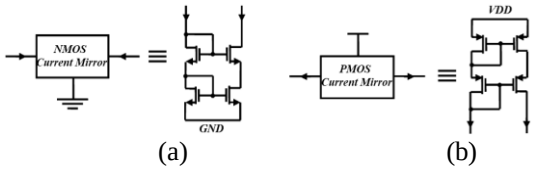

Figure 6. Fig. 6. (a) NMOS cascode current mirror (b) PMOS cascode current mirror

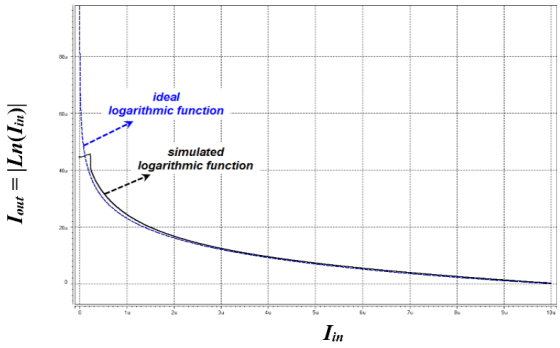

Figure 7. Simulation result of the natural logarithmic circuit using HSPICE

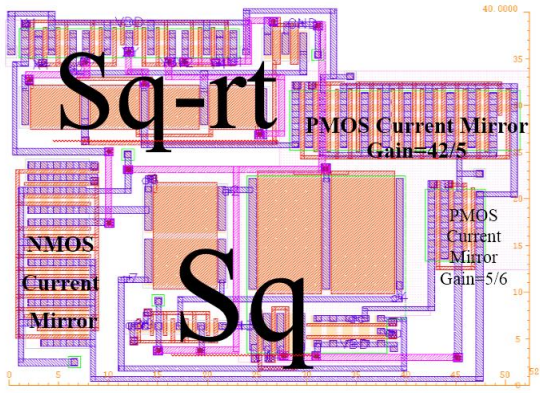

Figure 8. Layout of the natural logarithmic function generator circuit

Figure 8 shows layout of the natural logarithmic function generator circuit, which only two kinds of metal are used: ”Metal1” and “Metal2”.

4.1. Exponential Function Generator Circuit

Figure 9 shows block diagram of exponential function generator. In this block diagram, first I_{in} is injected to a PMOS cascode current mirror and two differently scaled of it flow in two branches.

The upper branch provides $0.19x^2$ or $(0.43x)^2$ and the bottom branch gives $0.82x$. Summation of these currents flow in node B and is subtracted from constant current of 10μA. I_{out} is exponential function of I_{in}. For example mathematically we have: $e^{-1}\approx0.37$, and in circuit implementation: $e^{-1}\approx3.61\mu A \equiv 0.361$ (because $10\mu A$ is normalized to one)

HSPICE simulation result of the circuit in Figure 9 that generate exponential function is shown in Figure 11.

In order to implement logarithmic and exponential functions, we need some constant coefficients to realize their approximations. This can be easily done using current mirrors with selectable gains, which is shown in Figure 10.

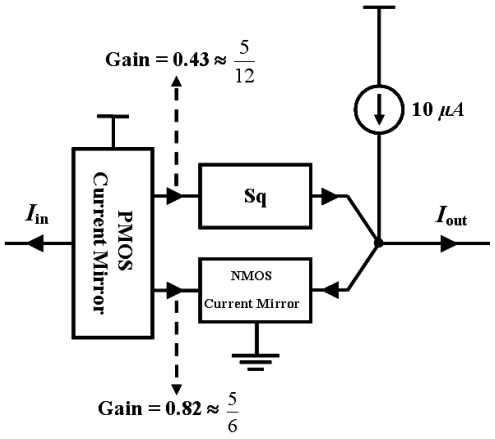

Figure 9. The block diagram of the exponential function generator (*Exp cell*)

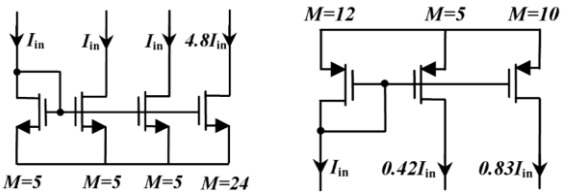

Figure 10. Realization of constant coefficients for using in logarithm and exponential functions block diagram

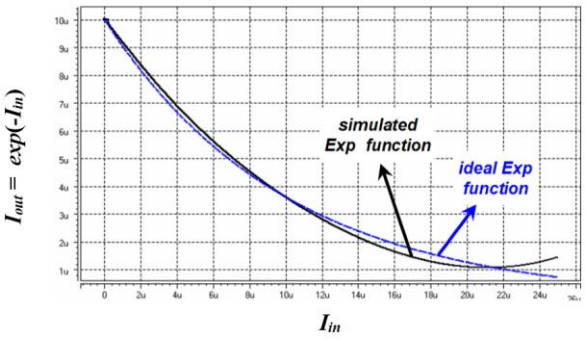

Figure 11. HSPICE Simulation result of the exponential circuit

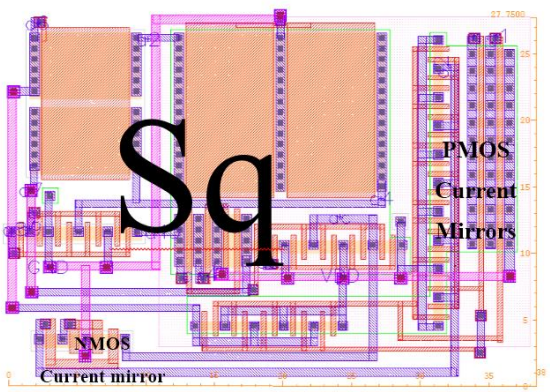

Figure 12. Layout of the exponential function generator circuit

5. Multi_Input Multiplier and Divider Circuit

The structure which multiplies input signals is shown in Figure 13. This is designed to yield equation (1) using designed circuits in section IV. This figure shows the block diagram of the circuit which can multiply five input currents. In fact, considering the logarithmic and exponential properties in equation (17), five *Ln cells* providing output currents connect to one node, so their current add to each other; then output current of this node have been injected to *Exp cell*:

$$e^{LnI_a+LnI_b+LnI_c+LnI_d+LnI_e} = I_a \times I_b \times I_c \times I_d \times I_e \qquad (17)$$

Figure 15 shows the other simulation results including error measurement. Two sinusoidal inputs (I_a and I_b) are applied to the multiplier at frequency of 1*MHz*. Output signal is sinusoidal shape which is exactly the multiplication of input signals. DC transfer simulation results show the linearity error of 0.89*%*. Similarly, block diagram of Figure 18 is implemented to realize equation (2), where a divider circuit with five inputs is demonstrated:

$$e^{(LnI_{num})-(LnI_a+LnI_b+LnI_c+LnI_d+LnI_e)} = \frac{I_{num}}{I_a \times I_b \times I_c \times I_d \times I_e} \qquad (18)$$

Generally current mode realization of the circuits leads to simple and intuitive configurations. In all of the circuits I_B is constant current of 10μA which is normalized to one.

The linearity of the multiplier/divider is estimated in terms of either percentage of distortion in DC transfer characteristics or THD of multiplier/divider. A THD of less than 2% in the region of operation is sufficient for many analog VLSI signal and information processing applications [19]. Simulation results of THD versus input current signal at 10 *KHz*, 100 *KHz* and 1 *MHz* are shown in Figure 16. Also Figure 17 demonstrates the application of the proposed multiplier as an amplitude modulator.

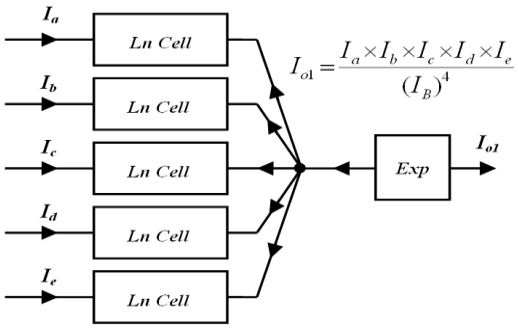

Figure 13. The block diagram which can multiply 5 inputs

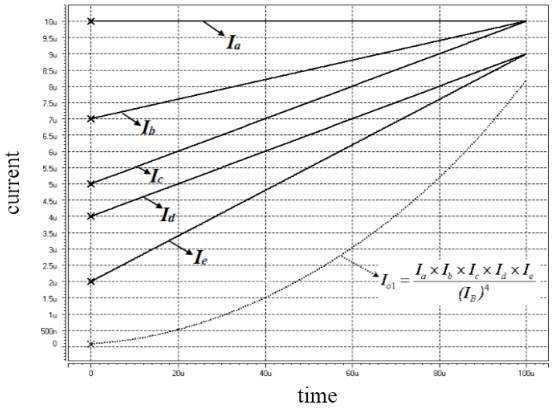

Figure 14. Simulation result of multiplying five input currents

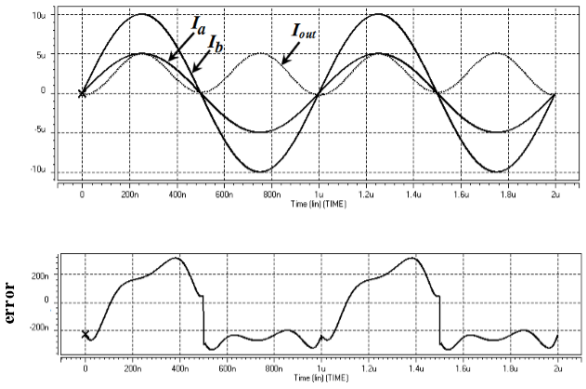

Figure 15. Simulation of the circuit in 1*MHz*

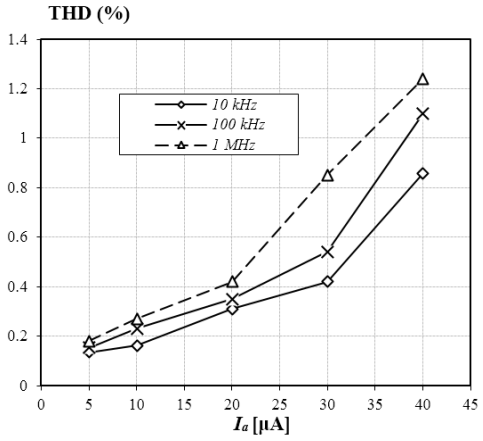

Figure 16. Relation between THD and input current

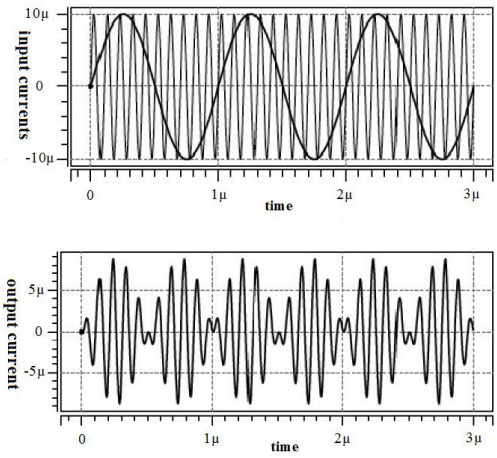

Figure 17. Amplitude modulation of sinusoidal signals

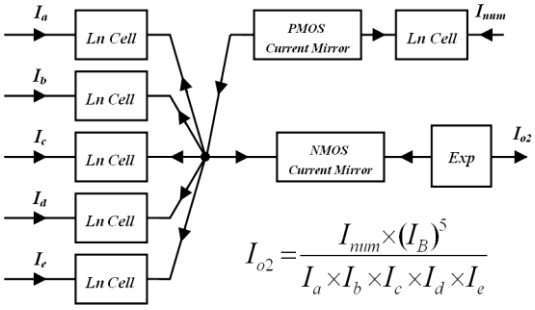

Figure 18. The block diagram which can divide a constant current over five input currents

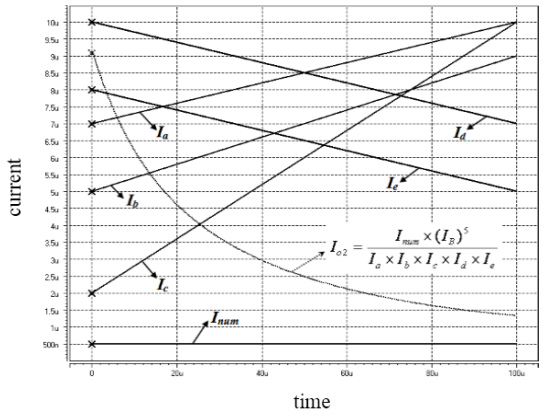

Figure 19. Simulation result of dividing a current over five input currents

Table 1. Comparison between the proposed multiplier and 4 previously reported multipliers

	[3]	[5]	[6]	[7]	This work
Power cons.(*mW*)	0.055	0.46	0.93	0.7	0.89
Max No. of Inputs	2	2	2	2	5
Bias Current (μA)	0.25	10	10	10	10
Power supply(*V*)	2	±1.5	5	5	3.3
THD(%)(1*MHz*)	1(1*K*)	3.7	0.65	1(10*K*)	0.42
Nonlinearity (%)	5	1.20	1.22	—	0.9
-3*dB* BW(*MHz*)	0.2	19	22.4	12.3	18.8
Technology(μm)	0.35	0.5	2	2.4	0.35

5. Conclusions

Multi_input four-quadrant analog multiplier and divider circuit based on a new method was proposed. Approximations of exponential and logarithmic functions which obtained by MATLAB software were realized in CMOS process. The circuits were designed and simulated using HSPICE simulator by level 49 parameters in 0.35μm standard CMOS technology. The simulation results demonstrated a linearity error of 0.9%, a THD of 0.42% in 1MHz, and a maximum power consumption of 0.89mW. MATLAB simulation results verified the validity of results which were simulated by HSPICE. Also Table 1 shows a performance comparison of the proposed circuit with former realizations.

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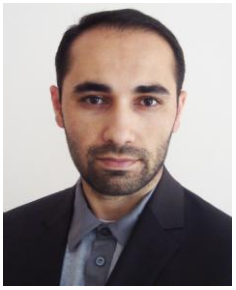

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