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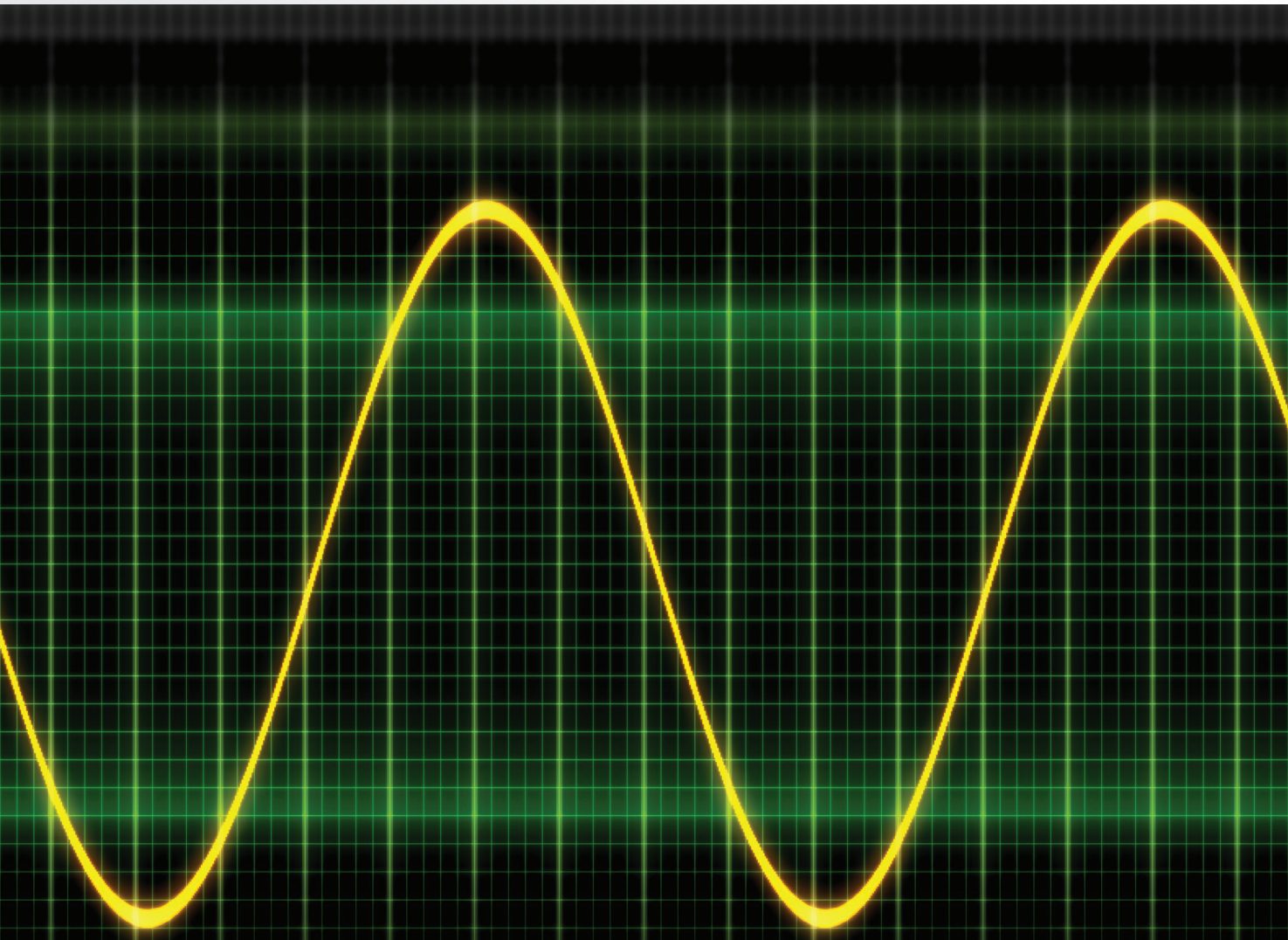

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Electrica aims to contribute to the literature by publishing manuscripts at the highest scientific level on all fields of electrical and electronics engineering. The journal publishes original research and review articles that are prepared in accordance with ethical guidelines.

The scope of the journal includes but not limited to; electronics, microwave, transmission, control sytems, electrical machines, energy transmission and high voltage.

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Letter to the Editor	500	No abstract	5	No tables	No media

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Contents

RESEARCH ARTICLES

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RESEARCH ARTICLE

Electrica 2019; 19(2): 91-100

Noise Robust Voice Activity Detection Based on Multi-Layer Feed-Forward Neural Network

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ABSTRACT

This paper proposes a voice activity detection (VAD) method based on time and spectral domain features using multi-layer feed-forward neural network (MLF-NN) for various noisy conditions. In the proposed method, time features that were short-time energy and zero-crossing rate and spectral features that were entropy, centroid, roll-off, and flux of speech signals were extracted. Clean speech signals were used in training MLF-NN and the network was tested for noisy speech at various noisy conditions. The proposed VAD method was evaluated for six kinds of noises which are white, car, babble, airport, street, and train at four different signal-to-noise ratio (SNR) levels. The proposed method was tested on core TIMIT database and its performance was compared with SOHN, G.729B and Long-Term Spectral Flatness (LSFM) VAD methods in point of correct speech rate, false alarm rate, and overall accuracy rate. Extensive simulation results show that the proposed method gives the most successful average correct speech rate, false alarm rate, and overall accuracy rate in most low and high SNR level conditions for different noise environments.

Keywords: Voice activity detection, time and spectral features, multi-layer feed-forward neural network

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Introduction

Voice activity detection (VAD) is a signal processing technique that allows a speech signal to be seperated into voice and other parts. Non-speech regions include silence and noise signal parameters and VAD is used to effectively distinguish between speech and non-speech regions. The principal VAD applications are speech coding [1, 2], speaker and speech identification [3], noise reduction in digital hearing aid devices, mobile communications [4], and noisy speech enhancement [5, 6]. VAD methods used in many applications are based on thresholding energy, pitch detection, zero-crossing rate, linear predictive coefficients, and cepstral coefficients because of their simple structure [7-9]. However, in VAD applications using these criteria, it is difficult to detect speech regions in low signal-to-noise ratio (SNR) or non-stationary background noises. Up to recently, various features have suggested and this features including energy-entropy feature [10], cepstral feature [11, 12], and Teager energy feature [13]. In most of these methods, the noise signal is considered to be stationary over certain periods of time. For this reason, these methods are highly sensitive to SNR variations in the processed speech signal.

Voice activity detection methods are divided into three basic category based on time, frequency, and time-frequency domain. Time domain methods include energy, zero-crossing rate, and low frequency band power. The frequency domain methods include various spectral energy features which are energy-entropy, cepstral, and Teager energy features. Also, time-frequency methods include Wavelet transform and Empirical Mode Decomposition [14]. For noisy conditions, time domain, frequency domain, and time-frequency domain methods such as discrete wavelet transform, wavelet packet transform, and perceptual wavelet packet transform are insufficient in detecting speech/voice regions. In most of these methods, threshold values levels cannot be calculated accurately and precisely at all noise types and all SNR levels. Therefore, in recent years, empirical mode decomposition method, which separates speech signals

from high frequency to low frequencies into intrinsic modes, has been used in the determination of speech/voice regions [15, 16]. These traditional methods are insufficient in detecting speech/voice regions in noisy conditions.

Related Works

In recent years, various methods have been developed to detect voice or speech activity regions under different noisy conditions [17, 18]. The most known VAD approach in these methods, a statistical model for determining the voice and unvoiced regions has recommended by Sohn et. al [19]. The robust VAD algorithm, which use the likelihood ratio test based on statistical models, shows a better performance in the determination of the speech regions than the traditional methods. In this method, a speech decision rule was obtained from the generalized likelihood ratio test, assuming that noise statistics were a priority. In order to estimate time-varying noise statistics, a new noise-pattern adaptation algorithm was developed using soft decision information in the areas where the speech signal was present. This algorithm, which was designed to determine the voice regions of clean speech signals, cannot perform the same performance in speech and non-speech regions in noisy speech signals. The G729B, a modern standard VAD method, was developed for short-time frames and this method used line spectral frequencies, low band energy, zero-crossing rate, and full band energy parameters [20]. In this algorithm, a structure which was used together with the intuitively defined regions and borders was applied and decided for every 10 ms.

Most standard VAD algorithms are derived from short-term analysis frameworks and the VAD decision is made over these short-term frames. In contrast to the short-term framework for VAD, long-term spectral divergence (LTSD) was proposed as a long-term VAD analysis and a long-term spectral envelope was compared with the average noise pattern to establish a speech and non-speech decision rule [21]. In another long-term approach, a new and robust VAD algorithm was recommended using the long-term spectral flatness (LSFM) measure [22]. This new LSFM-based VAD increased the robustness of speech detection in various noisy environments using low noise spectrum estimation and adaptive threshold values. The proposed algorithm was evaluated under 12 types of noises and five types of SNR in core TIMIT test corpus. Comparisons based on the standard three VAD algorithms such as AMR1, AMR2 and G729B show that the LSFM-based VAD approach achieves the best average accuracy rate (88.95%).

Recently, a novel voice activity detection (VAD) scheme employing differential entropy at each frequency bin of power spectral estimates of past and present overlapping speech frames were proposed [23]. In this method, frequency domain long-term differential entropy (FLDE) was used to determine the speech and non-speech regions. They evaluated the performance of the proposed FLDE scheme, considering 12 types of noises and 5 different SNRs which were artificially added to speech samples from the SWITCHBOARD corpus. Graf et al. [24] mentioned about harmonicity, power, SNR, formant structure, modulation, and stationarity features of VAD algorithms. Pasad et al. [25] showed that speech and non-speech regions were difficult to detect when background sounds such as breath, mic pops, etc. were present in the signal.

In most of these methods, threshold values cannot be calculated accurately and precisely at all noise types and all SNR levels. Therefore, in recent years, the classification of speech and non-speech regions is performed through artificial neural networks. Farsinejad et al. [26]. proposed a VAD algorithm using short-time power, zero-order maximum likelihood parameter, and pitch-period difference and Probability Neural Network (PNN). In another VAD algorithm based on Support Vector Machine (SVM) [13], the determination of voice and unvoiced regions, the noisy speech signal was decomposed by Wavelet Packet Transform (WPT) and Teager energy of each wavelet packet coefficients was calculated. The energy values of noisy speech signal used as input for SVM.

In [27], fuzzy entropy and a SVM-based VAD approach have been proposed to detect voice regions in noisy conditions. In this method, the Fuzzy entropy (FuzzyEn) features obtained from noisy speech signals were used to train and test the SVM model in determining speech and non-speech regions. In various noisy conditions, speech and non-speech regions were determined with a accuracy of 93.29%. However, the performance of this method is insufficient for low SNRs. In another VAD study, Deep Neural Network (DNN) was used to determine the speech regions [18]. In this VAD approach, six different features extracted from speech signals were used to train and test the network. In VAD performance evaluation, the area under the curve (AUC) and F-measure were used and absolute increments were calculated as 10.41% and 8.56%, respectively. Similarly, a VAD approach was proposed for the speech recognition system, which allows the classification of speech and non-speech regions and DNN model was used for classification [28]. In this DNN-based VAD approach, a 22% improvement in equal error rate (EER) was achieved compared to traditional VAD approaches. Wang et al. [29] suggested a DNN-based VAD approach on the CENSREC-1-C database. They used mel-frequency cepstral coefficients, instantaneous frequency derivative, power normalised cepstral coefficient, and magnitude information and found an equal error rate of 19.44%.

A VAD method that uses line spectral frequency based statistical features with extreme learning based classification has been proposed [30]. In this study, data having a duration of more than 350 hours were used and an overall accuracy rate of 99.43% was obtained. Bouguelia et al. [31] proposed a new active learning method (ALM) that questions the label of samples based on how they affect the outcome of the classification mode. An unsupervised classification method was proposed in order to determine the presence and absence of speech regions in speech signals and this method was successful at the boundary points where the detection was quite important [32]. In another VAD approach, a VAD system has been

proposed in a multi-speaker environment. In this approach, Mahalanobis classifier and attributes of speech energy signals were taken into consideration [33]. Shi et al. [34] used a neural network-based approach with maximum short-term automatic correlation and spectrum variance for end-point detection of speech signals. In this VAD approach, 200 clean speech signals were corrupted with three different noise types such as white, babble, and car for SNR values ranging from -5 to 10 dB. The average correct rates of 93.59, 85.11 and 90.29% were obtained for the white, babble, and car noise types, respectively .

Any VAD algorithm basically consists of two parts which are 'feature extraction' and 'speech / non-speech decision mechanism'. The parameters are extracted in the first section from the speech signals that can represent the distinctive features of the speech relative to the noise. In the second part, these voice parameters are used to decide whether the region is to be speech / non-speech based on a set of decision rules.

In this study, voice activity detection algorithm was improved by using time and spectral features based on MLP-NN. The time and frequency domain features of segmented speech signal distorted by different noise type at 0, 5, 10 and 15 dB SNR levels used as input of MLP-NN. The proposed method was tested on core TIMIT database and its performance was compared with SOHN, G.729B, and LSFM VAD methods in point of correct speech rate, false alarm rate, and overall accuracy rate.

Methodology

Basic Structure of Proposed VAD

The steps of the proposed method is given in Figure 1. Firstly, noise was added to the clean speech signals and the signals were separated into frames. Then, time and spectral features were extracted for each frame. These features of noisy speech signals were applied to MLF-NN and the network was tested with speech data. Finally, the performance of the system was evaluated.

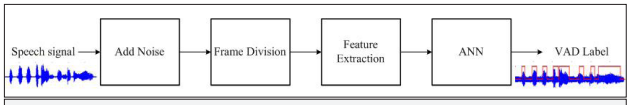

Figure 1. A schematic for the proposed method
30x3 mm (600x600 DPI)

Features for VAD

Speech signals are inherently non-stationary signals that change over time. Therefore, speech signals were processed by dividing into frames. In the proposed method, six different features per frame was used. These features were the short-time energy, zero-crossing rate, spectral entropy, roll off, flux, and centroid. These features were applied to the input of MLF-NN for training and the network was determined if the speech was either speech or non-speech.

Short-Time Energy

Short-time energy (STE) is commonly used to determine the voice and unvoiced regions. Voice regions have high energy, whereas non-speech regions have low energy values. However, this feature loses its efficiency especially in lower SNRs. In general, the STE is defined as follows [35]:

$$E_m = \sum_{k=-\infty}^{\infty} [x(k)w(m-k)]^2 \quad (1)$$

where $x(k)$ and $w(m–k)$ denote a segment of the sequence and time-shifted window sequence, respectively.

Zero-Crossing Rate

Zero-crossing rate (ZCR) is a measure of how many times the speech signal has passed through zero. In speech and non-speech regions, zero-crossing rate has lower and higher values, respectively. The ZCR is defined as [35]:

$$Z_m = \frac{1}{2}\sum_{n=0}^{N-1} \left|\mathrm{sgn}[x(n)] - \mathrm{sgn}[x(n-1)]\right| w(n-m)$$
$$\mathrm{sgn}[x(n)] = \begin{cases} 1 & x(n) \geq 0 \\ -1 & x(n) < 0 \end{cases} \quad (2)$$

where $x(n)$ is the time domain signal for frame m.

Spectral Entropy

The spectral entropy is a measure of uncertainty for intrinsic characteristics of speech spectrums. Many existed experiments have proved that spectral entropy is superior to the time domain features for speech activity detection [36]. Spectral entropy has low and high values for speech and non-speech regions, respectively. Spectral entropy is calculated for each frame and each frame separated into four sub-frames. Fourier Transform of speech frame for each sub-band is defined as [37]:

$$X(k) = \sum_{n=0}^{N-1} x(n)\exp(-j\frac{2\pi nk}{N}), \quad k = 0,1,2,...,N-1 \quad (3)$$

where $X(k)$ represents the spectral magnitude of the k th frequency bin and N is the total number of frequency bins. The spectral energy of each frame $E(k)$ is expressed as:

$$E(k) = \left|X(k)\right|^2, \quad k = 0,1,2,...,N/2 \quad (4)$$

and the probability measure in the spectral domain can be written as:

$$p(i) = \frac{E(i)}{\sum_{k=1}^{N/2} E(k)}, \quad i = 0,1,2,...,N/2 \tag{5}$$

Then, the spectral entropy for each frame is calculated as:

$$H = -\sum_{i=1}^{N/2} p(i)\log[p(i)] \tag{6}$$

Spectral Centroid

Centroid is a measure of the spectral shape. The spectral centroid value in the high frequency range is greater than in the low frequency range. Therefore, the spectral centroid measure are used to identify voice and unvoiced regions. While the spectral centriod values are low in the speech regions, the spectral centroid values of the non-speech regions are high. The spectral centroid value of a signal spectrum can be expressed as follows [38]:

$$C_r = \frac{\sum_{k=1}^{N/2} f[k]|X_r[k]|}{\sum_{k=1}^{N/2}|X_r[k]|}, \quad k = 0,1,...,N-1 \tag{7}$$

where $X_r(k)$ is the magnitude of the Fourier transform at frame r and $f(k)$ is the frequency at bin k.

Spectral Roll-off

The spectral roll-off could be defined as the frequency at which 85% of the spectrum magnitude is concentrated and this value is also a measure of the spectral shape. It has higher values in the higher frequency ranges than in the low frequency ranges. Because of this property, this criterion can be used in voice activity detection. The spectral roll-off measure can be formulated as follows [38]:

$$\arg\min_{f_c \in \{0,...,N-1\}} \sum_{k=0}^{f_c} |X_r[k]| \geq 0.85 \sum_{k=0}^{N-1} |X_r[k]| \tag{8}$$

where f_c is the roll-off frequency and $X_r(k)$ is the magnitude of the *k-th* frequency component at frame *r*.

Spectral Flux

The flux could be defined as the average variation of spectrum between the two adjacent frames. The spectral flux of the noise signal has higher values than the periodic signals. Therefore, spectral flux can be used to identify the voice and unvoiced regions. Spectral flux can be expressed as follows [38]:

$$F_r = \sum_{k=0}^{N/2} (|X_r[k]| - |X_{r-1}[k]|)^2 \tag{9}$$

where $X_r(k)$ and $X_{r-1}(k)$ are the normalized magnitude of the Fourier transform at frames r and $r-1$.

Artificial Neural Network for VAD

Neural Networks have also been shown to be applicable in the area of speech detection or voice activity detection. The most commonly used neural network is the multi-layer feed-forward (MLF) neural network and it is very useful in practice since it could represent a set of very non-linear functions. A MLF neural network is a few layered structures consisting of neurons as seen in Figure 2. A MLF neural network has an input layer, one or more hidden layers, and an output layer. The most widely used network structure has one hidden layer [39]. The MLF networks could be trained with a back-propagation learning algorithm [40].

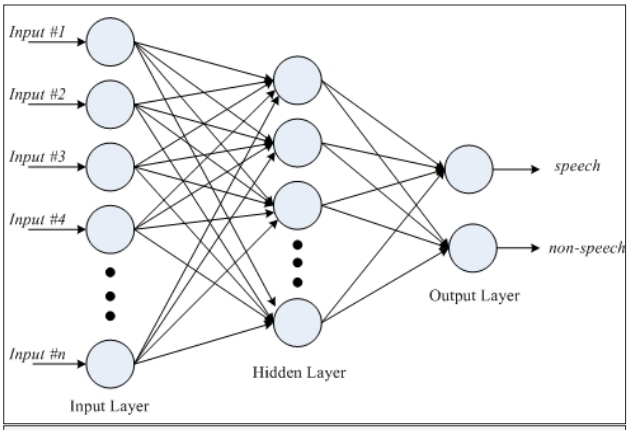

Figure 2. A structure of multi-layer feed-forward neural network
128x83 mm (96x96 DPI)

Each neuron sums its inputs from the previous layer of neurons and passes it through a transfer function. The first layer is the input layer and is completely connected to the hidden layer through a set of weights. Similarly, the hidden layer is completely connected to the output layer through another set of weights. A clean speech sequence can be applied at the input layer and the decision of speech or non-speech sequence will be obtained at the output layer for an appropriately trained neural network.

Transfer Function

Within any single processor, the summation of the incoming connection activity is performed by calculating the sum of the products of the respective weights and input activity:

$$x_j = \sum_i w_{ji} * y_i \tag{10}$$

where *j* is the index number for the processor in the layer under consideration, y is the output level of the th processor in the previous layer, and w_{ji} *is* the weight for the connection between the *i* th and *j* th processors. The result of this weighted summed process is the activation level, X_j, which is then operated on by the transfer function, *f(x)*, to produce the new output for that processor, $Z_j = f(x_j)$. The transfer function is usually chosen to be non-linear to assist in the formation of a complex representative space. The most commonly used transfer function types are sigmoid or hyperbolic functions. The following log-sigmoid transfer function was chosen and is defined as:

$$f(x) = \frac{1}{1+\exp(-x)} \tag{11}$$

Training and Generalization

The MLF neural network is based on a dual working principle of training and prediction. There is a need of two data sets which are train and test and optimal weights are determined in during the training phase. In prediction (test) mode, network generates an output based on input values with its trained network [40].

Experimental Results

Dataset

The proposed algorithm was tested on English sentences which were taken from TIMIT database [41]. TIMIT corpus consists of 24 individual speakers (16 males and 8 females) of eight different dialects, each with 10 phonetically balanced English sentences which are approximately 3-seconds long. The speech records in the TIMIT database are sampled with 16 kHz. In many studies, the TIMIT sentences were downsampled to 8 kHz [42-45]. In addition, as the sampling rate of the G729B and Sohn VAD was 8 kHz, all data was resampled to 8 kHz for a fair comparison [46]. The TIMIT database consists of 720 different speech samples and 432 and 288 utterances were used for training and testing, respectively. The clean speech signals were corrupted by white, car, babble, airport, street, and train noises from the NOISEX-92 noise database [47].

Performance Evaluation

The proposed VAD algorithm was evaluated according to correct detection P_d, false alarm P_f, and the overall accuracy rate (Acc). To obtain P_d and P_f rates, the speech (voice) and non-speech (silence or noise) regions of clean speech signals were primarily manually labeled. The speech correct hit rate P_d is calculated as the rate of correctly detected labeled speech regions by the VAD algorithm, while the false alarm P_f is calculated as the rate of non-speech is identified as speech. The correct speech hit rate (P_d) and the false alarm (P_f) can be expressed as:

$$P_d = \frac{N_{1,1}}{N_{1,1}^{ref}} \qquad P_f = \frac{N_{0,1}}{N_{1,1}^{ref}} \tag{12}$$

where $N_{1,1}$ represents correctly classified number of speech samples by VAD methods, $N_{0,1}$ represents non-speech samples which are erroneously identified as speech samples and $N_{0,0}$ represents correctly classified number of non-speech samples by VAD methods. N_1^{ref} and N_0^{ref} represent correct speech and non-speech samples that manually labeled samples taken from the database, respectively. The overall accuracy rate (Acc) is calculated as:

$$Accuracy = \frac{N_{1,1} + N_{0,0}}{N_1^{ref} + N_0^{ref}} \tag{13}$$

Since there are always trade-off relationships among these two metrics, we use the mean of overall accuracy, P_d and P_f as the final metric for better performance comparison. For an ideal VAD algorithm, the speech or non-speech correct detection rate and overall accuracy rate should be maximized, while the false alarm rate should be minimized.

Implementation

The time resolution is limited in determining the speech regions and is much lower than the sampling rate of the speech signal. Therefore, the decision rule for determining the regions of speech was not calculated for each sample of the signal. Instead, the speech signals were processed by dividing them into short frames [24]. In this study, the speech signals were divided into overlapping frames by using Hamming window. As with most VAD applications, the duration of overlapping frames were 20 ms, which implies that each frame consists of 160 samples, and shifted by 10 ms between frames [45, 48, 49]. In TIMIT database, speech frames (segments) were manually marked for identifying speech or non-speech regions. In this study, Gradient Descent (GD), Gradient Descent with Adaptive (GDA), the Broyden–Fletcher–Goldfarb–Shanno (BFGS) Quasi-Newton and Levenberg-Marquardt (LM) learning algorithms were used to train the MLF neural network. The learning algorithm was used in the training of the network, since there was a very small difference between the minimum error values reached by these learning algorithms (approximate error 10^{-6}) and the same error value was reached with less iteration by the LM algorithm. Log-sigmoid transfer function was chosen as the activation function in MLF neural network structure, which was trained with Levenberg-Marquardt learning algorithm.

In this study, the input layer consists of 6 neurons, the single hidden layer consists of 15 neurons and the output layer consists of 2 output neurons. The most appropiate number of neurons in the hidden layer were chosen by testing different

combinations. In the MLF-NN network, the first neuron of the output layer yields the speech regions (voice) and the other output neuron yields the non-speech regions. The weights were initially adjusted to some small random values close to zero and these weights were updated during the training of the network and the output produced was matched with the correct output. Only clean speech signals were used in training and the signals used in training were not used in the test. The estimated VAD results of the network output were compared with manually labeled VAD results.

Figure 3 shows the short-time energy, zero-crossing rate (ZCR), spectral entropy (SE), spectral flux (SF), spectral centroid (SC), and spectral roll-off (SR) acoustic parameters of segmented noisy speech in white noise condition. In the determination of speech or voice segments, high energy, low ZCR, SE, SF, SC, and SR values were used.

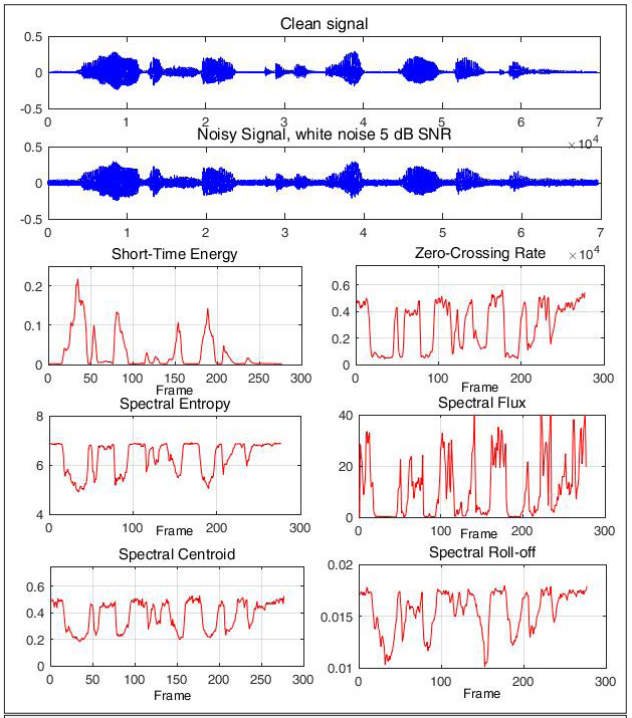

Figure 3. Results of short-time energy, ZCR, SE, SF, SC and SR for speech signal corrupted by white noise at 5 dB SNR level
240x245 mm (72x72 DPI)

The proposed, LSFM, SOHN and G729B VAD algorithms with a clean speech ("He picked up the dice for a second roll") and its noisy version (SNR = 0 dB) is shown in Figure 4. First, the voice regions of noisy speech signal was manually labeled. Then, the neural network structure was trained with clean speech signals and the network were tested for noisy signals. In Figure 4, the voice and unvoiced segments were determined with 92.14% accuracy rate for the proposed VAD algorithm.

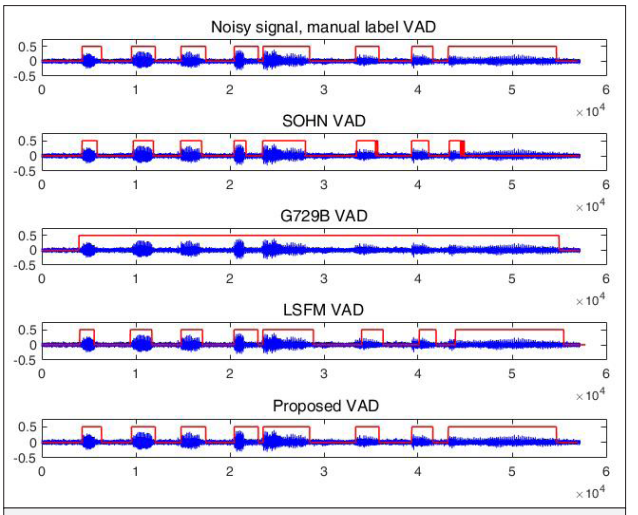

Figure 4. From top to bottom: Clean signal, Noisy signal, Manually labeled VAD, SOHN VAD, G729B VAD, and proposed VAD method results for 0 dB SNR white noise conditions
270x203 mm (72x72 DPI)

The accuracy performances of SOHN, G729B, LSFM and the proposed VAD algorithms in six different noise types and four different SNR level conditions are given in Table 1. As given in the table, although the correct detection rate of the speech regions using SOHN and G729B VAD algorithms is high, the false alarm rate and overall accuracy rates are not reasonable. This means that in traditional VAD methods, the speech regions are determined as non-speech regions. The recommened VAD algorithm plays an important role to overcome this problem. Also, LSFM VAD is able to determine speech regions with high accuracy, especially at low SNR levels. The proposed method has effective and successful results in terms of high correct speech rate (P_d), low false alarm (P_d), and high overall accuracy rate compared with other methods for various noisy environments.

Conclusion

This article has proposed a voice activity detection method based on time and spectral features using multi-layer feed-forward neural network classification. In traditional VAD methods, it is necessary to determine an appropriate threshold value to distinguish between voice and other regions. In this way, VAD methods based on the threshold value may be insufficient in noisy environments. In order to overcome this problem, VAD method based on a classification algorithm was used to distinguish between speech and non-speech regions in both clean and noisy environments. We suggested time and spectral based features for speech/non-speech decisions. The time domain features which are short-time energy and zero-crossing rate and spectral domain features which are entropy, centroid, flux, roll-off and a well-trained MLF-NN were utilized to identify and label parts that are speech and non-speech. Finally, the recommended method was objectively evaluated in six kinds of noises at different SNR levels. The suggested approach was also compared with LSFM, SOHN, and G729B VAD techniques

Table 1. The correct speech rate P_d, false alarm P_f and overall accuracy rate of the proposed, Long-Term Spectral Flatness (LSFM), SOHN and G729B VAD for different noisy environments

		Proposed VAD			LSFM VAD			SOHN VAD			G729B VAD		
Noise	**SNR**	**P_d**	**P_f**	**Acc**	**P_d**	**P_f**	**Acc**	**P_d**	**P_f**	**Acc**	**P_d**	**P_f**	**Acc**
	15	99.32	2.64	96.22	96.52	3.61	92.85	86.85	16.60	85.92	99.97	41.12	58.16
White	10	97.58	2.32	95.52	94.68	3.25	91.05	81.83	9.41	84.00	99.93	42.19	57.73
	5	94.00	1.97	93.70	92.72	2.56	89.32	71.17	3.16	81.43	97.90	42.38	57.75
	0	91.54	1.20	90.11	91.68	1.92	88.17	52.28	2.69	71.75	95.73	42.40	57.68
	15	98.38	2.62	95.43	96.39	3.48	92.30	85.89	27.60	72.61	99.92	42.36	57.79
Babble	10	97.02	2.98	93.78	94.81	4.27	91.53	79.64	27.30	70.63	98.90	42.35	57.77
	5	93.18	6.82	89.22	93.35	4.82	88.14	68.46	28.70	65.64	98.80	42.32	57.82
	0	90.15	8.85	83.71	91.05	6.16	84.72	51.97	32.60	57.75	96.60	42.34	57.76
	15	98.01	2.53	93.06	95.71	3.78	91.75	79.06	22.08	74.61	99.90	38.60	62.12
Car	10	97.95	2.55	91.77	93.60	4.16	88.66	63.60	19.90	69.32	99.72	40.23	61.68
	5	94.72	6.50	87.89	90.45	7.03	84.36	61.62	19.21	60.12	98.10	40.81	60.25
	0	90.80	9.14	80.73	87.12	11.08	75.26	58.99	20.20	50.29	95.21	40.68	60.12
	15	97.74	2.91	93.20	93.19	8.42	89.14	81.08	26.32	71.98	99.91	40.95	60.15
Train	10	96.06	4.96	90.41	91.95	9.61	86.90	68.35	25.20	67.89	99.70	40.30	61.15
	5	94.57	5.57	80.10	90.02	10.15	83.64	58.77	26.20	59.86	98.86	39.48	62.22
	0	91.44	6.54	78.32	88.83	11.78	80.36	55.56	31.82	49.60	96.00	38.78	62.61
	15	98.71	1.57	91.52	95.79	5.71	90.13	82.78	27.74	71.44	99.91	41.99	58.43
Airport	10	98.67	1.60	90.79	94.36	6.08	87.91	71.01	27.60	67.27	99.83	41.91	58.54
	5	97.52	2.78	86.41	91.97	8.13	83.27	62.76	29.93	64.45	98.60	41.78	58.72
	0	93.89	6.13	78.63	89.31	8.86	80.49	51.27	24.49	59.81	95.12	41.67	58.83
	15	98.43	1.99	93.21	96.34	2.76	91.53	75.54	35.35	72.43	96.97	41.94	60.65
Street	10	98.44	1.92	91.61	95.05	2.91	89.28	71.98	39.75	68.55	95.92	42.55	59.12
	5	95.11	5.85	87.03	93.72	4.03	85.75	70.31	33.46	61.54	94.74	47.72	58.94
	0	92.02	8.01	77.08	91.24	7.12	80.46	63.91	26.87	51.42	92.70	48.35	58.32

VAD: voice activity detection; LSFM: Long-Term Spectral Flatness; SNR: signal-to-noise ratio

for better ratification of its accomplishments and capabilities. Although only clean speech signals were used in training and the training duration of the MLF network is long, this VAD algorithm based on time and spectral speech parameters can be recommended for high probabilities of voice activity, high accuracy rate and low probabilities of false-alarm in determining the regions of speech or non-speech activity. Experimental results show that the proposed algorithm performs well in most low and high SNR level conditions for different noise environments.

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RESEARCH ARTICLE

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Design and Modeling of Solar Photovoltaic System Using Seven-Level Packed U-Cell (PUC) Multilevel Inverter and Zeta Converter for Off-Grid Application in India

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ABSTRACT

In the present study, standalone operation of the solar photovoltaic system with storage is evaluated with the recently introduced seven-level packed U-cell (PUC) multilevel inverter. Zeta converter is used to regulate the output voltage of the photovoltaic (PV) array with the help of the MPPT algorithm. Level-shifted modulation scheme is applied for the PUC inverter. The standalone operation is taken into consideration keeping in view the application/penetration of the solar PV system in remote areas. The Ministry of New and Renewable Energy (MNRE), Government of India has set up the plan to establish the standalone solar PV system for off-grid application in the regions to meet the power requirement of those communities and regions that are difficult to connect with the grid. The climatic condition in the central and western parts of India is conductive for solar PV generation. In contrast to the other well-known inverter topologies, such as neutral point clamped, flying level capacitors, and cascaded H-bridge, among others, PUC inverter requires the least number of switches and capacitors for the same output levels. The system is modeled in the MATLAB®/Simulink using the Waaree Energies WSM-315 modules to supply a load of 2 kW. To optimize the solar PV-based system, incremental conductance optimization technique is used.
Keywords: Multilevel inverter, packed U-cell inverter, solar PV array, incremental conductance technique

Introduction

Energy is one of the most fundamental parts of our universe. The use of energy is essential for our lives especially electrical energy. All electronic devices require electricity for power. Among the renewable energy sources, solar energy is easily available at different locations in comparison with geothermal and wind energy that are too site specific. To meet the required demand of electrical energy and the environmental challenges (increasing pollution), solar-based energy system is a viable option [1]. The widespread applications of the solar photovoltaic (PV) array in off-grid application are due to its simplicity in installation and operation [2]. The recent focus of researchers worldwide is to optimize the three following things in a solar system: (1) increasing the efficiency of the system, (2) reducing the installation cost, and (3) increasing the reliability. The topology used in the present study is meeting all the above three mentioned requirements (efficiency, reliability, and overall cost).

Multilevel inverters are used to achieve high power from medium voltage source. They are emerging because of their advantages compared with conventional inverters. Multilevel output is achieved by synthesizing various voltage levels [3]. Although they do not provide the pure sinusoidal output voltage, there is a considerable improvement in total harmonic distortion (THD) compared with its two-level counterpart, thus mitigating the power quality issues [4]. The IEEE standard 519-2014 "Compliances, updates, solutions and case studies" put a limit on harmonics voltage and current at the point of common coupling. This standard fixes the harmonics limit of 5% for current and 8% for voltage waveforms [5].

Packed U-cell (PUC) inverters have a number of advantages in comparison with traditional multilevel inverters, such as low device count [6], reduced complexity in control, and overall good power quality [7]. PUC multilevel inverters were introduced in 2008 by the deduction of CHB in which two switches have been removed and two cells are connected directly

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[8]. PUC seven-level inverter only needs one DC source and one capacitor with reduced structure as compared with other multilevel inverters for the same number of levels in output voltage [9].

The complete model of the system obtained in the present study is shown in Figure 1. It consists of PV modules, such as a power source, and the MPP tracking algorithm is applied on zeta converter and PUC converter. The complete system is modeled and analyzed. For the modulation of PUC inverter, two modulation schemes (belonging to the family of level-shifted modulation), namely, (1) in-phase disposition pulse width modulation (IPD-PWM) and (2) phase opposition disposition PWM (POD-PWM) have been applied with intelligent switching combination of power converters.

A comparative analysis of the above-mentioned modulation schemes applied on the PUC-7 inverter is presented, and a comparison is done based on the power quality of output. The comparison done in the present study is based on the real parameters of the system.

The present study presents the solar PV system by using the recently introduced PUC inverter interfacing with the zeta converter, working as boost converter. A PUC inverter-based PV system using zeta converter is still unexplored. In the present study, a designing of the PV system with zeta converter is designed, modeled, and simulated in MATLAB®/Simulink environment.

Solar modules from the Waaree Energies WSM-315 have been obtained that are easily available in India and have the highest power rating among all available solar PV panel. The simulation is performed at a solar irradiation of 900 W/m^2 and at a temperature of 28 °C, which are an average insolation and temperature value in the northern region of India.

The study is organized as follows. Section 2 explains the design of the solar array and zeta converter. Section 3 shows the operation of the PUC inverter. Section 4 discusses the modeling of the PV cell and MPPT technique. Section 5 presents the theoretical analysis of carrier-based PWM schemes. Section 6 shows the experimental validation of the inverter system. Finally, Section 7 presents the conclusion.

Design of the system

The design of the system consists of the design of the PV array, design of the zeta converter, and PUC inverter operation.

Design of the PV array

A typical house has a load of 2 kW; hence, the system is modeled for the 2 kW load. The Waaree Energies-315 solar PV module has been selected. The specification of the Waaree Energies WSM-315 module of PV cell is given in Table 1.

The number of modules connected in series/parallel can be calculated by defining the voltage of the solar PV array at MPP under standard test condition as V_{mmp} =140 V

$$I_{mpp} = \frac{P_{mpp}}{V_{mpp}} = \frac{2000}{140} = 14.28\ A. \quad (1)$$

The number of modules in series required is calculated in Eq. (2):

$$N_S = \frac{P_{mpp}}{V_{mpp}} = \frac{140}{35} = 4 \quad (2)$$

Table 1. Specification of the Waaree Energies WSM-315 module PV cell

Parameters	Values
Peak power P_m	315 W
Voltage at MPP	35 V
Short circuit current	9.77 A
Current at MPP	9.0 A
No. of cell connected	72
Shunt resistance R_{sh}	313.3991 Ω
Series resistance R_{se}	0.39385 Ω

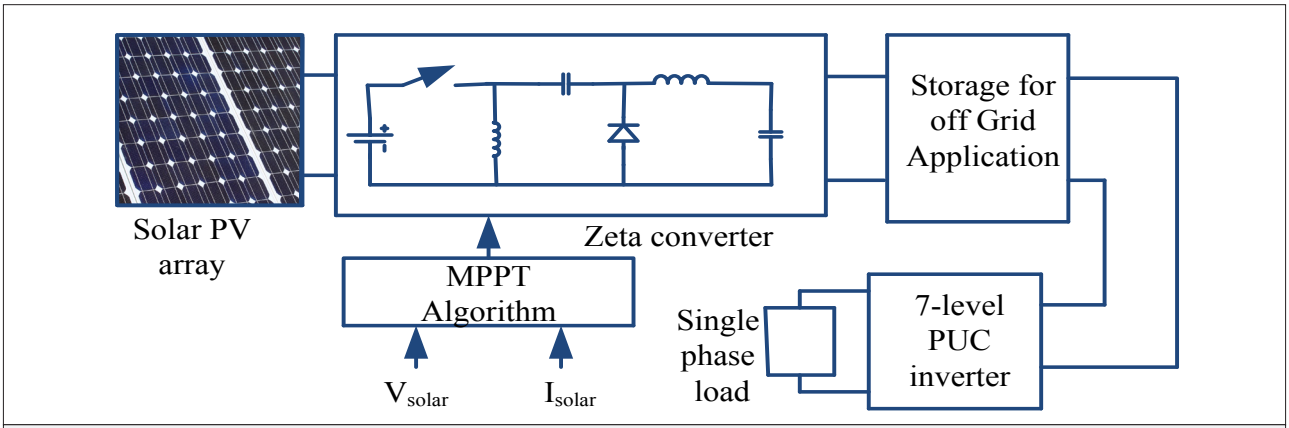

Figure 1. Block diagram of single-phase solar PV-based PUC inverter

The number of modules parallel required is calculated in Eq. (3):

$$N_P = \frac{I_{mpp}}{I_m} = \frac{14.28}{9} \cong 2 \quad (3)$$

Therefore, the solar PV array has two parallel paths with each path consisting of four modules.

Design of the zeta converter

Zeta converter is shown in Figure 3. It belongs to the family of buck-boost converter, but it draws continuous current in contrast to the buck-boost converter. The continuous current is because of the output inductance that ensures ripple-free current. With respect to component count, it comprises the same number of components as Cuk converter [10]. Moreover, in contrast to the Cuk converter, it operates in non-inverting mode means, and output voltage has the same polarity as input in contrast to the buck-boost converter; hence, the problem of negative voltage sensing is eliminated [11]. Different buck-boost converter configurations and their application to the inverter operation are reported in the literature. The reasons for using the zeta converter are its advantage over other converters as follows:

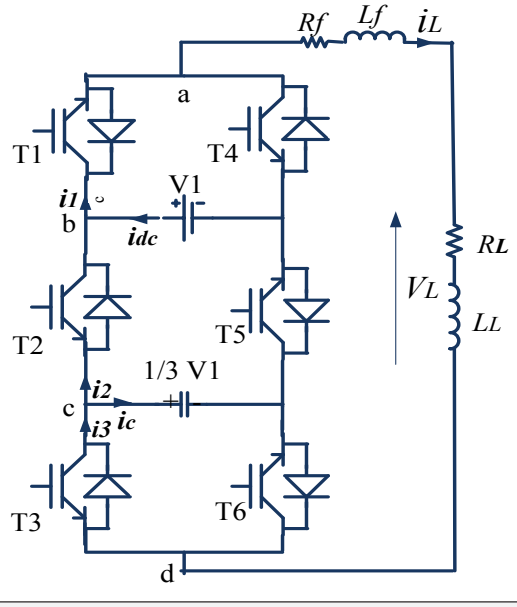

Figure 2. Packed U-Cell converter topology

1. A conventional buck-boost converter has a low component count. However, the output current is pulsating in nature that increases the ripple in output voltage.
2. SEPIC also depicts a pulsating output current. As the output stage of the power supply is very sensitive, this pulsating current is not desirable.
3. The flyback converter suffers from leakage inductance problem that imposes a limit on its rating.

To eliminate these issues, a zeta converter is employed as a buck-boost converter in the present study. It provides a continuous output current with a low ripple output voltage along with a high-level performance that is highly recommendable for solar PV applications. Its design includes the calculations of various components, such as L_1, L_2 and C_1. It always operates in CCM to reduce the stress on its elements

The design of the zeta converter is done by first estimating the duty cycle D as given by Eq. (4) [12]

$$D = \frac{V_{dc}}{V_{dc}+V_{mpp}} = \frac{250}{250+140} = 0.64 \quad (4)$$

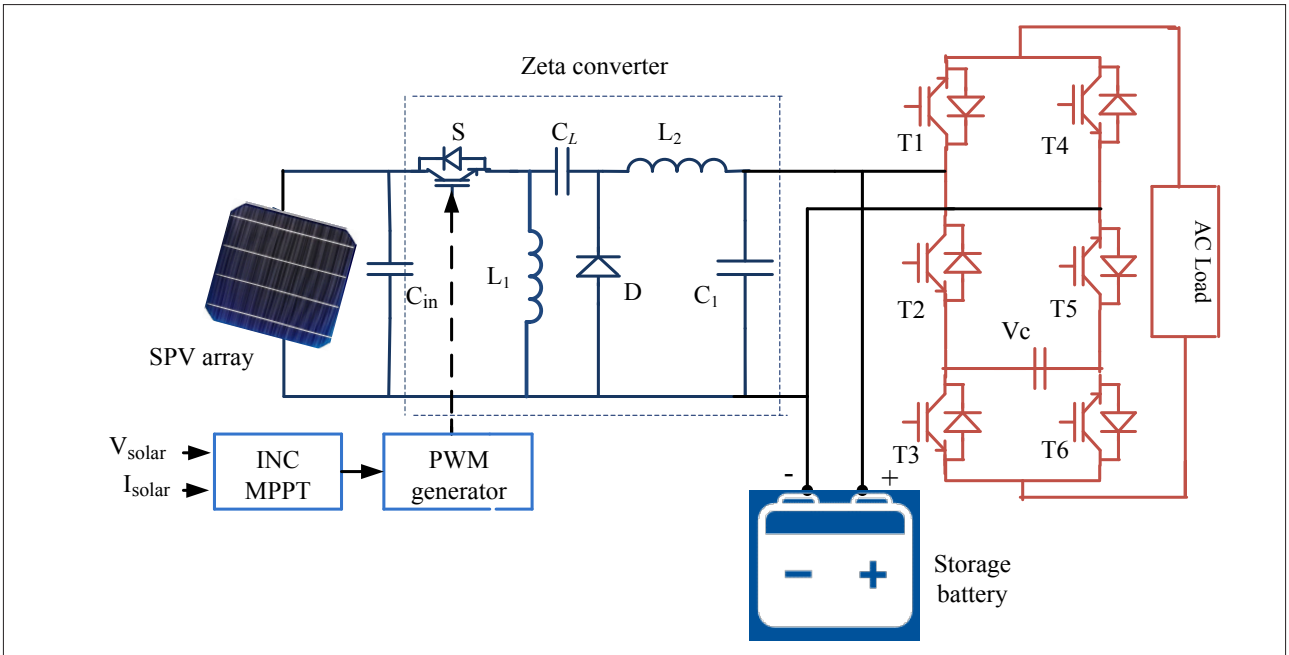

Figure 3. Proposed solar PV with zeta converter topology

Table 2. Switching table for PUC-7 inverter

States	Voltage	T1	T2	T3	T4	T5	T6
0	Va	1	0	0	0	1	1
1	Va–Vc	1	0	1	0	1	0
2	Vc	1	1	0	0	0	1
3	0	1	1	1	0	0	0
4	0	0	0	0	1	1	1
5	–Va	0	1	1	1	0	0
6	Vc–Va	0	1	0	1	0	1
7	–Vc	0	0	1	1	1	0

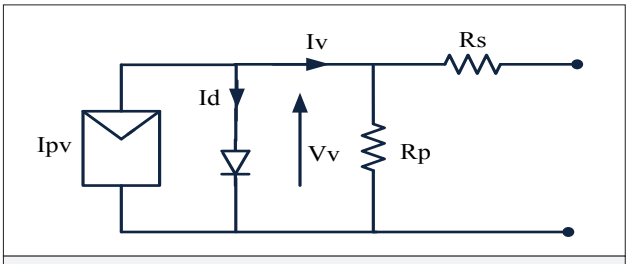

Figure 4. Single PV cell model

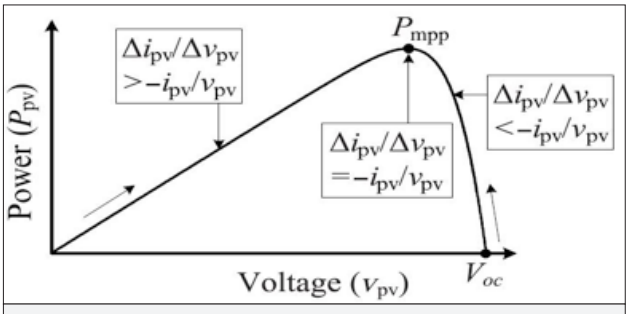

Figure 5. Illustration of the INC MPPT technique

Where V_{dc} is an average output voltage of the zeta converter equal to the rating of the load connected. The average value of the current flowing through the DC link of the inverter is given by [12]:

$$I_{dc} = \frac{P_{mpp}}{V_{dc}} = \frac{2000}{250} = 8 \text{ A.}$$

Then L_1, L_2 are C_1 calculated in Eqs. (5), (6), and (7):

$$L_1 = \frac{D \times V_{mpp}}{f_{sw} \times \Delta I_{L1}} = \frac{0.64 \times 140}{5000 \times 14.28 \times 0.06} = 20.9\ mH \quad (5)$$

$$L_2 = \frac{(1-D) \times V_{dc}}{f_{sw} \times \Delta I_{L2}} = \frac{(1-0.64) \times 250}{5000 \times 8 \times 0.06} = 37.5\ mH \quad (6)$$

$$C_1 = \frac{D \times I_{dc}}{f_{sw} \times \Delta V_{C1}} = \frac{0.64 \times 8}{5000 \times 250 \times 0.1} = 41\ \mu F \quad (7)$$

Where f_{sw} is the operating frequency of IGBT used in the zeta converter, ΔI_{L1} is the value of allowed ripple in the current through L_1, is ΔI_{L2} the value of allowed ripple in the current through L_2, and $I_{L1} = I_{mmp}$ and $I_{L2} = I_{dc}$.

Operation of the PUC inverter

The circuit topology for seven-level PUC inverter is shown in Figure 2. For seven-level operation, the capacitor voltage has to be maintained at one-third of the DC link voltage. The seven-level output can be obtained by switching scheme as shown in Table 2. The relationship between number of voltage level and number of capacitor is given by Eq. (8) [13,14]:

$$N_V = 2^{Nc+2} - 1 \quad (8)$$

Where is N_v the number of output voltage levels, and N_c is the number of capacitor used.

With reference to Figure 2, the switching function of the PUC inverter is defined by Eq. (9), and inverter output is defined by Eq. (10)

$$\left.\begin{aligned} T_i &= 0 \quad if\ T_i\ is\ off \\ &= 1 \quad if\ T_i\ is\ on \end{aligned}\right\} \quad (9)$$

$$V_{ad} = V_{ab} + V_{bc} + V_{cd} \quad (10)$$

Based on the switching table shown in Table 2, each voltage can be expressed as

$$V_{ab} = V_1(T_1 - 1) \quad (11)$$

$$V_{bc} = (V_1 - V_2)(1 - T_2) \quad (12)$$

$$V_{cd} = V_2(1 - T_3) \quad (13)$$

Hence, by combining Eqs. (11), (12), and (13), Eq. (10) can be presented as:

$$I_{pv} = I_{ph} - I_d = I_{ph} - I_s\left(exp\left(\frac{qV_V}{akT}\right) - 1\right) \quad (14)$$

Modeling of the solar PV array and INC MPP tracker

The modeling of the single-cell model of the PV cell is shown in Figure 4. The PV cell current is given by Eq. (15) [12,16]:

$$I_{pv} = I_{ph} - I_d = I_{ph} - I_s\left(exp\left(\frac{qV_V}{akT}\right) - 1\right) \quad (15)$$

For N_s and N_p, the number of connected cells in series and parallel, respectively, Eq. (15) is modified and given as Eq. (16):

$$I = N_p I_{ph} - N_p I_s\left(exp\left(\frac{q(V + R_s I)}{aN_s kT}\right) - 1\right) - \frac{V + R_s I}{R_p} \quad (16)$$

Where I_{ph} is the photocell current that only depends on solar insolation, I_s is the diode reverse saturation current, and R_s and R_p are the total series and parallel resistance of the PV array.

Maximum power point is defined by the point on the power curve at which $\frac{dP_{Pv}}{dV} = 0$, the slope $\frac{dP_{pv}}{dV}$ is positive or negative on the left or right of this point, and the maximum point is calculated by Eq. (17)

$$\frac{dP_{Pv}}{dV} \cong I + V\frac{\Delta I}{\Delta V} \quad (17)$$

Incremental conductance (INC) MPPT algorithm has a relationship between instantaneous conductance $\frac{I_{pv}}{V_{pv}}$ and ICC $\frac{\Delta I_{pv}}{\Delta V_{pv}}$ given by Eq. (18) and shown in Figure 5.

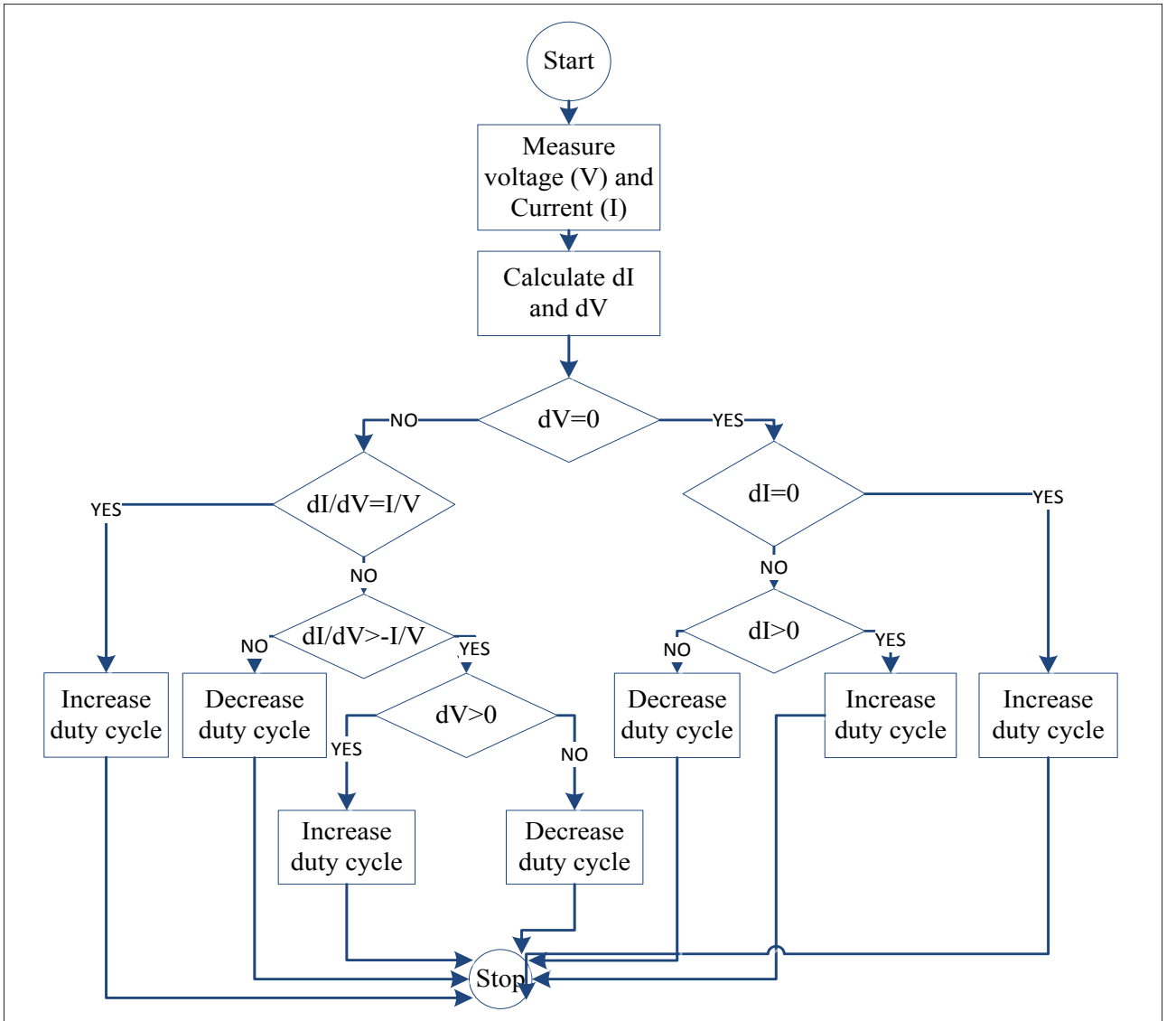

Figure 6. Flowchart of incremental conductance algorithm

$$\left.\begin{array}{l} \frac{\Delta I_{pv}}{\Delta V_{pv}} = -\frac{I_{pv}}{V_{pv}} \text{ at MPP point} \\ \frac{\Delta I_{pv}}{\Delta V_{pv}} > -\frac{I_{pv}}{V_{pv}} \text{ at left of MPP point} \\ \frac{\Delta I_{pv}}{\Delta V_{pv}} < -\frac{I_{pv}}{V_{pv}} \text{ at right of MPP point.} \end{array}\right\} \quad (18)$$

The error between INC and instantaneous conductance must be reduced to zero to enhance the tracking dynamics [17]. The flowchart of the INC algorithm is shown in Figure 6.

Simulation and analysis of the proposed system

Solar PV array and storage system

The I–V and P–V characteristics of the Waaree energy solar PV module are shown in Figure 7. The solar PV cell is simulated for an average insolation of 900 W/m^2 with a temperature of 28 °C. The battery will provide power when solar insolation is not present and it gets charged when extra power is available. The battery also enhances the dynamic stability of the inverter and improves the response [18]. Figure 8 shows the battery discharging characteristics. The specification of the battery is 250 V, 15 Ah. The open circuit voltage is calculated from its nonlinear Eq. (19) based on the actual state of charge. Actual battery voltage that depends on the charge/discharge current is given by Eqs. (20)–(22) [19].

$$E_{oc} = E_o - k\frac{Q}{Q-it} + Ae^{-Bit} \quad (19)$$

$$E_{act} = E_{oc} - \frac{Qk}{Q-it}.it - \frac{Qk}{Q-it}.i^* + Ae^{-Bit} \quad (20)$$

$$E_{act} = E_{oc} - \frac{Qk}{Q-it}.it - \frac{Qk}{it+0.1Q}.i^* + Ae^{-Bit} \quad (21)$$

$$Q = it = \int idt \quad (22)$$

Where E_{oc} is the open circuit battery voltage, E_o is the nominal voltage of the battery, and E_{act} is the actual voltage of the battery at dis-

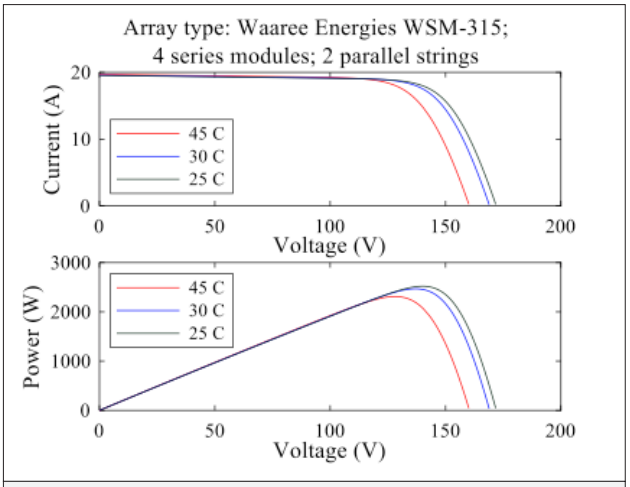

Figure 7. I–V and P–V characteristics of PV array.

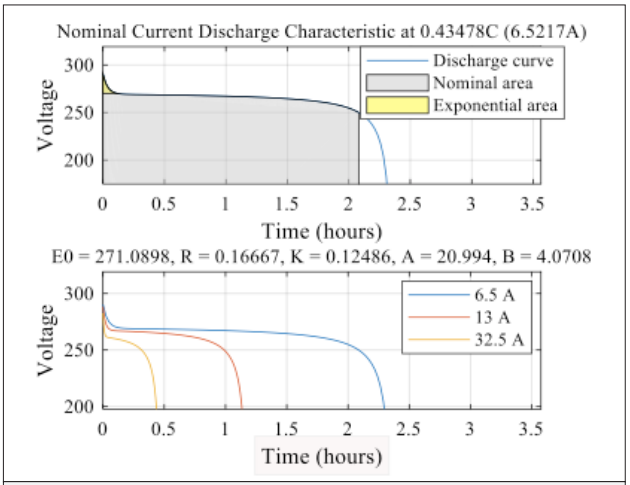

Figure 8. Battery discharging characteristics.

tinct *C* rate. *Q* indicates the maximum battery capacity in Ah. *K* indicates the polarization constant. i^* is the filtered battery current. A and B indicate the exponential voltage and capacity, respectively.

Zeta converter and MPPT performance

Zeta converter shown in Figure 3, is connected directly to the solar PV array. It boosts the voltage to a usable value and also charges the battery when more power is generated by solar array. Switching signal for zeta converter is obtained from the INC algorithm block shown in Figure 3.

Figure 9 shows the duty ratio and corresponding output voltage of the zeta converter as shown in Figure 10. From Figure 10, it can be observed that due to variation in the load condition at *t*=0.2 s, the graph fluctuates and attains a new stable state.

Modulation schemes and control

The system discussed so far is modeled and simulated in MATLAB®/Simulink by using IPD- and POD-PWM schemes.

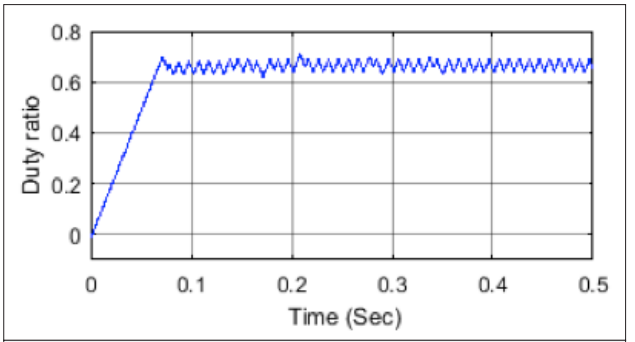

Figure 9. Duty ratio

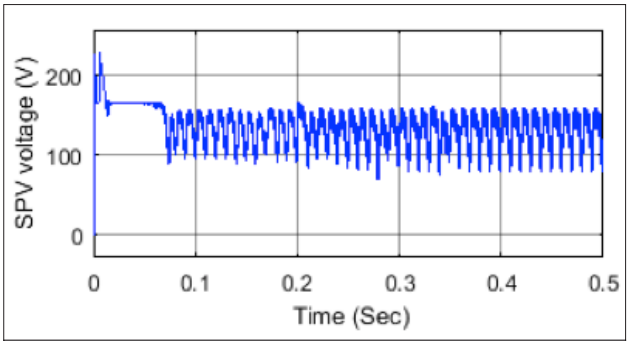

Figure 10. Zeta converter output

The phase voltage of two-level voltage source inverter with PWM and triangular modulating signal can be described as [20]:

$$F(t) = \frac{MV}{2}\cos(\omega_F t) + \frac{2V}{\pi}\sum_{m=1}^{\infty} J_o(mM\frac{\pi}{2})\sin(m\frac{\pi}{2}) .\cos(m\omega_c t) + \frac{2V}{\pi}\sum_{m=1}^{\infty}\sum_{n=1}^{\pm\infty}\frac{J_n\frac{mM\pi}{2}}{m} .sin\left((m+n)\frac{\pi}{2}\right)cos(m\omega_c + n\omega_F t) \quad (23)$$

Where *M*=modulation index, ω_c=freq. of carrier (rad/s), ω_F= =freq. of fundamental (reference), *V*=supply voltage (V), and J_o, J_n =Bessel function of the first kind.

Eq. (23) comprises three terms:

(a) The first term gives the amplitude of the fundamental component that is proportional to modulation index *M*.

(b) The second term shows the amplitude of the harmonics content at the carrier and multiple of the carrier frequency.

(c) The third term gives the amplitude of the harmonics at side band.

Level-shifted IPD-PWM multicarrier schemes for PUC inverter are shown in Figure 11. Figure 12 shows the POD-PWM scheme. The frequency of carrier wave is obtained as 5000 Hz.

For seven-level output, capacitor voltage has to be maintained at one-third of the DC link voltage [21]. A PI controller is used for this purpose. The controller block diagram is shown in Figure 13. The PI controller reduces the error and improves the dynamic stability of the inverter [22].

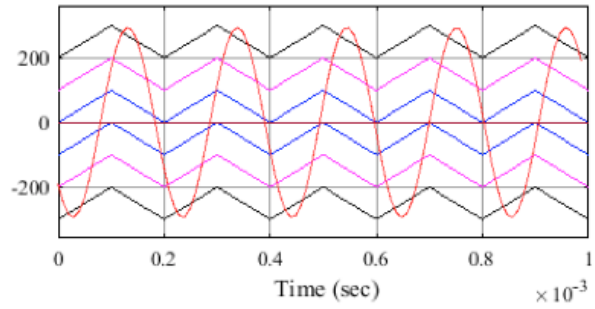

Figure 11. IPD-PWM scheme for PUC-7 inverter

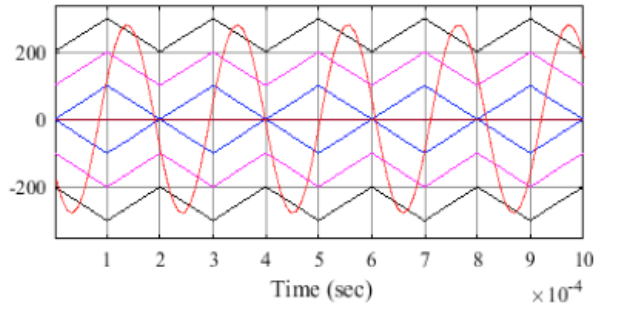

Figure 12. POD-PWM scheme for PUC inverter

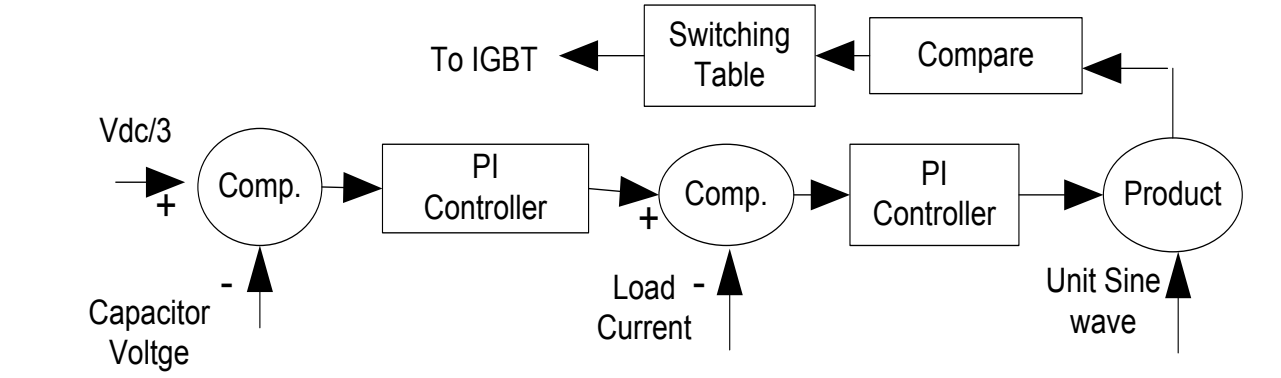

Figure 13. Voltage balancing controller

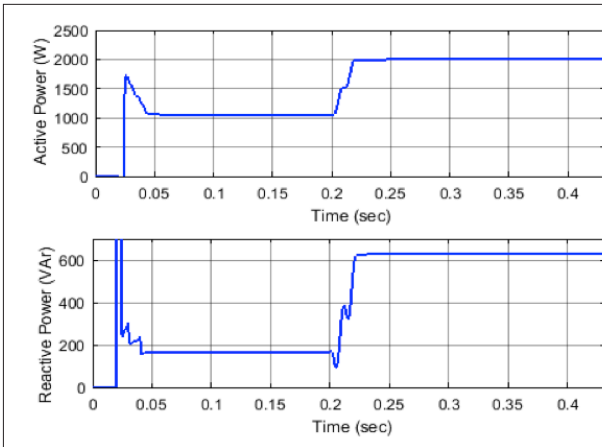

Figure 14. Active and reactive powers of inverter

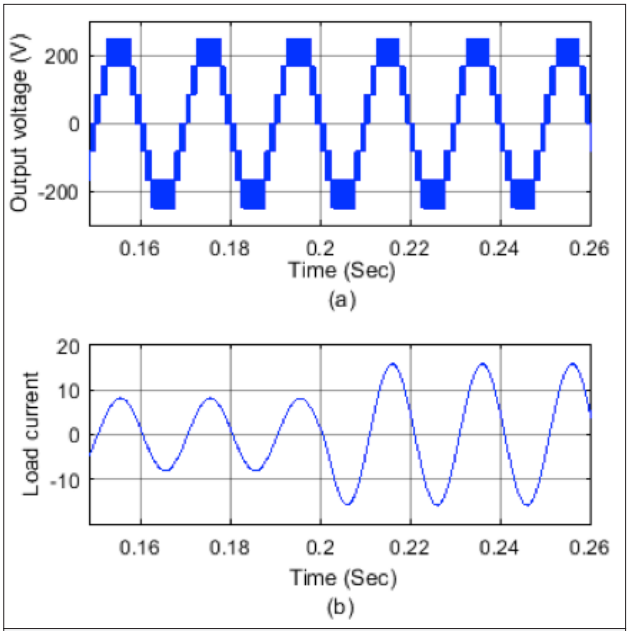

Figure 15. a, b. (a) Output voltage (a), load current in IPD-PWM (b)

The simulated capacity of the inverter with respect to active power and reactive power is shown in Figure 14. The model is simulated for 2 kW load that can be seen from Figure 14.

Performance under the IPD-PWM schemes

Figure 15 shows the output voltage and current waveform of the PUC inverter, at time *t*=0.2 s. The load is doubled (by connecting additional 40 Ω resistive load in parallel) resulting in an increase of load current as shown in Figure 15. Initially, the current is 5.8 A and at *t*=0.2 s. It becomes 11.33 A rms. The THD in the load current is found to be 0.5% at steady state. The FFT

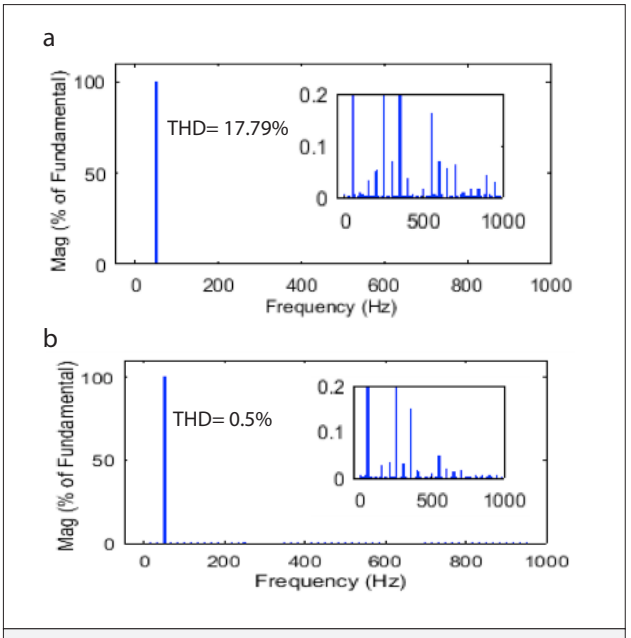

Figure 16. a, b. FFT window for (a) voltage and IPD-PWM scheme (b)

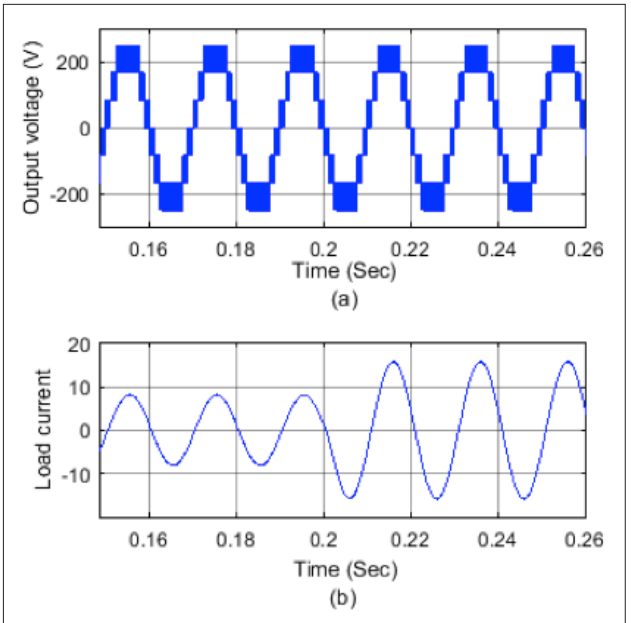

Figure 17. a, b. Voltage (a) and load current in the POD-PWM scheme (b)

analysis of the voltage waveform shows that THD is 17.79% and rms value is 178.1 V.

Capacitor voltage balancing

Figure 13 shows the detailed block diagram of controller used for capacitor voltage balancing (at one-third of the main DC bus voltage) to obtain the seven level at output. Figure 19 shows the capacitor voltage waveform for the POD-PWM scheme. Capacitor voltage varies between 79 V and 87 V with

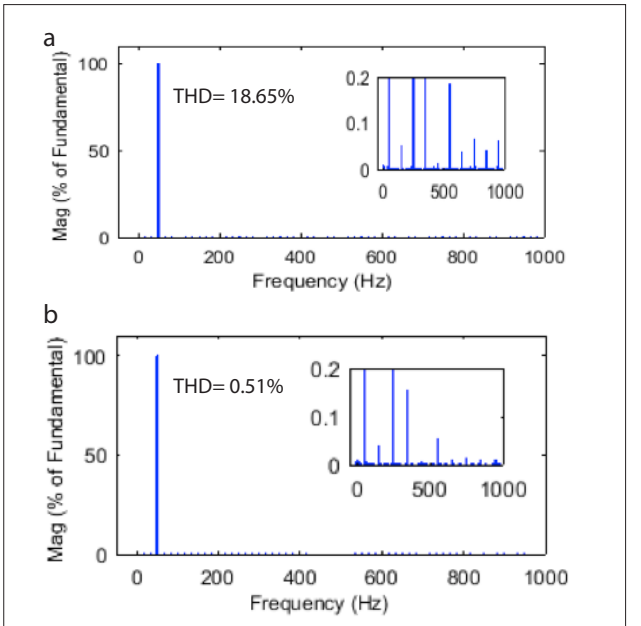

Figure 18. a, b. FFT window for voltage (a) and current in the POD-PWM scheme (b)

Table 3. Simulation parameters

Parameters	Rating
Capacitor	5000 µF
Load resistance	30 Ω
Load inductance	15 mH
Switching frequency	5000 Hz
Load change	20 Ω to 40 Ω at t=0.2 s

Table 4. FFT result for IPD- and POD-PWM schemes

Level-shifted PWM Schemes	*Parameters*	*THD %*
IPD-PWM scheme	Voltage	17.79
	Current	0.50
POD-PWM scheme	Voltage	18.65
	Current	0.51

an average value of 83 V (which is desired). It is unaffected with the load change, which is occurring at 0.2 s, showing the good dynamic performance of the controller.

Performance under the POD-PWM schemes

The POD-PWM scheme carrier waveform for PUC-7 inverter is shown in Figure 12. Reference signal is generated by the voltage balancing controller compared with these carrier signals to produce the switching signals. Figure 17 shows the output voltage and load current for the IPD-PWM scheme. This scheme is simulated for the same load as the IPD-PWM scheme. To analyze the transient behavior, load is changed from 20 Ω to 40 Ω at *t*=0.2 s as shown in Figure 17. FFT analysis of the voltage

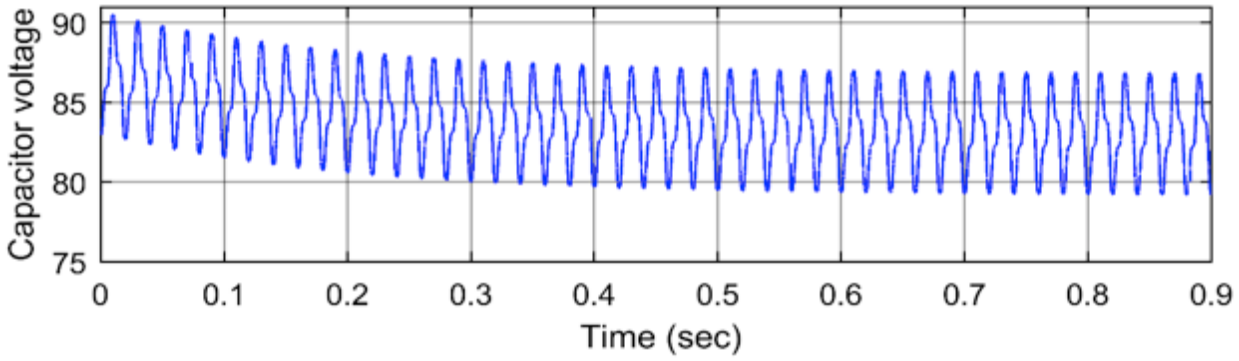

Figure 19. Capacitor voltage in the POD-PWM scheme

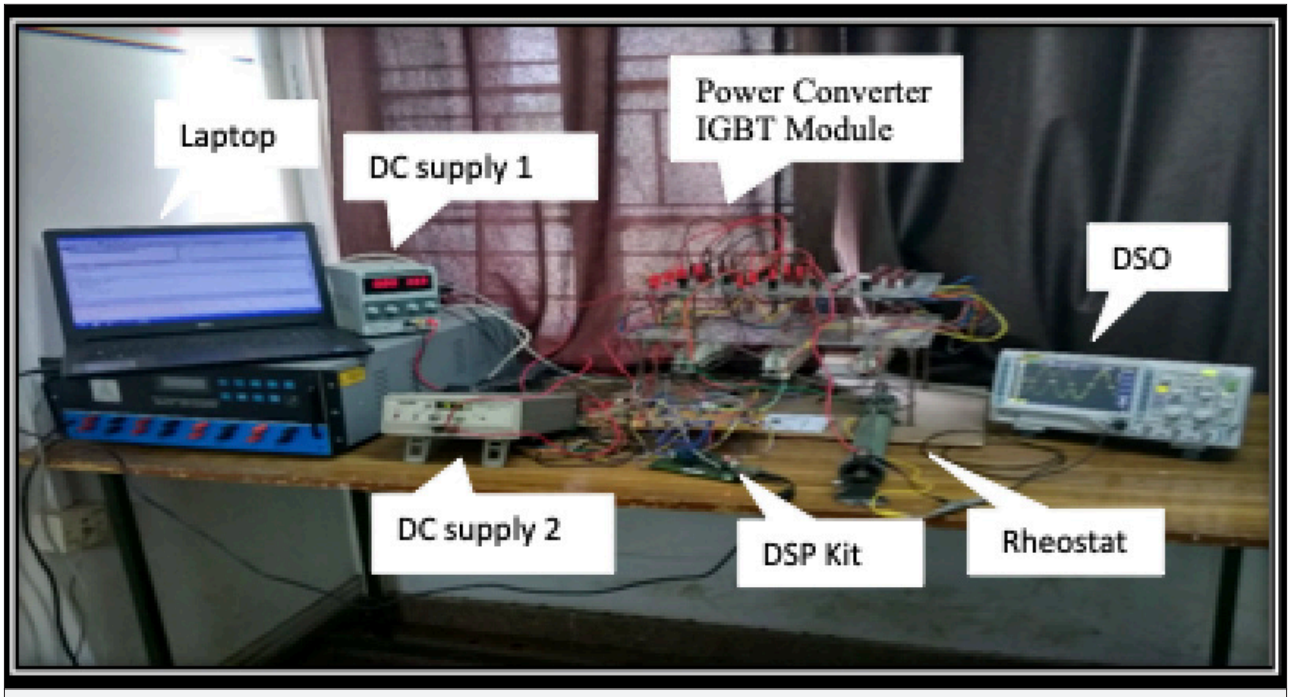

Figure 20. Experimental setup

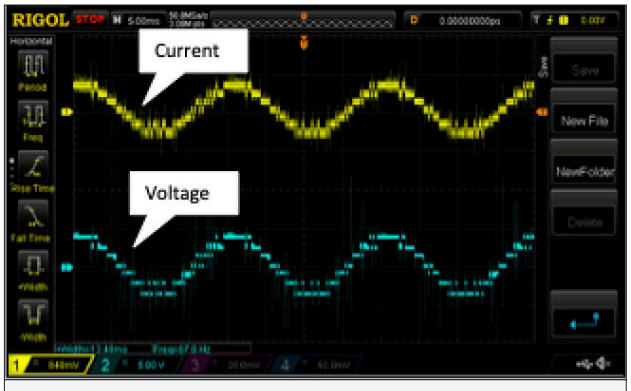

Figure 21. Output voltage and current on DSO of seven-level PUC inverter

Figure 22. Switching signals of PUC-7 level on DSO

waveform is presented in Figure 18. The THD in the voltage wave is found to be 18.65% with an rms value of 175.2 V. FFT window for load current is shown in Figure 18 with 0.51% THD,

Table 5. Parameters of the component used in the experiment

Parameters/Components	***Rating***
Two DC Voltage Supplies	0-15 V, 0-30 V
Fundamental frequency(f_o)	50 Hz
Switching frequency (f_s)	1 kHz
Rheostat	1.5 kΩ
Switches (S_1 to S_6)	SKM75GB063D (SEMIKRON)
Optocoupler	TLP 250 (TOSHIBA)
DSP	TMS320F28335(TI)
Sampling time	1μsec
Dead time	2μsec

and rms value is 11.4 A. Initially, when the load is not increasing, the current is 5.72 A.

Experimental validation

The hardware setup for the PUC multilevel inverter as shown in Figure 1 is presented in Figure 19. The laboratory prototype is fully fabricated in the laboratory. The developed prototype is of a general purpose, user interface, and can be used for the development of other converters, such as DC/DC, AC/DC, and multilevel converters, and so on. This laboratory prototype is used to implement the circuit presented in Figure 1, and the results are experimentally verified. Table 5 lists the parameters of the component used in the experiment. Figures 20 and 21 show the switching pulses required for seven level and the output voltage across the load and current through the load, respectively. Rheostats are used as a load.

Conclusion

The aim of the present study was to analyze and compare between two level-shifted modulation schemes applied on the solar PV-based seven-level PUC inverter interacting with zeta converter. The comparison is performed on the basis of power quality and some feature of zeta converter operation. Table 4 presents the power quality of the proposed system. Based on the simulation result, it is observed that IPD-PWM scheme has 17.79% THD in voltage and 0.50% in load current, whereas POD-PWM scheme has 18.65% THD in voltage and 0.51% in load current waveforms. Device switching frequency and device conduction period in case of IPD-PWM are different for each switch, and the rotation of the switching patters is more uniform as compared with the POD-PWM scheme. This is the reason of getting better performance under the IPD-PWM scheme. Simulation results suggest that the IPD-PWM scheme is favorable for application due to good power quality. The overall system is compact, has good dynamic response, is reliable, and has good power quality. It has the least number of device counts as compared with other conventional multilevel inverters. The topology is verified in MATLAB®/Simulink environment.

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ISTANBUL UNIVERSITY CERRAHPASA

RESEARCH ARTICLE

Electrica 2019; 19(2): 113-119

EDAS/COAS Based Antenna Selection for Code Index Modulation Aided Spatial Modulation

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ABSTRACT

In this study, a new code index modulation (CIM) aided spatial modulation (SM) technique based on the Euclidean distance and capacity optimized based antenna selection (EDAS/COAS), called EDAS/COAS-CIM-SM, is proposed for multiple-input multiple output (MIMO) systems. Since in the proposed EDAS/COAS-CIM-SM technique, incoming information data bits indicates modulated symbols, activated transmit antenna indices as well as their corresponding spreading code indices, data bits are conveyed not only by the modulated symbols but also by the indices of the active antenna and spreading code indices. Thus, the proposed two systems provide faster data rates while spending less transmission power and possessing better error performance than the conventional direct sequence- spread spectrum (DS-SS), SM, EDAS and COAS based SM (EDAS-SM, COAS-SM), and CIM based SS (CIM-SS) systems. In addition, in order to improve the overall performance of the CIM aided SM (CIM-SM) system, EDAS and COAS techniques are considered at the receiver. Computer simulations have also shown that the EDAS/COAS-CIM-SM system has better error performance than the CIM-SM system over the Rayleigh fading channels for binary phase shift keying (BPSK) modulation schemes.

Keywords: Spatial modulation, euclidean distance and capacity optimized based antenna selection, code index modulation, MIMO systems, direct sequence spread spectrum

Introduction

The use of mobile data is growing exponentially in today's world. Concepts such as high-quality video conferencing, high-quality video and audio broadcasting, online gaming, sending and uploading large files, very low latency, need for low power consumption, and the necessity to connect to the internet anywhere and anytime are becoming more and more popular. According to experts' estimates, global internet traffic will exceed 71 Exabytes in 2022 [1]. Therefore, the evolution of new high data-rated, high energy & spectral efficient communication systems has become mandatory. In order to meet the above mentioned needs, many new research topics such as Millimeter Wave (mmWave) communication, Spectrum Sharing, Beamforming, Device-to-Device communication (D2D), Moving Networks (MN), Ultra-dense Networks (UDN), Ultra-reliable Networks (URN), Internet of Things (IoT) Communications, Index Modulation (IM), multiple-input multiple-output (MIMO) are being studied [2, 3].

In order to optimize signal performance, MIMO technique has been studied in many new works. As its name suggests, MIMO structure is based on multi-antenna technology and is a rational technology that increases performance parameters such as data rate, spectral efficiency, and energy efficiency [4]. Spatial Modulation (SM) is one of the most popular methods recently studied in the field of MIMO systems. The SM method utilizes a single radio frequency (RF) chain during the same time period, as well as the advantages of multiple antennas. As a result of the use of a single RF chain, signal processing, and circuit complexity are greatly reduced while energy efficiency increases. In the SM scheme, a single transmitter antenna is selected in each transmission time slot and the extra information is carried on without having to pay any extra cost by detecting which antenna is selected on the receiving side. In other words, antenna indices also contribute the data transmission. The most important features of the SM

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are the multiplication gain increasing in proportion to the logarithm of the number of antennas, the reduction of the transmitter complexity by using a single RF chain, the reduction of power consumption, the reduction of the processing complexity of the receiver, the synchronization and the complete elimination of inter-channel interference (ICI) problems [5].

Antenna selection technique is another scheme in MIMO systems that communicate using a single transmitter RF chain as in SM. In the antenna selection techniques, the antenna with the best channel condition is selected by using the Channel State Information (CSI) and then the transmission is carried out via this antenna. Since communication is made over a single antenna throughout a symbol duration, ICI is eliminated, power consumption and complexity are greatly reduced [6, 7]. The antenna selection techniques that have been of interest in the SM scheme for the last few years are both Euclidean Distance optimized Antenna Selection (EDAS) and Capacity Optimized Antenna Selection (COAS) based techniques, both of which greatly improve performance. Therefore, these techniques will be included in this study in order to increase performance much more. In simple terms, in the EDAS scheme, all possible vector sets are determined and then a specific set of antennas that maximizes the minimum Euclidean distance is found after that the communication is carried out with these antennas. On the other hand, in the COAS scheme, the best antenna selection is found by selecting the antenna that corresponds to the largest channel norms [8, 9]. In addition, the EDAS system is applied to the cooperative-SM scheme in [10].

Over the past few years, there has been a great deal of interest in IM, which is one of the most important research topics of 5G communications. As the name suggests, IM schemes transmit the indices of some medium such as antennas, RF mirrors, sub-carriers, spreading codes, modulation types, antenna activation sequences, etc. embedded in the signal. Thanks to this simple and rational scheme, extra information is transmitted using little or even no energy, spectral efficiency increases, and no additional hardware cost is required [11, 12].

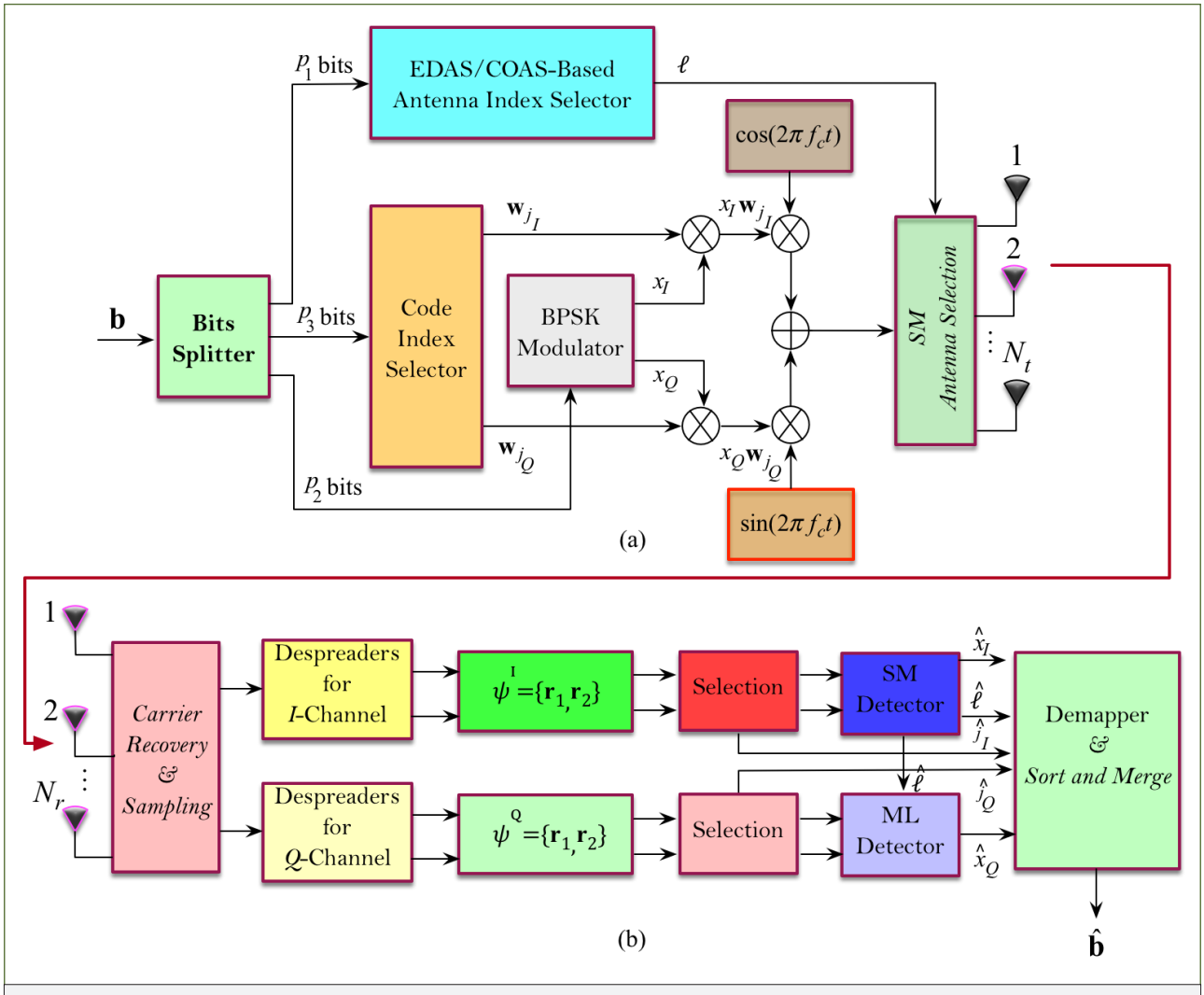

Figure 1. a, b. EDAS/COAS-CIM-SM system model, (a) transmitter, (b) receiver

The IM technique used in this article is the code index modulation aided spread spectrum (CIM-SS) technique, which is considered among the competitors of the SM method. The CIM-SS technique is based on the direct sequence-spread spectrum (DS-SS) method, which is based on sending bit sequences to the receiver side by multiplying them with pseudorandom noise (PN) or spreading codes, thereby resisting noise and jamming. In the CIM-SS method, the extra information bits are transmitted over the orthogonal in-phase and quadrant (*IQ*)-channels by multiplying with spreading codes to the receiver side and this process is called "*spreading*". On the receiver side, the received signal is multiplied again with the spreading codes and is estimated by the correlators and this process is called "*despreading*". Since the extra bits of information are embedded into the spreading code indices, extra information bits are detected without any additional cost by detecting the spreading code. As a result, the CIM-SS method is a fast and secure communication technique because it hosts the advantages of the DS-SS method, transmits information via index modulation, and uses orthogonal channels for information transmission [13, 14]. More than these, a new high data-rated technique called CIM aided SM (CIM-SM), which is a combination of CIM-SS and SM methods, has been introduced at [15, 16] to the literature. The CIM-SM technique is faster, more spectral and energy efficient than the above-mentioned techniques.

In this study, new antenna selection-based MIMO transmission systems with high energy efficiency, high data rate and good error performance, called EDAS/COAS-CIM-SM, is proposed by combining EDAS, COAS, CIM, and SM techniques which are promising in 5G and beyond communication systems. It is shown via computer simulations that the proposed system performs data transmission at a higher rate, consumes less transmission energy, and also has better spectral efficiency and performance than the DS-SS, CIM-SS, SM, CIM-SM, EDAS-SM and COAS-SM techniques.

System Model

The general structure of the proposed EDAS/COAS-CIM-SM system model is shown in Figure 1. The considered system consists of the number of N_t transmitting antennas, N_r receiving antennas, and $N_c = 2$ two different Walsh Hadamard spreading codes, i.e., $\boldsymbol{w}_j = [w_{j,1}, w_{j,2}, \ldots, w_{j,L}]^T$, $j \in \{1,2\}$ are used for the spreading operation. Also, each of spreading codes consists of L chips. N_{SM} out of N_t antennas ($N_{SM} \leq N_t$) refers to the number of antennas which will be activated by the EDAS/COAS technique, and thus, $A = \{\ell\}_{\ell=1}^{N_{SM}}$ expresses the transmission antenna index set. Since EDAS/COAS based antenna selection technique is considered at the transmitter side, the performance of the SM receiver with the EDAS/COAS is better than the traditional SM receiver. Therefore, not only the active antenna index and symbol estimation performance on the receiving side will be improved compared to traditional SM scheme, but also make better the performance of the code index detection compared to CIM-SS and CIM-SM techniques. Binary phase shift keying (BPSK) modulation is envisaged for the proposed system. *IQ*-channel components are used both in the transmitter and receiver sides. It is assumed that the CSI is known at the transmitter and receiver side perfectly. Finally, the considered system structure is designed by adapting EDAS, COAS, SM, CIM techniques and BPSK modulation.

As seen from the transmitter structure of the EDAS/COAS-CIM-SM scheme depicted in Figure 1 is the incoming binary information data bits to be transmitted through one symbol period (T_S). In the considered scheme, **b** is divided into $p_1 = \log_2(N_{SM})$, $p_2 = \log_2(2M)$, and $p_3 = \log_2(2N_C)$ sub-vector groups such that $p = p_1 + p_2 + p_3$. The p_1, p_2, and p_3 sub-block groups of bits are transmitted in the antenna indices of SM, BPSK symbols and indices of spreading codes, respectively. x_I and $x_Q \in \pm 1$ BPSK symbols of the *IQ*-components are determined according to the bits sequence of p_2. The x_I and x_Q are then spreaded by the $\boldsymbol{w}_{j_I}$ and $\boldsymbol{w}_{j_Q}$ spreading code selected by the bits sequence of p_3. Finally, spreaded signals $x_I \boldsymbol{w}_{j_I}$ and $x_Q \boldsymbol{w}_{j_Q}$ are transmitted through *IQ*-components from the l^{th} antenna activated by bits sequence of p_1. From this point forth, the faded noisy signal received by the EDAS/COAS-CIM-SM receiver can be expressed as follows:

$$r(t) = \sum_{l=1}^{L} \Big(x_I w_{j_I} g(t - lT_c)\cos(2\pi f_c t) + x_Q w_{j_Q} g(t - lT_c)\sin(2\pi f_c t) \Big) h(t) + n(t), \quad (1)$$

where, $g(t)$ is the unit rectangular pulse shaping filter on $[0, T_c]$ period time, here T_c is the chip duration of the spreading code. f_c is the carrier frequency. $h_l(t)$, $l = 1,2,\ldots, N_{SM}$ is the Rayleigh fading channel coefficient. $n(t) \sim CN(0, N_0)$ expresses a complex Gaussian random process and its variance is $N_0/2$ per dimension.

Because the *IQ*-components of (1) have a similar structure, the signal model of the proposed system can be rewritten in the terms of only *I*-component. Thus, at the receiver after the perfect carrier estimation and sapling of the baseband signal, the l^{th} noisy chip signal received by r^{th} receive antenna can be expressed as follows:

$$r_{j,r}^{l} = x_I w_{j_I} h_{r,\ell} + n_{j,r}^{l}, \quad (2)$$

where, $r = 1,2,\ldots, N_r$ and $l = 1,2,\ldots, L$. j denotes the code indices of the spreading code. In order to simplify the presentation, the *I* parameter specifying the *I*-channel is dropped from *r* and *n*.

As shown by the receiver of the EDAS/COAS-CIM-SM scheme in Figure 1b, after the despreading operation at the receiver terminal for each *IQ*-components, each of the branches is used to estimate the spreading code indices, the active antenna indices,

and the transmitted symbol sequence, i.e., $(\hat{j}_I, \hat{j}_Q, \hat{\ell}, \hat{x}_I, \hat{x}_Q)$ Here, to reduce the complexity of the EDAS/COAS-CIM-SM system, detection of $(\hat{\ell}, \hat{x}_I, \hat{x}_Q)$ parameters will be performed by the EDAS/COAS based SM detector after the estimation of Walsh Hadamard Code indices $(\hat{j}_I, \hat{j}_Q)$ is detected. Therefore, the estimated $(\hat{j}_I, \hat{j}_Q)$ indices are fed back to the despreading vector set by using in the selection block diagram in the receiver, and then the $\mathbf{r}_{j_I}$ and $\mathbf{r}_{j_Q}$ despreading data associated with the (j_I, j_Q) are only applied to the input of the EDAS/COAS based SM detector. By this way, the complexity of the system is greatly reduced. For this reason, first, the spreading code indices are estimated from the sampled signals using correlator branches. To do this, the $\mathbf{r}_{j_I}$ is multiplied by the corresponding $\mathbf{w}_{j_I}$ spreading code in each branch and summed over the period $T_s = LT_c$. Thus, the despreaded output of the i^{th} correlator for *I*-component can be expressed as follows:

$$r_{i,r} = \sum_{l=1}^{L} w_{i,l} r_{j,r}^{l} = \sum_{l=1}^{L} w_{i,l}\left(x_I w_{j_I} h_{r,\ell} + n_{j,r}^{l}\right) = \begin{cases} E_w x_I h_{r,\ell} + \tilde{n}_{j,r}, & \text{if } i = j \\ \tilde{n}_{j,r}, & \text{if } i \neq j \end{cases} \tag{3}$$

where, E_w is the average energy transmitted per spreading code, and it is also expressed as $E_w = 1/\sqrt{L}\sum_{l=1}^{L} w_{j,l}^2$. $\tilde{n}_{j,r} = \sum_{l=1}^{L} w_{j,l}\, n_{jr}$ denotes the additive white Gaussian noise (AWGN) term multiplied by the Walsh Hadamard code. When the despreading operation is performed through all despreader, the resulting vector set at the receiver can be expressed with the help of (3) as follows:

$$\psi = \{\mathbf{r}_1, \mathbf{r}_2\}. \tag{4}$$

In order to estimate the indices of the spreading codes for *I*-component in the proposed system, first, the quadratic norm of the vectors $\psi = \left\{\| \mathbf{r}_i^I \|^2\right\}_{i=1}^{N_c}$ in the set of ψ is taken, and then, the indices of the maximum element of the squared norm vectors in the sets are determined. Since the Walsh Hadamard Codes are orthogonal to each other, the largest-valued element of the normed vector is also equal to the element over the same indices. From this point forth, the indices of the maximum elements of the normed vector sets for the *IQ*-components is determined as follows:

$$\hat{j}_I = \text{argmax}\ \{\| \psi^I \|^2\}, = \text{argmax}\ \left\{\| \mathbf{r}_1^I \|^2, \| \mathbf{r}_2^I \|^2\right\} \tag{5}$$

$$\hat{j}_Q = \text{argmax}\ \{\| \psi^Q \|^2\}, = \text{argmax}\ \left\{\| \mathbf{r}_1^Q \|^2, \| \mathbf{r}_2^Q \|^2\right\}. \tag{6}$$

Once j_I, j_Q are obtained by the spreading code index detectors, EDAS/COAS based SM detector will try all of the combinations of the (ℓ, x_I) over the despreaded signals $\mathbf{r}_{j_I}$ with j_I indices to obtain the estimations of $(\hat{\ell}, \hat{x}_I)$. Since EDAS/COAS based antenna selection technique is used at the transmitter in the CIM-SM system, the detector performance for $(\hat{\ell}, \hat{x}_I)$ parameters is better than traditional SM. Thus, the maximum likelihood (ML) estimation of the (ℓ, x_I) parameters for the *I*-component of the proposed EDAS/COAS-CIM-SM system can be defined as follows:

$$\left[\hat{\ell}, \hat{x}_I\right] = \underset{\substack{\ell \in A = \{1,2,\ldots,N_{SM}\} \\ X_I \in \{-1,+1\}}}{\text{argmin}} \left\{\| \mathbf{r}_{j_I}^I - E_w x_I \mathbf{h}_\ell \|^2\right\}, \tag{7}$$

where the vector $\mathbf{h}_l$ with the size of $N_r \times 1$ is the l^{th} column of the **H** channel matrix. The rows of the **H** convey the information of the receiving antenna index of the receiver while the columns of the **H** carry the information of the active antenna index of the transmitter. The **H** can also be written as $\mathbf{H} = [\mathbf{h}_1, \mathbf{h}_2, \ldots, \mathbf{h}_{N_{SM}}]$.

The other hand, as also shown in Figure 1b, to reduce the complexity of the receiver $\hat{\ell}$ detected in the *I*-channel branch is used for the *Q*-channel. Therefore, the ML estimation for x_Q symbol can be expressed as follows:

$$\hat{x}_I = \underset{X_Q \in \{-1,+1\}}{\text{argmin}} \left\{\left\| \mathbf{r}_{j_Q}^Q - E_w x_Q \mathbf{h}_{\hat{\ell}} \right\|^2\right\}, \tag{8}$$

Finally, with the bit-back matching technique using the detected $(\hat{j}_I, \hat{j}_Q, \hat{\ell}, \hat{x}_I, \hat{x}_Q)$ values, the originally transmitted bit sequence $\hat{\mathbf{b}}$ is reconstructed at the receiver with help of the demapper as shown in the receiver of the EDAS/COAS-CIM-SM system.

EDAS/COAS Based Spatial Modulation for CIM-SM System

In this section, EDAS and COAS based SM for CIM-SM system will be presented. As seen in recent studies, antenna selection based wireless communication techniques for MIMO system improves system performance greatly. In these systems, information bits are transmitted through the best antenna related for the channel with the best conditions.

Euclidean Distance optimized Antenna Selection (EDAS) Based SM

In the traditional SM technique, the information bits are firstly divided into blocks of $\log_2(N_t M)$. Then, $\log_2(N_t M)$ bits are divided into $\log_2(N_t)$ and $\log_2(M)$ bits of sub-sequence. Thus, while the $\log_2(M)$ bits selects the modulated symbol from the *M*-PSK signal set, on the other hand, $\log_2(N_t)$ bits select the l^{th} transmission antenna out of N_t. Thus, antennas having good or bad channel conditions will also be activated. From this perspective, in the EDAS or COAS based SM technique, SM scheme is not performed on all the antennas of the transmitting terminal. For example, when considering the EDAS technique on the transmitter, only the number of N_{SM} out of N_t transmit antennas will be used for SM technique. To do this, firstly, the set $\wp$ of enumerations of all possible $n = \binom{N_t}{N_{SM}}$ combinations of selecting N_{SM} out of N_t transmit antennas will be determined. Then, the best combinations of the set are selected. Later, the SM scheme is performed over these selected antennas

of the set. Therefore, the transmission data rate is now $\log_2(N_{SM}M)$ bits. For example, if $N_{SM} = 2$ transmit antennas out of the $N_t = 4$ are selected, the $\wp$ set has $n = \binom{4}{2} = 6$ elements and these are expressed as $\wp = \{[1,2], [1,3], [1,4], [2,3], [2,4], [3,4]\}$. Among $\binom{N_t}{N_{SM}}$ the possibilities, the specific transmit antenna set which maximizes the minimum Euclidean distance $d_{\min}(\mathbf{H}_x)$ among all possible transmit vectors is defined as follows [8]:

$$\chi_{ED} = \arg\max_{\chi\in\wp}\left\{\min_{\substack{\mathbf{x}_1,\mathbf{x}_2\in\Omega\\ \mathbf{x}_1\neq\mathbf{x}_2}} \| \mathbf{H}_\chi(\mathbf{x}_1-\mathbf{x}_2)\|^2\right\}, \quad (9)$$

where $\mathbf{H}_\chi \in \mathbb{C}^{N_r\times N_{SM}}$ has the number of N_{SM} columns determined by χ_{ED}. Ω is the set of all possible transmit vectors given by $\Omega = \{\mathbf{e}_\ell x_l\}_{\ell=1}^{N_{SM}}$, here, $x_l \in \{+1,-1\}$ and $\mathbf{e}_l$ presents a vector with size of $N_{SM}\times 1$ having 1 as the only non-zero element at the l^{th} location, and length of Ω is the $|\Omega| = N_{SM}M$. If $d_{\min}(\mathbf{H}x)$ is defined as $d_{\min}(\mathbf{H}_\chi) = \min_{\substack{\mathbf{x}_1,\mathbf{x}_2\in\Omega\\ \mathbf{x}_1\neq\mathbf{x}_2}} \| \mathbf{H}_\chi(\mathbf{x}_1-\mathbf{x}_2)\|^2$, (9) can be rewritten with respect to Euclidean distance as follow:

$$\chi_{ED} = \arg\max_{\chi\in\wp}\{d_{\min}(\mathbf{H}_\chi)\}. \quad (10)$$

Therefore, the system performance can be increased by maximizing $d_{\min}(\mathbf{H}_x)$. As a result, since the EDAS technique maximizes the $d_{\min}(\mathbf{H}_x)$, it improves the system performance compared to traditional SM, CIM-SM, CIM-SS schemes. Consequently, the performance of the EDAS-CIM-SM technique is greatly improved when the antenna set X_{ED} obtained in (5) is applied to SM technique.

Capacity Optimized Antenna Selection (COAS) Based SM

In the case where the channel state information and the signal-to-noise ratio (SNR) are known, the capacity of the SM scheme (C_{SM}) with the N_{SM} transmit antennas can be expressed as follows:

$$\beta \le C_{SM} \le \beta + \log_2(N_{SM}), \quad (11)$$

where is defined as $\beta = \frac{1}{N_{SM}}\sum_{\ell=1}^{N_{SM}} \log_2(1+\rho\|\mathbf{h}_\ell\|^2)$. It can easily be seen from (11) that in order to maximize the capacity of the SM (and thus CIM-SM), the β must be maximized. Therefore, the β can be maximized by selecting the N_{SM} antennas corresponding to the largest channel norms from the N_t transmission antennas. In accordance with these explanations, the set of antenna indices corresponding to N_{SM} largest channel norms out of N_t can be calculated in the receiver side, and then, the transmitter is notified back. From this perspective, the COAS based antenna set can be expressed as follows [8]:

$$\chi_{CO} = \{q_1, q_2, \dots, q_{N_{SM}}\}, \quad (12)$$

The order of χ_{CO} set is obtained according to the following conditions:

$$\|\mathbf{h}_{q_1}\|^2 > \|\mathbf{h}_{q_2}\|^2 > \dots > \|\mathbf{h}_{q_{N_{SM}}}\|^2 > \|\mathbf{h}_{q_{N_{SM}+1}}\|^2 > \dots > \|\mathbf{h}_{q_{N_t}}\|^2 \quad (13)$$

Finally, the performance of the COAS-CIM-SM technique is greatly improved when the antenna set χ_{CO} containing the $\mathbf{h}_{q1}, \mathbf{h}_{q2}, \dots, \mathbf{h}_{qN_{SM}}$ vectors are used for the SM technique.

Numerical Results

In this section, Monte Carlo based computer simulation results for the proposed EDAS/COAS-CIM-SM and other compared methods are presented for the *M*-PSK modulation over the Rayleigh fading channels. In the receiver side, the ML detection technique is performed to obtain the active antenna indices and the transmitted symbols. In order to estimate the spreading code indices of *IQ*-components, correlator method is used. SNR is defined as $\mathrm{SNR}(dB) = 10\log_{10}(E_b/N_0)$, here, $E_b = \frac{1}{p}\sum_{l=1}^{L}\left(\frac{w_{i,l}}{\sqrt{L}}\right)^2$ is the average bit energy and is the number of bits conveyed one symbol. Also, the spreading code is normalized with $\sqrt{L}$ for the transmission power to remain constant and $L = 16$. SM, EDAS-SM, COAS SM, CIM-SM, CIM-SS, and DS-SS techniques were used as reference comparisons for the simulation results.

BER performance curves of DS-SS with $N_t = 1$, 64-PSK; SM with $N_t = 4$, 16-PSK; CIM-SS with $N_t = 1$, 4-PSK, $N_c = 4$; CIM-SM with $N_t = 4$, BPSK, $N_c = 2$; COAS-SM with $N_t = 6$, $N_{SM} = 4$ 16-PSK; EDAS-SM with $N_t = 6$, $N_{SM} = 4$, 16-PSK; COAS-CIM-SM with $N_t = 6$, $N_{SM} = 4$,$N_c = 2$, BPSK; and EDAS-CIM-SM with $N_t = 6$, $N_{SM} = 4$, $N_c = 2$, BPSK techniques for $p = 6$ bits are depicted when the number of receiver antennas $N_r = 1$ for Figure 2 and $N_r = 4$ for Figure 3. The EDAS-CIM-SM, COAS-CIM-SM, and CIM-SM systems transmit 6 bits by 2 bits with antenna indices, 2 bits with spreading code indices, and 2 bits with BPSK symbol via *IQ*-components. The SM, COAS-SM, and EDAS-SM schemes convey 6 bits: 2 bits antenna indices and 4 bits with a 16-PSK modulated symbol. In the CIM-SS technique, 4 bits are carried in spreading code indices and 2 bits are conveyed with the 4-PSK modulated symbol. In the DS-SS scheme, all 6 bits are transmitted on a 64-PSK modulation. Considering Figure 2 and 3, it is seen that the proposed COAS-CIM-SM and EDAS-CIM-SM techniques have a considerable SNR gain compared to other methods.

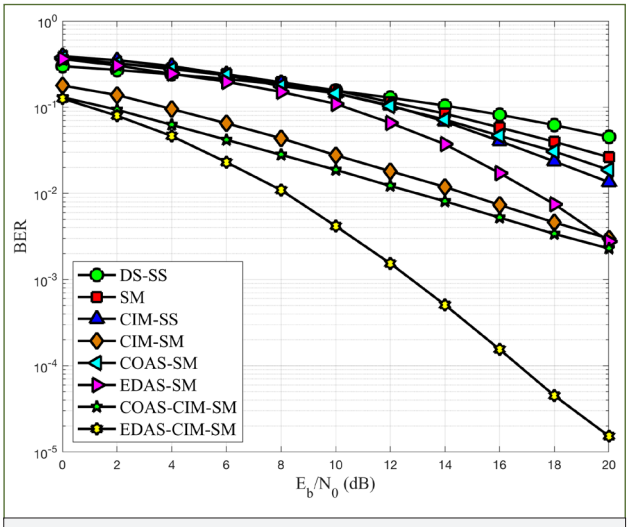

Figure 2. Performance comparison of DS-SS, SM, CIM-SS, CIM-SM, COAS-SM, EDAS-SM, COAS-CIM-SM and EDAS-CIM-SM systems for $N_r = 1$

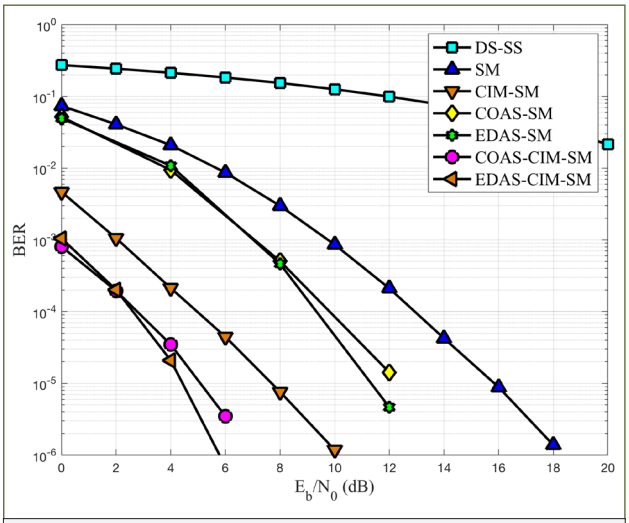

Figure 3. Performance comparison of DS-SS, SM, CIM-SS, CIM-SM, COAS-SM, EDAS-SM, COAS-CIM-SM and EDAS-CIM-SM systems for $N_r = 4$

Figure 4 represents the BER performance comparison curves of DS-SS with $N_t = 1$, 32-PSK; SM with $N_t = 2$, 16-PSK; CIM-SM with $N_t = 2$, BPSK, $N_c = 2$; COAS-SM with $N_t = 4$, $N_{SM} = 2$, 16-PSK; EDAS-SM with $N_t = 4$, $N_{SM} = 2$, 16-PSK; COAS-CIM-SM with $N_t = 4$, $N_{SM} = 2$, $N_c = 2$, BPSK; and EDAS-CIM-SM with $N_t = 4$, $N_{SM} = 2$, $N_c = 2$, BPSK techniques for $p = 5$ bits are illustrated when the number of receiver antennas $N_r = 2$.

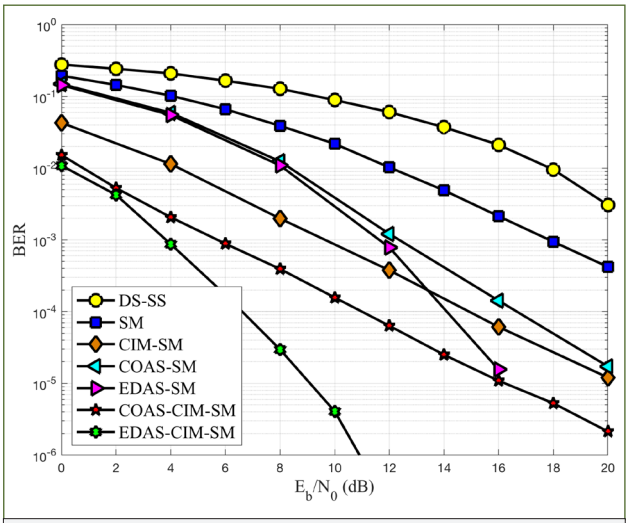

Figure 4. Performance comparison of DS-SS, SM, CIM-SM, COAS-SM, EDAS-SM, COAS-CIM-SM and EDAS-CIM-SM systems for $N_r = 2$

Finally, we can see in Figure 4 that our proposed techniques provide considerable SNR gains compared to other methods for the same number of bits per symbol.

Conclusion

In this paper, new Euclidian and capacity optimized antenna selection-based MIMO transmission systems with high energy efficiency, high data rate and better error performance, called EDAS-CIM-SM and COAS-CIM-SM, is proposed by combining EDAS, COAS, CIM, and SM techniques which are promising in 5G and beyond communication systems. It is shown via computer simulations that the proposed systems perform data transmission at a higher rate, consumes less transmission energy, and also has better spectral efficiency and performance than the DS-SS, CIM-SS, SM, CIM-SM, EDAS-SM and COAS-SM techniques.

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RESEARCH ARTICLE

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Array Antenna Feeding Network Design for 5G MIMO Applications

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ABSTRACT

Emerging smart antenna systems require different beam patterns of multiple antennas. Although adjustable phase shifters are mostly used in continuous-beam systems, the Butler matrix is used in switching-beam systems due to its low cost and easy fabrication. In this study, an antenna-array-feeding circuit based on the Butler matrix that can be used for Multiple Input Multiple Output applications is designed for 5G new radio. With the proposed switching system, the control of four beams can be achieved. The Butler circuit, designed to cover the 3.5–4.2 GHz 5G band, has a low complexity and is capable of meeting the need for high data throughput. A simulation of the circuit and circuit sub-elements designed using a 0.508-mm-thick substrate material is performed using the Computer Simulation Technology Microwave Studio computer-aided design tool. Furthermore, a prototype of the Butler circuit is fabricated, and the amplitude and phase variations at the output ports are measured. An average transmission loss of the feed circuit is measured as 1.5 dB, and when the length of the Phase Shifter in the circuit is set to λ/8, with a four-element linear array added to the output of the Butler circuit, the main beam is steered to ±15o and ±35o having maximum gain in the 6.39–8.77 dBi range.

Keywords: 5G, antenna array, Butler circuit, MIMO, Vivaldi

Introduction

Wide bandwidths are critical in modern wireless communication applications. Today, communication systems such as LTE need broadband operation for a high data rate transmission. Broadband LTE consists of multiple narrow-band signals. Multiple input–multiple output (MIMO) systems have recently been used in modern wireless systems. These systems use the spatial diversity technique consisting of multiple transmitter and receiver antennas. With this technique, the channel fading effects are minimized, and the channel capacity is increased [1-2].

The transition from 4G to 5G mobile network is expected to occur in the next 10 years [3, 4]. Due to constantly increasing network speed and capacity requirements, research has been conducted in many countries to implement the 5G wireless broadband technology. The wide range of services, frequencies, and application areas make 5G new radio precious. In addition to low and high frequencies, medium frequencies (1 GHz–6 GHz) are planned to be used as well. Within this band, the 3.5–4.2 GHz range is defined as the new radio 5G medium band, and it includes both licensed and unlicensed frequency bands.

Multi-beam antennas help to improve the transmission quality and increase the channel capacity by reducing the interference and multi-path fading in wireless communication systems. The beam-shaping techniques that provide unique beams for beam switching or beam steering have become an indispensable element of intelligent antenna systems. The Blass [5, 6], Nolen [7, 8], and Butler matrices [9, 10] are analog solutions that generate multiple beams by selecting input excitation. Among them, the Butler matrix is a widely used beam former for the antenna array applications, such as multi-beam antenna systems. Butler circuits have been used in many beam-switching array systems due to their simple design, low cost, and easy fabrication [11-14]. The size of branch-line couplers in the Butler circuit makes its incorporation with monolithic mi-

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crowave integrated circuits complicated and expensive. To overcome the size disadvantage of branch-line coupler, a number of approaches have been proposed [15-17].

In this paper, an antenna-array-feeding network based on the Butler matrix is designed for MIMO applications of 5G new radio. The Butler matrix is used to shape the beam in a phased array antenna system. *N* beams are generated by feeding *N* antennas with a Butler network having an *N* input–*N* output. Since 90° hybrid couplers are used in the Butler network, complexity increases with an increase in the number of beams. Therefore, the most commonly used structure to obtain an acceptable beam scanning angle is 4×4 Butler network. It is possible to direct the main beam to ±45° and ±15° by placing radiating elements with a half-wavelength distance. It is also possible to direct the beam to a different angular direction by controlling input phases and distance between the elements. The spatial resolution can be improved by increasing the number of beams. For this, a higher order Butler matrix should be used (N=8, 16, . . .). However, an increase in the degree of the Butler matrix will lead to a higher power loss. Moreover, the requirement of extra crossover elements in the network will make the design difficult.

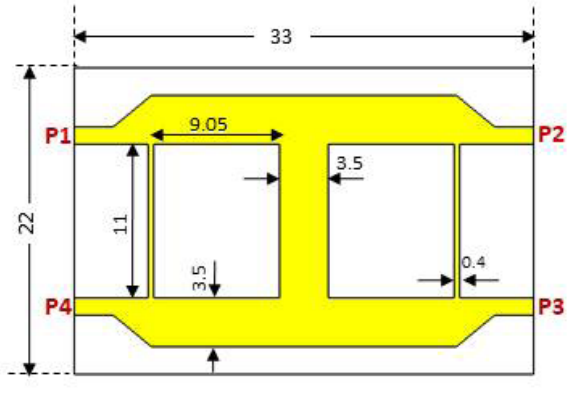

Figure 1. Wideband 3 dB hybrid coupler

The Butler circuit, designed to operate in the 3.5–4.2 GHz 5G band, is capable of meeting the need for high data throughput [18]. In this study, a wideband 4×4 Butler circuit is designed for medium frequencies of 5G new radio. In Section 2, the designed Butler circuit and structures used in the circuit are introduced. Simulation results of wideband hybrid coupler and crossover elements are also given in this section. All simulations are performed using the CST Microwave Studio (CST GmbH, Darmstadt, Germany.), a computer-aided design tool using a finite-integration technique. The measurement results of the designed circuit are given in Section 3. In Section 4, the beam-steering capability of the Butler circuit is demonstrated with an application example based on a four-element linear antenna array.

Butler Matrix Design

The 4×4 Butler matrix consists of two wideband crossover, four wideband 3 dB hybrid couplers, and four phase shifters. Rogers 3003 with a thickness of 0.508 mm and a dielectric constant of ε_r =3 is used as substrate material. The conductive material on both sides of the dielectric is copper with a thickness of 17 µm. In the design of the Butler circuit, microstrip transmission line is used. Input and output ports of the circuit are designed to be compatible with 50 .

Performance of the Butler matrix is directly related with the performance of the elements it contains. Thus, the simulation and optimization of each circuit element was made separately and then combined. The CST Microwave Studio was used for the optimization of the designed structures.

Wideband Hybrid Coupler Design

The coupler is the most important circuit element in the Butler circuit since there are four in the circuit and by cascading two of them, a crossover is formed. The bandwidth of a 90° hybrid coupler can be increased by using two-section branch-line technique instead of the standard coupler architecture [19].

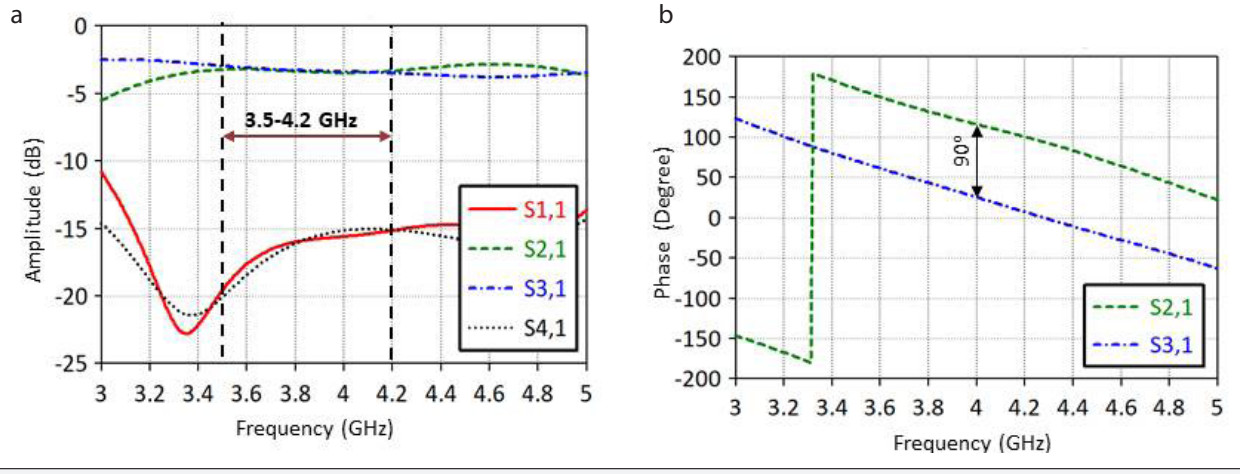

Figure 2. a, b. S-parameters of the hybrid coupler: (a) amplitude response and (b) phase response

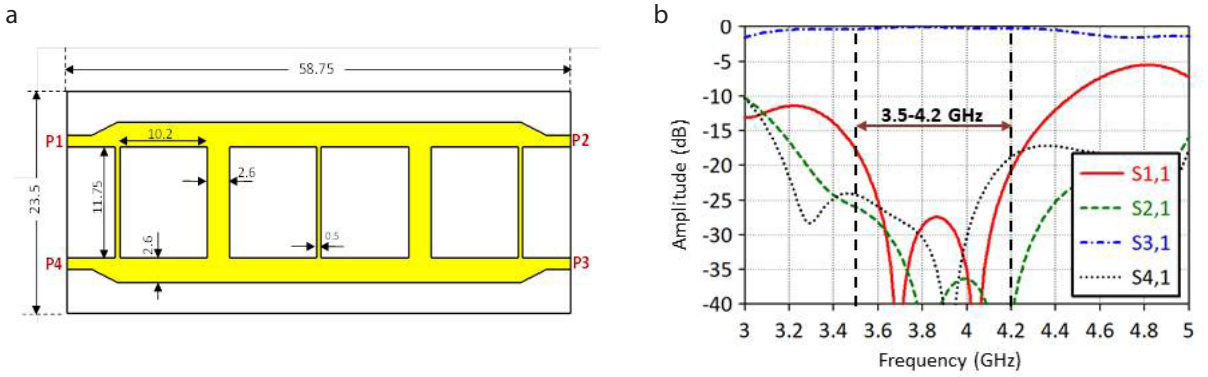

Figure 3. a, b. Wideband crossover: (a) top view and (b) amplitude response

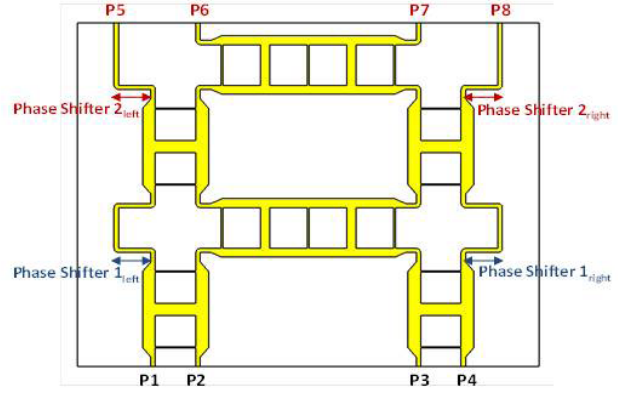

Figure 4. Wideband Butler matrix

Figure 1 is top view of the wideband 3 dB hybrid coupler designed for 5G medium frequencies. All dimensions are indicated on the figure. All units are in millimeters.

The strip width is set to 1.24 mm at the input–output ports to be compatible with 50Ω. Ports of the symmetrical four-port structure are shown in Figure 1. While the narrow-band hybrid coupler contains λ/4 transmission lines, line lengths obtained as a result of optimization for broadband operation are given in the figure. The width of the side lines are determined to have $Z_o/\sqrt{2} = 35\Omega$ characteristic impedance. For the transition, lines with $2Z_o 2^{1/4} = 118\,\Omega$ characteristic impedance are used at sides, and 35Ω is used in the middle. The amplitude and phase response of S-parameters obtained when the circuit is fed through Port 1 is given in Figure 2. Due to the symmetrical structure of the circuit, results obtained from other ports are not shared.

In the 3.5–4.2 GHz band, power is divided evenly between the second and third port. The coupling parameter is approximately 3dB throughout the entire band. The isolation at the forth port and return loss at the first port are below 15 dB. Figure 2b shows that the phase difference between the output ports (Ports 2 and 3) is 90°.

Wideband Crossover

A wideband crossover can be achieved by combining two wideband couplers [20]. A crossover is used at the intersection points to prevent combination of the signals. Thus, the main function of the crossover is to allow the signal flow to the transversal port and ensure isolation with adjacent ports. A wideband crossover structure was formed by combining the broadband 3 dB coupler introduced in Section 2.1. The crossover circuit is shown in Figure 3.a. The variation of S-parameters is given in Figure 3.b. It can be seen that the isolation between Port 1 and Port 2 is below 25 dB, and the isolation between Port 1 and Port 4 is below 18 dB. Furthermore, the coupling ratio between transverse ports (Port 1 and Port 3) is close to 0 dB throughout the entire band.

Wideband Butler Matrix Design

The 4x4 Butler circuit, which is formed by the use of four wideband hybrid power dividers, four phase shifters, and two wideband crossovers, is given in Figure 4. Phases of the output ports can be controlled by the use of two phase shifters (Phase Shifter 1_{left}, Phase Shifter 1_{right}). In addition, positions and phases of the antenna array elements can be adjusted by the length of 50 transmission lines, leading to output ports (Phase Shifter 2_{left}, Phase Shifter 2_{right}).

Figure 5.a shows the amplitude variation of the S-parameters for the wideband Butler circuit. The variation of output phases for the case when Phase Shifter 1_{left}=Phase Shifter 1_{right}=λ/4 is demonstrated in Figure 5.b. When the circuit is fed from Port 1, the isolation between Port 1 and other input ports (Ports 2–4) is below 14 dB, and the coupling between Port 1 and output ports (Ports 4–8) is approximately 6 dB (±1.5 dB). Thus, the Butler circuit divides the transmitted input power to approximately four. Output phases vary linearly with frequency. Output phases can be controlled by using the phase shifters generated by transmission lines.

Measurement Results

To measure the amplitude and phase response of the Butler circuit, a prototype is fabricated with the LPKF ProtoMat H100

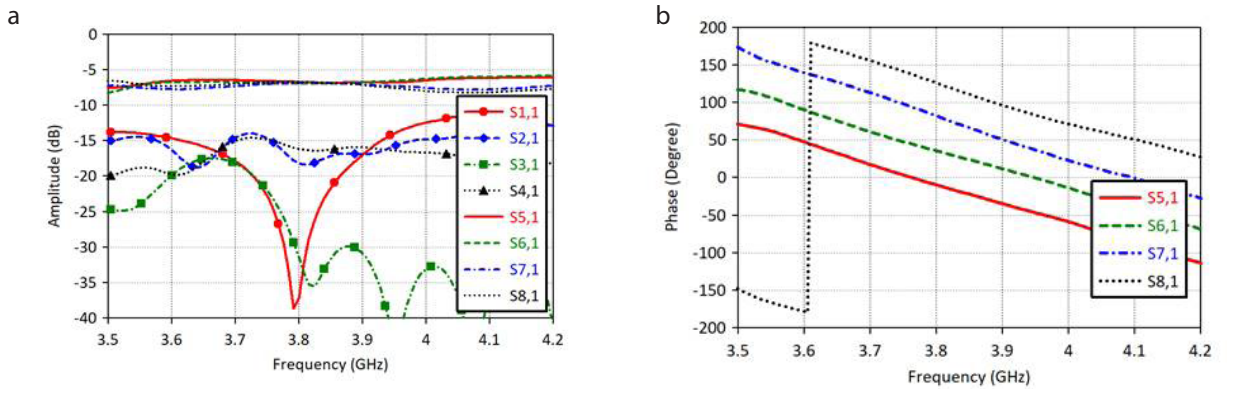

Figure 5. a, b. S-parameters of the Butler matrix fed from Port 1: (a) reflection coefficient from the input ports and coupling at the output ports, and (b) output phase variation example

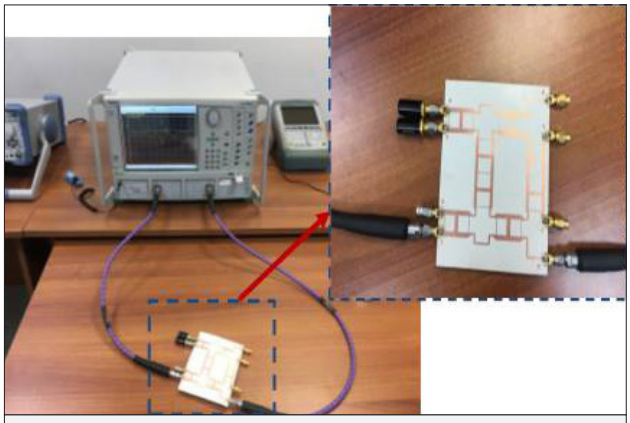

Figure 6. Wideband Butler matrix circuit measurement setup

printed circuit board production machine. The measurement setup is shown in Figure 6. An expanded view of the fabricated prototype is given in the inset. A SubMiniature version A (SMA) connector compatible with impedance is soldered to each port. S-parameters of the antenna are measured with the Anritsu vector network analyzer. During measurement, coaxial cables from the analyzer are connected to the two ports to be measured, while all other ports are terminated with matched loads to avoid reflection. Figure 7 shows return loss at the input ports and coupling at the output ports. Since the simulation results were given in the previous section, they are not shared with measurement results to prevent complexity. Due to the symmetrical structure of the circuit, similar results are obtained by feeding the circuit from Port 1 and Port 4. Also, it is the case for Port 2 and Port 3. Thus, only the results obtained when the circuit is fed from Port 1 and Port 2 are included in Figure 7. The similarity between simulation and measurement results can be observed by comparing Figure 5 and 7.

An Application Example: Vivaldi Array Fed by Butler Circuit

In this section, an application example for the use of the Butler circuit for beam steering will be demonstrated. A four-element linear antenna array will be placed to the output ports of the Butler circuit, and the main beam of the array will be steered to different angular directions with the excitation of input ports. For this purpose, a modified version of the commonly used Vivaldi antenna is used. A Vivaldi antenna is preferred due to its complete planar geometry and the possibility to feed it with a microstrip line.

Modified Vivaldi Antenna Design

The Vivaldi antenna is a widely used ultra-wideband antenna that has many practically applications. Due to its planar structure, it can be easily integrated with ultra-wideband sensor circuits. It has an almost symmetrical radiation pattern in E- and H-planes. Theoretically, due to its exponentially tapered slotted structure, the Vivaldi antenna has unlimited bandwidth. However, in practice, it has a limited band as a result of its physical constraints, such as the expansion rate of the slot, the slot line width, and the transition from the feed line.

A well-known disadvantage of a classic Vivaldi antenna is its reduced directivity at low frequencies. By increasing the aperture size of the antenna, a better impedance matching and effective radiation can be achieved at low frequencies. Another solution is adding slots with varying lengths to increase the aperture of the antenna [21, 22]. The corrugated profile formed by adding slots to the two sides of the exponentially tapering provides a better characteristic (high gain, wider band) compared to the Vivaldi antenna, especially in microwave imaging applications [23]. For these reasons, a modified Vivaldi antenna with rectangular slots of varying lengths was used instead of a standard Vivaldi antenna.

The proposed Vivaldi antenna consists of a microstrip feed line, microstrip line to slot line transition, and the radiating structure. It is designed to operate as a receiver and transmitter in the 3.5 GHz–12 GHz (1: 3.4 bandwidth) frequency band. The slot curve of the Vivaldi antenna is an exponential function expressed by

$$S(z) = (W_{slot}/2)e^{az}, \quad (1)$$

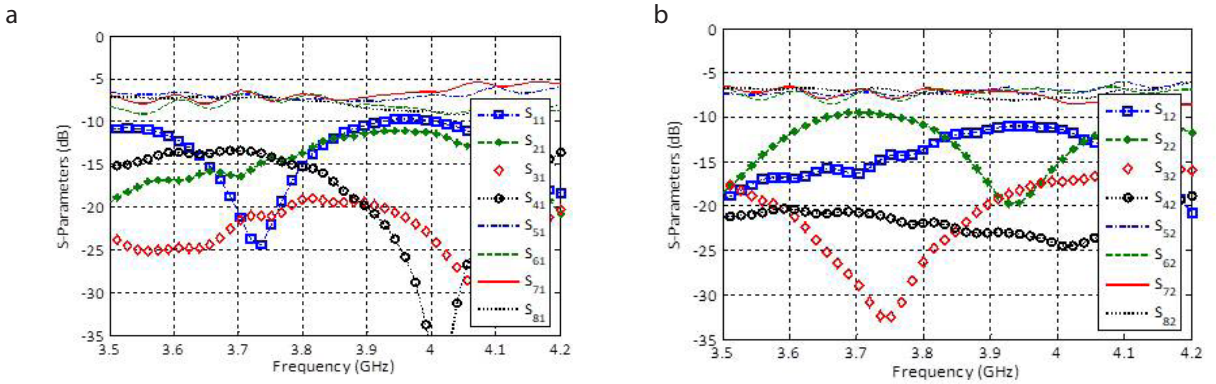

Figure 7. a, b. Measured S-parameters of the Butler matrix: (a) Port 1 as the input port and (b) Port 2 as the input port

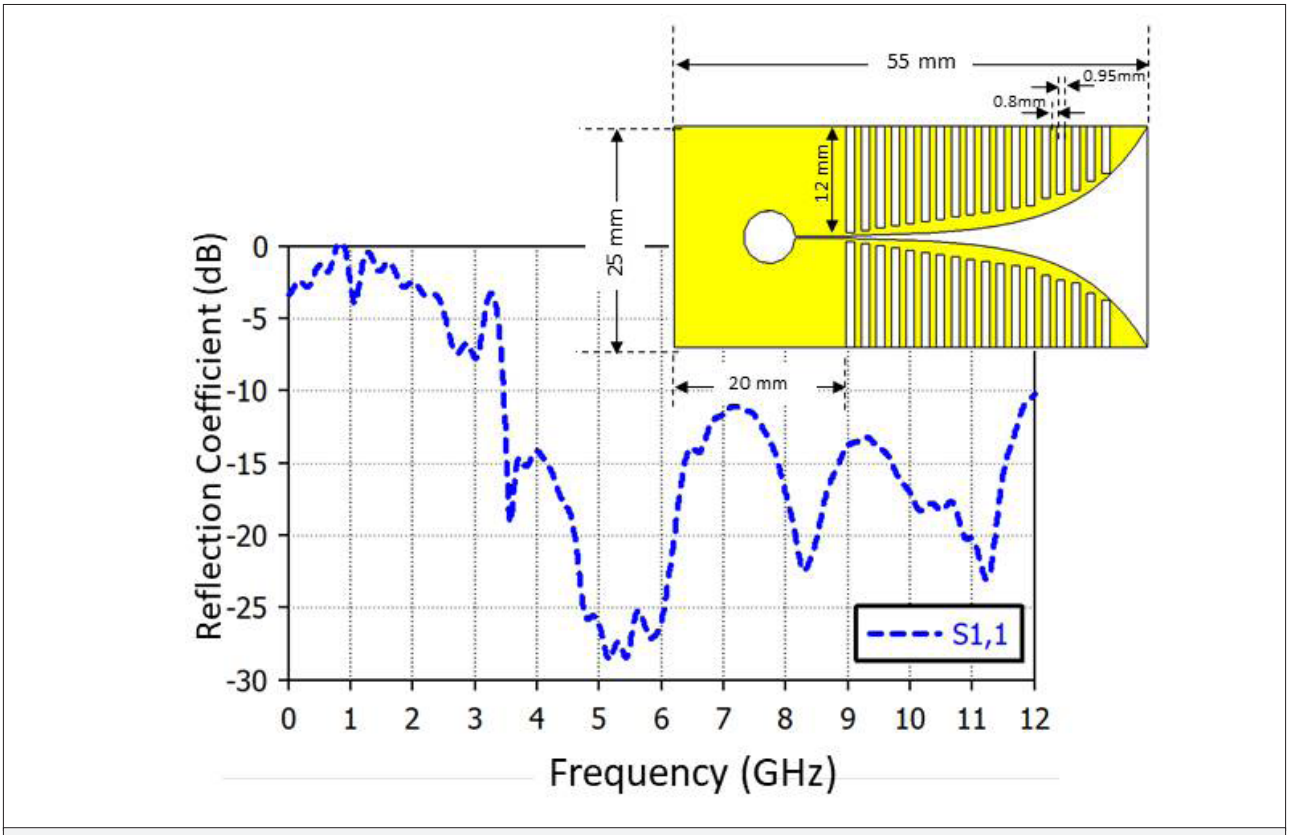

Figure 8. Reflection coefficient variation of the corrugated Vivaldi antenna

where α=0.165 and W_{slot}=0.25*mm*. A quarter wavelength open circuit stub is used for wideband matching.

The size of the Vivaldi antenna is 25mmx55mm. The design uses the Rogers 3003 laminate (ε_r =3) with 0.508 mm substrate and 17 µm copper. The distance between the rectangular slots, the width of the slots, and the length of the slots are also shown on the antenna. The distance between the slots and the width of the slots remain the same, whereas the length of the slots decreases toward the aperture. In simulations, it was observed that an increase in the number of slots changes the direction of the current at the edges and cause extra resonance. Slots at the edges act as a resistive load and contribute to the radiation by directing the wave to the slot line region. This improves the radiation characteristics of the Vivaldi.

The reflection behavior of the corrugated Vivaldi antenna is expressed in terms of S11. Figure 8 shows the variation of the reflection coefficient with frequency. Return loss is less than 10 dB in the frequency range 3.5 GHz–12 GHz. The frequency band of the antenna includes the 3.5–4.2 GHz band for the 5G

medium frequencies. The structure of the modified Vivaldi antenna is shown in Figure 8 together with its dimensions as the inset. The change in the gain of the antenna within this band is 0.2 dB. The gain pattern in E- and H-planes at the center frequency (max. gain, 6.1 dBi) is shown in Figure 9.

Four-Element Vivaldi Array Fed by the Butler Matrix

Since the Butler circuit is an ideal feeding network for beam-switched array systems [11-14], it is designed for 5G medium frequencies as a feeding network for the four-element linear corrugated Vivaldi array. The distance between the elements is 25, 60, and 25 mm, respectively. The transmission line at the output ports of the Butler circuit is in the microstrip form resulting in an uncomplicated connection with the Vivaldi antenna feed. Both the Vivaldi antenna and the Butler circuit use Rogers 3003 with 0.508 mm thickness. The ports are compatible with 50Ω. In Fig. 10, the four-element Vivaldi array with the Butler feeding network is shown. The outer dimensions of the circuit are 135 mm×155 mm.

Figure 11 shows the normalized radiation patterns of the corrugated Vivaldi array at 3.75 GHz obtained by excitation of different input ports. Since the beam steering is at $\phi = 90^o$ plane, only E-plane patterns are demonstrated. Asymmetry in the patterns is due to the balun used for impedance matching in the corrugated Vivaldi. Table 1 lists performance parameters of the radiation patterns. When the radiation patterns are observed, it can be seen that the main beam is steered to $\theta \cong +15^0$ and -15^0 and by the excitation of Ports 1 and 4, respectively and main beam is steered to and $\theta \cong +35^0$ and -35^0 by excitation of Ports 2 and 3, respectively. Considering the 3dB beam widths of the patterns given in Table 1, it can be concluded that with a four-element corrugated Vivaldi array fed by the proposed Butler circuit, half of the semi-sphere ($-45^o \leq \theta \leq 45^o$) is scanned with a maximum gain of the pattern varying between 6.39 and 8.77 dBi.

Table 1. Performance parameters of the corrugated Vivaldi array fed by the proposed Butler circuit

Excitation Port	Main Beam Direction (o)	Gain (dBi)	Directivity (dB)	3 dB Beam-width (o)
P1	15	8.5	9.13	23.2
P2	35	6.86	7.47	27
P3	35	6.39	7.02	26
P4	15	8.77	9.39	23.1

Conclusion

MIMO systems with more than one user require a system that can create multiple beams in different directions. The Butler circuit is one of the most commonly used circuits for beam steering. In this work, a wideband Butler circuit compatible with planar geometry is introduced for beam-switching circuits to control the main beam direction. A 4×4 Butler circuit is designed for MIMO applications operating in 5G new radio me-

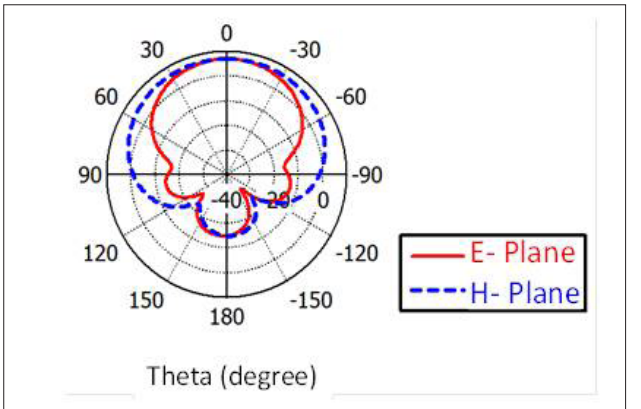

Figure 9. E- and H-plane patterns of the corrugated Vivaldi antenna at 3.75 GHz

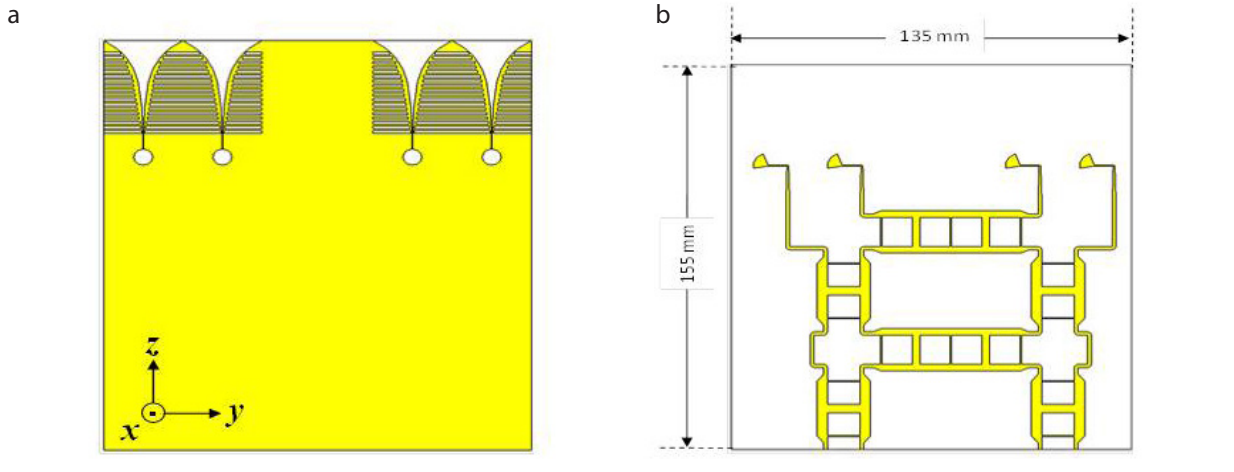

Figure 10. a, b. Four-element corrugated Vivaldi array fed by the Butler matrix: (a) top view and (b) bottom view

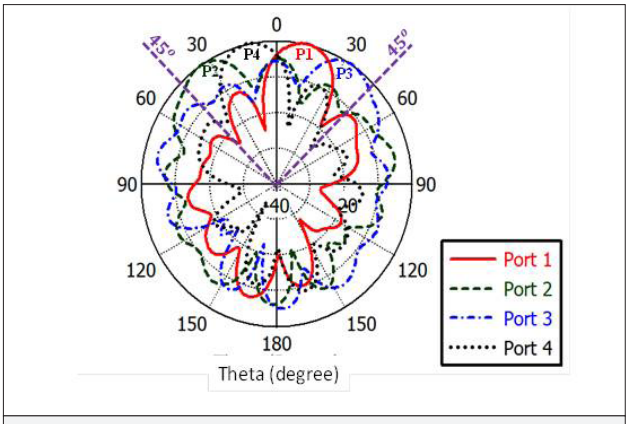

Figure 11. E-plane normalized radiation pattern of a four-element corrugated Vivaldi array fed by the Butler matrix

dium frequencies and is simulated with a full-wave simulation tool. Simulation results showed the amplitudes between -6 dB and -8 dB at the outputs of the Butler circuit. Output phases of the Butler circuit can be controlled by the use of phase shifters for beam steering. The Butler circuit is fabricated and measured. The measurement results show similarity with the simulation results. In addition, with an application example on the usage of Butler circuit as the feed network of a four-element linear array, the beam-steering capability of the designed circuit is demonstrated.

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ISTANBUL UNIVERSITY CERRAHPASA

RESEARCH ARTICLE

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A New FGMOS UCCII and SIMO Type Universal Filter Application

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ABSTRACT

A new floating gate MOS (FGMOS) universal current conveyor (UCCII) is proposed to have the properties of simplifier circuit topology, simpler signal processing and wider input swing. Since the FGMOS transistors are used in the proposed UCCII circuit, the number of transistors is reduced and the topology of the circuit is simplified because it is easier to get arithmetic operations in circuits by using FGMOS transistors when compared to conventional MOS transistors. At the same time, using FGMOS differential amplifier structure in the input stage of the FGMOS UCCII circuit increased the input signal swing resulting both an increase in the linearity of the circuit and an improvement in the voltage following properties. A single input multi output (SIMO) type universal filter application is given to show the versatility of the UCCII block. Both the proposed FGMOS UCCII circuit and filter circuit are simulated with SPICE program by using 0.35µm technology parameters. When the simulation results are analyzed it is seen that that the FGMOS UCCII circuit reached the expected improvements according to the MOS equivalent circuit and expected to be used in linearly tunable filters.
Keywords: FGMOS, UCCII, analog, wide range

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Introduction

There has always been a need for differential signals in low-power low-voltage design and designing a circuit for differential signals has enabled versatile applications. So many application examples like filter topologies, multipliers, oscillators are presented in literature [1-4] employing the differential extensions of the second generation current conveyor (CCII) structure. In fact CCII in analog circuit design is very advantageous as a circuit block. Many efficient applications can be made by taking the basic building block of CCII element. In the case of differential input applied circuits, there is a feature that weakens the CCII element, which is a single input node with a high impedance value. The use of multiple CCIIs to solve this problem has been presented as a solution [1]. Another solution is to create more complex CCII structures with differential inputs based on the CCII structure.

Floating Gate MOS (FGMOS) transistors have been used in analog circuit designs in an exciting way in recent years [5-8]. Since FGMOS transistors are widely used in digital circuits, they are already available in standard CMOS technology. For this reason, FGMOS transistors are used by analog designers in more applications nowadays. As a result, FGMOS transistors are used not only in digital circuits but also in analog circuit design. For this purpose, considering the benefits of the FGMOS transistor in voltage following characteristics in current conveyors, the universal current carrier (UCCII), which is designed by taking into account the advantages such as simpler circuit topology in differential current conveyors, has been proposed by using FGMOS transistors.

Universal current carrier structure can be considered as a single circuit block incorporating all current conveyor structures designed like the dual output current conveyor (DOCCII) and differential voltage current conveyor (DVCCII) since the first and second generation current conveyors. In this paper, a new FGMOS UCCII is proposed having the properties of simplifier circuit topology, sim-

pler signal processing and wider input swing. Since the FGMOS transistors are used in the proposed UCCII circuit, the number of transistors is reduced and the topology of the circuit is simplified because it is easier to get arithmetic operations in circuits by using FGMOS transistors when compared to conventional MOS transistors. At the same time, using FGMOS differential amplifier structure in the input stage of the FGMOS UCCII circuit increased the input signal swing resulting both an increase in the linearity of the circuit and an improvement in the voltage following properties. A SIMO type universal filter application is given to show the versatility of the UCCII block. Both the proposed FGMOS UCCII circuit and filter circuit are simulated with SPICE by using 0.35µm technology parameters. When the simulation results are analyzed it is seen that that the FGMOS UCCII circuit reached the expected improvements according to the MOS equivalent circuit and expected to be used in linearly tunable filters.

Rest of the paper is divided into several sections. In the second section, general characteristics of FGMOS transistor are mentioned. In the third section, structure and operation of the proposed FGMOS UCCII circuit is explained. In the fourth and fifth sections, SPICE simulation results of the proposed circuit and filter application are presented, respectively. The last section is conclusion.

FGMOS Transistors

The FGMOS transistor is formed by isolating electrically the gate of a standard MOS transistor at the production stage and by placing multiple inputs on this isolated passage (FG) without any resistive connections. Although there are capacitive connections between the multiple inputs and FG, there is no resistive transition. Since FG is completely surrounded by high resistive material, it is a floating node in terms of dc operating point [5]. The equivalent schematic and equivalent circuit for an n-input n-channel FGMOS transistor are given in Figure 1 and Figure 2, respectively.

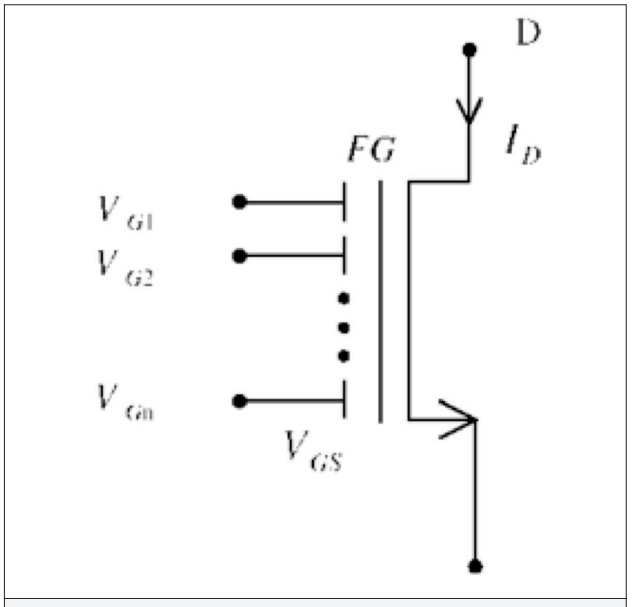

Figure 1. Diagram of a n-input n-channel FGMOS transistor

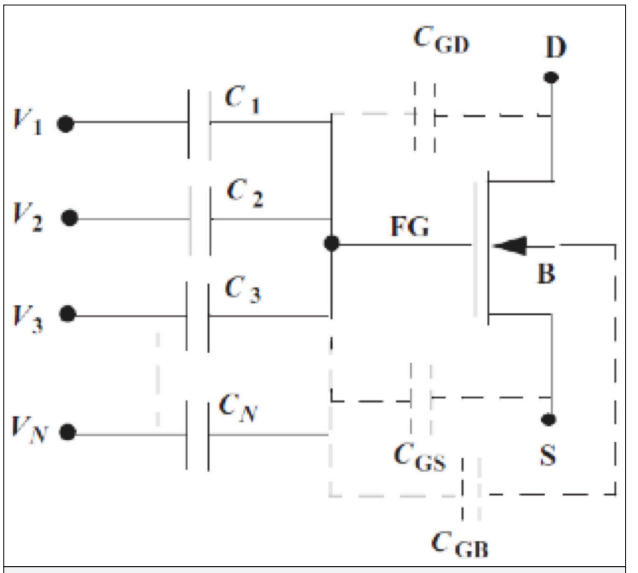

Figure 2. Equivalent circuit of a *n*-input *n*-channel FGMOS transistor

Since the voltages applied to the multiple inputs are capacitively connected to the FG, they control the voltage in the floating gate and tune the current flowing through the MOS transistor channel. The voltage at the FG is given by:

$$V_{FG} = \frac{C_{FGD}V_D + C_{FGS}V_S + C_{FGB}V_B + \sum C_i V_i}{C_T} \quad (1)$$

$$C_T = C_{FGD} + C_{FGS} + C_{FGB} + \sum_{i=1}^{n} C_i \quad (2)$$

The terms V_{FG}, V_D, V_S and V_B in the equations are the floating gate voltage, drain voltage, source voltage and bulk voltage, respectively. C_i are input capacitances where i changes from 1 to n which corresponds the number of multiple inputs. C_{GB}, C_{GS} and C_{GD} are the parasitic capacitances related to bulk, source and drain respectively; and C_T is the sum of C_{GB}, C_{GS}, C_{GD} and C_i.

$$C_i \gg C_{FGD}, C_{FGS}, C_{FGB} \quad (3)$$

Parasitic capacitances are much smaller than the input ones in general and in accordance with the technique in [9], negligible terms of the equation are excluded and gate voltage is equal to the total weight of the input voltages according to the input capacitor values.

Proposed Circuit Description

Universal current carrier is characterized by three high-impedance input terminals (Y_1, Y_2, Y_3), one low-impedance node (X) and four high-impedance output nodes (Z_1, Z_2, Z_1' and Z_2'). Its block scheme is given in Figure 3 and matrix characteristics are summarized in Eq.4.

$$\begin{bmatrix} V_X \\ I_{Y1} \\ I_{Y2} \\ I_{Y3} \\ I_{Z1} \\ I_{Z2} \\ I_{\overline{Z1}} \\ I_{\overline{Z2}} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & -1 & 0 & 0 & 0 & 0 \end{bmatrix} \begin{bmatrix} V_{Y1} \\ V_{Y2} \\ V_{Y3} \\ I_X \\ V_{Z1} \\ V_{Z2} \\ V_{\overline{Z1}} \\ V_{\overline{Z2}} \end{bmatrix} \quad (4)$$

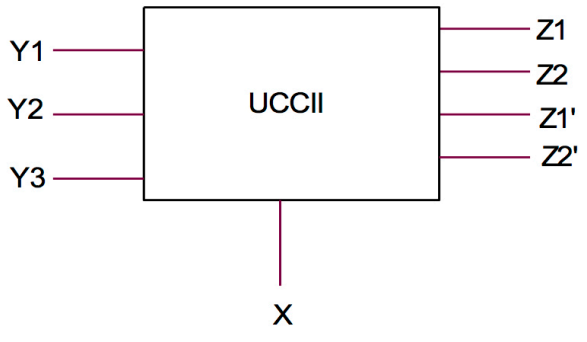

Figure 3. UCCII block representation

Figure 4 shows how UCCII can be obtained from the CCII basic block [1]. In fact, the UCCII structure is similar to the DVCCII structure. An additional Y-node and Z-nodes were added to the structure. In order to obtain other CCII structures from this structure, conjugates of Z nodes were also added to the structure. For example, the classical CCII+ structure can be obtained by taking the Y_1 terminal as the Y node and the Z_1 terminal by the Z node. In addition to other existing CCII structures, some new topologies can also be obtained through this circuit block.

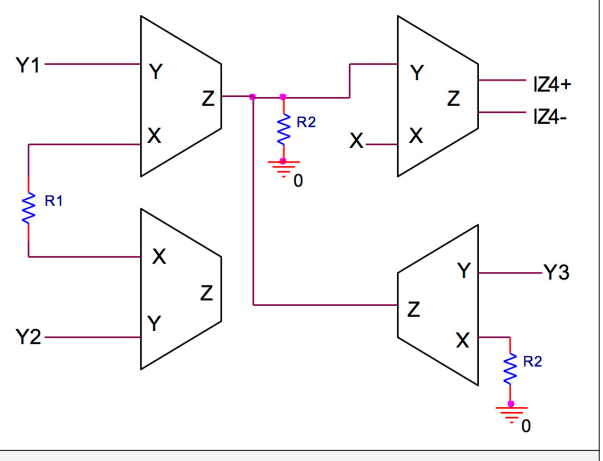

Figure 4. Obtaining UCCII using CCII block

As can be seen in Figure 4;

$$V_X = V_{X4} = V_{Y4} = R_2(I_{Z1} + I_{Z3}) = \frac{R_2(V_{X1}-V_{X2})}{R_1} + \frac{R_2 V_{X3}}{R_3} = \frac{R_2(V_{Y1}-V_{Y2})}{R_1} + \frac{R_2 V_{Y3}}{R_3} \quad (5)$$

If all resistances are chosen equal, then below equation is taken.

$$V_X = V_{Y1} - V_{Y2} + V_{Y3} \quad (6)$$

The proposed FGMOS UCCII circuit is given in Figure 5. As shown in the figure, the differential input stage is constructed with two FGMOS transistors in the proposed circuit. The arithmetic relation between the V_X and $V_{Y1,2,3}$ voltages in the structure is based on the principle of equalizing the current flowing from the FGMOS transistors. For the FGMOS transistors, if the currents are equal, the weighted sum of the voltages applied to the inputs of the FGMOS transistors will be equal. Equal selection of the C_i capacitors connecting the inputs to the floating gate, in other words the FGMOS transistors being the matched transistors, are provided. By providing this feature, $V_{Y1} + V_{Y3} = V_X + V_{Y2}$ equation is obtained between the V_X and $V_{Y1,2,3}$ voltages applied to the inputs of the FGMOS transistors. By adjusting this equation, finally $V_X = V_{Y1}$-$V_{Y2} + V_{Y3}$ is obtained.

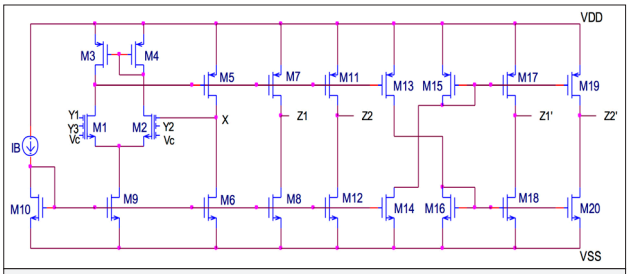

Figure 5. Proposed FGMOS UCCII circuit

Floating Gate MOS transistors in differential pairs have three inputs which are applied through equal sized capacitors, Ci. The input signals of V_{Y1}, V_{Y2}, V_{Y3} and the control voltage V_C are applied to one of the floating gates in the differential pairs. Since the voltage at the gate is less than the input voltage the differential pair transistors can work in saturation even when large signals are applied. This leads to increase the input dynamic swing.

Determining parameters of voltage and current conveying properties are the slopes of related transistors and it is achieved easily by choosing matched transistors.

The parasitic resistances seen at the X and Z terminals and the capacitors seen from the Y terminals (since the R_Y component is very large) can be expressed as follows:

$$R_X = \frac{2}{\frac{C_i}{C_T} g_{m2}\left[g_{m5}\left(g_{ds1}+\frac{C_{GD}}{C_T}g_{m1}+g_{ds3}\right)^{-1} // r_{o6}\right]} \quad (7)$$

$$R_{Z1} = r_{o7}//r_{o8},\ R_{Z2} = r_{o11}//r_{o12},\ R_{Z1'} = r_{o17}//r_{o18},\ R_{Z2'} = r_{o19}//r_{o20} \quad (8)$$

$$C_Y = \frac{2}{3}(WLC_{OX}) \quad (9)$$

Simulation Results

The proposed FGMOS UCCII structure has been simulated in the SPICE program with 0.35 µm TSMC technology parameters. Supply voltage is taken as ± 1.5V while V_C voltage is taken as control voltage. The bias current is chosen as I_B = 125µA. The dimensions of the n-type transistors are taken as W / L = 2.1

µm / 0.7 µm and the p-type transistors are taken as W / L = 10.5 µm / 0.7 µm. The C_{FGD} and C_{FGS} capacitor values are calculated as 0.6fF and 5fF and the input capacitor values are chosen as C_i = 50fF. The compensation capacitor of 20fF is applied between the drain and gate terminals of the M7 and M11 transistors.

Figure 6-8 show the DC voltage transfer characteristics of the proposed circuit with respect to $V_{Y1, Y2, Y3}$ input DC voltages. DC voltage $V_{Y1, Y2, Y3}$ is swept between -1.5V and 1.5V while the DC voltage V_X is plotted. In Figure 6-8 while V_{Yi} is -1.5V, V_X takes -1.5V, 1.43V and -1.49V, respectively. While V_{Yi} is 1.5V, V_X takes 1.41V, -1.49V and 1.4V, respectively. As it is seen from these values, input swing is almost equal to the supply voltages.

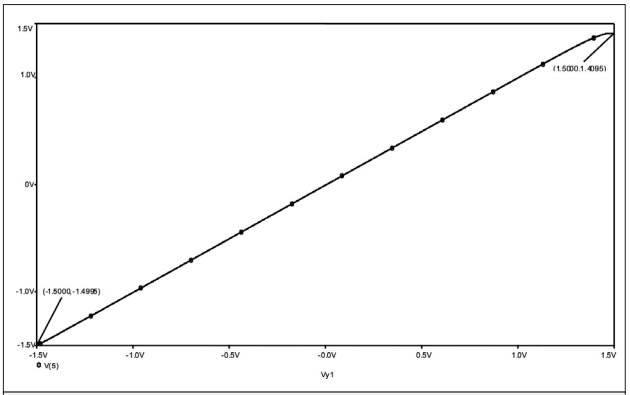

Figure 6. FGMOS UCCII DC voltage transfer characteristics (V_X-V_{Y1})

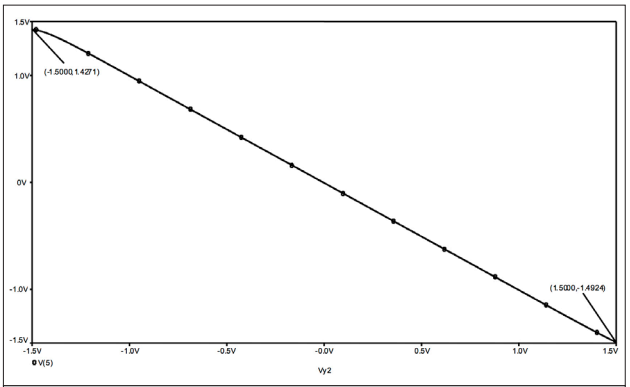

Figure 7. FGMOS UCCII DC voltage transfer characteristics (V_X-V_{Y2})

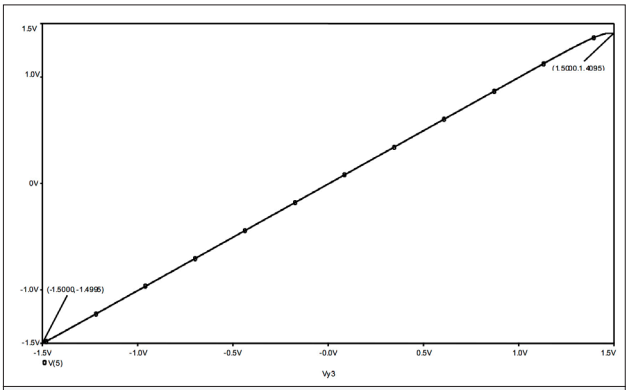

Figure 8. FGMOS UCCII DC voltage transfer characteristics (V_X-V_{Y3})

Figure 9 shows the DC current transfer characteristics of the FGMOS UCCII structure. As can be seen from the figure, the I_X current was swept between -10µA and 10µA while the DC output currents I_{Z1}, I_{Z2}, $I_{Z1'}$ and $I_{Z2'}$ currents are plotted. Between the input and output currents $I_X = I_{Z1} = I_{Z2}$ and $-I_X = I_{Z1'} = I_{Z2'}$ relations are obtained.

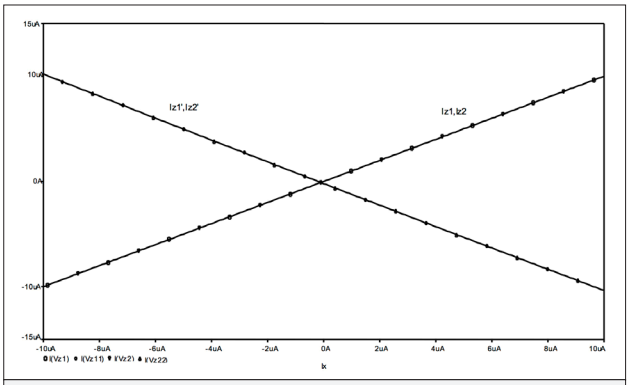

Figure 9. FGMOS UCCII DC current transfer characteristics

Figure 10 shows the AC voltage transfer characteristics of the FGMOS UCCII structure. In the AC voltage transfer characteristics, the 3dB frequency value is approximately 200MHz for V_{Y1}, V_{Y3} and 350MHz for V_{Y2}.

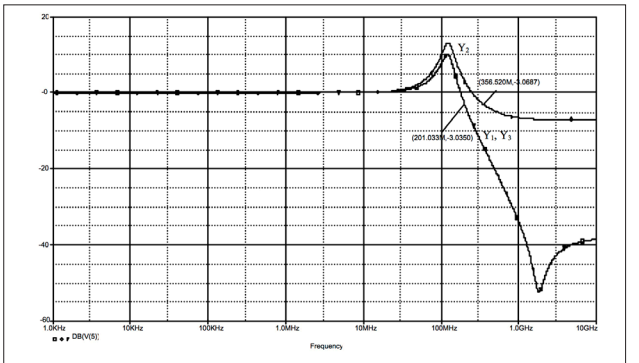

Figure 10. FGMOS UCCII AC voltage transfer characteristics (V_X-$V_{Y1,2,3}$)

Figure 11 shows the AC current transfer characteristics of the FGMOS UCCII structure. In the AC current transfer characteristics, the 3dB frequency value is approximately 340MHz.

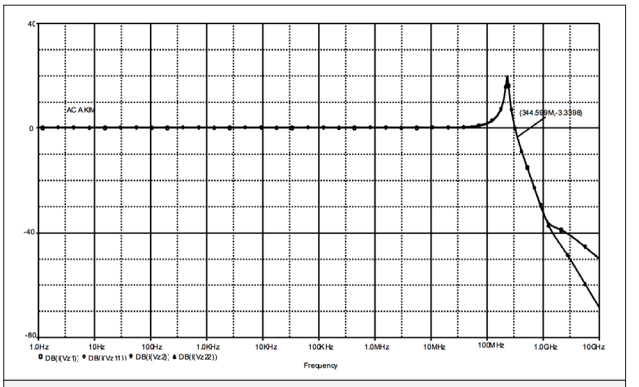

Figure 11. FGMOS FDCCII AC current transfer characteristics (I_X-$I_{Z1,2,1',2'}$)

When UCCII structure is formed by conventional MOS transistors, 31 transistors are used except for bias current [10]. When this structure is examined, it is seen that 6 transistors are used in the input stage to obtain $V_X = V_{Y1} - V_{Y2} + V_{Y3}$ correlation between X and Y nodes. In the proposed FGMOS UCCII structure, a total of 20 transistors, including bias current, are used. At this point, the number of transistors is reduced to three by using FGMOS transistors at the input stage which provides the correlation between the X and Y nodes in order to take advantage of the simplicity of providing arithmetic operations. Also the voltage following characteristics of the UCCII structure are improved with the linearity improvement of the FGMOS differential amplifier. It is known that the input swing of differential amplifier is increased by a factor of C_T / C_i by using FGMOS transistors instead of conventional MOS transistors [11, 12]. In addition, new Y terminals can be added by only increasing the number of input terminals of the FGMOS transistors used, without adding a new transistor to the UCCII structure. This shows the flexibility of using FGMOS transistors in circuit blocks with arithmetic operations.

The performance criteria obtained by the SPICE simulation program of the proposed FGMOS UCCII structure is summarized in Table 1.

Table 1. FGMOS and MOS UCCII circuits performance criteria

	FGMOS UCCII	MOS UCCII [10]
Supply voltage	±1.5V	±3V
Bias current	125μA	300μA
Input linearity swing (V_X-V_{Y1}, V_X-V_{Y3})	(-1.5V, 1.38V)	NA
Input linearity swing (V_X-V_{Y2})	(-1.49V, 1.4V)	NA
Maximum input signal (@THD=%5)	±1.36V	NA
Parasitic resistance (X, Y, Z)	405Ω, 14GΩ, 114kΩ	4mΩ (X)
-3dB bandwidth (V_X/V_{Y1}, V_X/V_{Y2}, V_X/V_{Y3})	280MHz, 436MHz, 280MHz	64MHz
-3dB bandwidth (I_Z/I_X)	180MHz	73.5MHz

FGMOS: Floating Gate MOS; UCCII: Universal Current Conveyor

SIMO Type Universal Filter Application

One input multi-output filter structure obtained using the FGMOS UCCII circuit is given in Figure 12 [13]. The structure consists of three UCCII and four passive elements. All passive elements are grounded, which gives an advantage for the integrated circuit design.

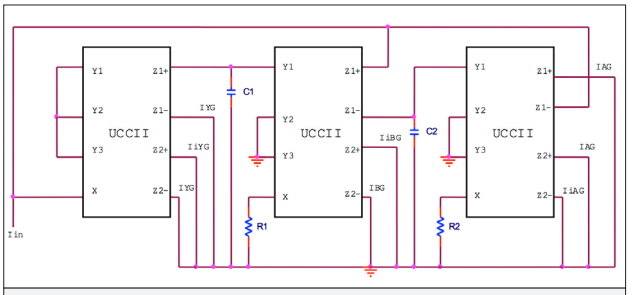

Figure 12. One input multi-output filter structure obtained using FGMOS UCCII circuit

The transfer functions of the filter structure are as follows.

$$\frac{I_{LP}}{I_{in}} = \frac{-I_{iLP}}{I_{in}} = \frac{1}{1+sC_2R_2+s^2R_1R_2C_1C_2} \quad (10)$$

$$\frac{I_{BP}}{I_{in}} = \frac{-I_{iBP}}{I_{in}} = \frac{sC_2R_2}{1+sC_2R_2+s^2R_1R_2C_1C_2} \quad (11)$$

$$\frac{I_{HP}}{I_{in}} = \frac{-I_{iHP}}{I_{in}} = \frac{s^2R_1R_2C_1C_2}{1+sC_2R_2+s^2R_1R_2C_1C_2} \quad (12)$$

The angular cut-off frequency and the quality factor are the same for all filters and are as follows.

$$\omega_0 = \frac{1}{\sqrt{R_1R_2C_1C_2}} \quad (13)$$

$$Q_0 = \sqrt{\frac{R_1C_1}{R_2C_2}} \quad (14)$$

Figure 13 shows the output curves of one input multi-output filter structure using the UCCII structure. In order to obtain f_0 = 1MHz, Q = 1 / √2 at the curves shown in Figure 13 according to equation (13), R_1, R_2, C_1 and C_2 are chosen as R_1 = 22kΩ, R_2 = 44kΩ and $C_1 = C_2$ = 5pF.

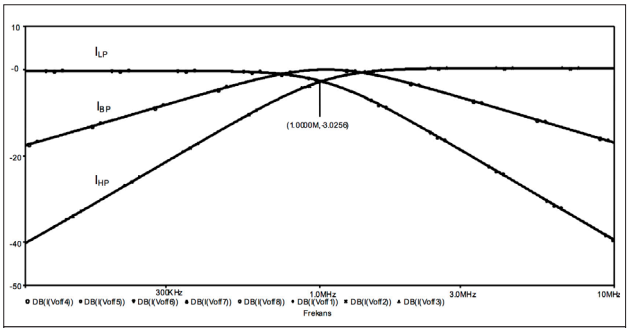

Figure 13. Output curves of one input multiple output filter structure performed with the FGMOS UCCII circuit

In order to examine the large signal behavior of one input multi-output filter structure obtained with FGMOS UCCII, an input signal of 1MHz sinusoidal with 200μA peak-to-peak amplitude is applied and the output currents are examined. The resulting output curves are shown in Figure 14.

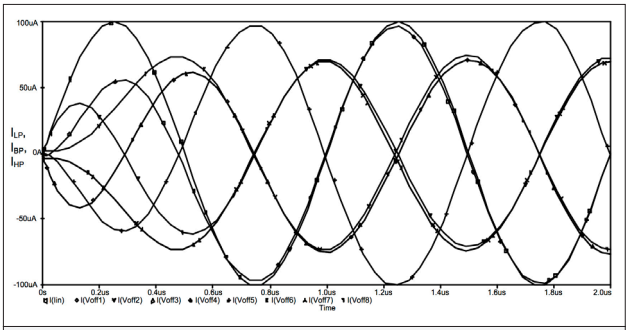

Figure 14. Large signal behavior of one input multi-output filter structure performed with the FGMOS UCCII circuit

Conclusion

Since the FGMOS transistors are used in the proposed UCCII circuit, the number of transistors is reduced and the topology of the circuit is simplified because it is easier to get arithmetic operations in circuits by using FGMOS transistors when compared to conventional MOS transistors. At the same time, using FGMOS differential amplifier structure in the input stage of the FGMOS UCCII circuit increased the input signal swing resulting both an increase in the linearity of the circuit and an improvement in the voltage following properties. The FGMOS UCCII circuit is handled with the CMOS equivalent and the simulation results are given in a tabular form. When the results given are analyzed, it is seen that the FGMOS UCCII circuit reached the expected improvements according to the MOS equivalent circuit.

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ISTANBUL UNIVERSITY CERRAHPASA

RESEARCH ARTICLE

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An Effective Method for Islanding Detection Based on Variational Mode Decomposition

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ABSTRACT

The present study presents a new islanding detection method based on variational mode decomposition (VMD). In the method, the VMD transform of the voltage at point of common coupling is calculated, and then based on the decomposed modes, an islanding detection index for distinguishing between islanding and normal conditions will be derived. Pursuing this objective, the measured voltage is decomposed into four modes, and a new islanding detection index will be derived from their energy and their variations. Then, thresholds will be adjusted based on values of proposed index in various conditions on normal and islanding operations. The proposed algorithm decomposes the measured signal into a predetermined number of intrinsic modes around central frequencies; the method is insensitive to the noise and sampling frequency. To validate the method, a distribution network has been simulated in PSCAD/EMTDC, and the algorithm is tested on a variety of islanding and normal circumstances. The results illustrate desired performance of the proposed algorithm for conditions such as motor, nonlinear, and large load switching; as normal condition; and islanding condition with a variety of power mismatches between local load and distributed generation. The results demonstrate the desired performance of the method with respect to both speed and accuracy.

Keywords: Passive islanding detection, Variational mode decomposition, Energy modes, Threshold, Non-detection zone

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Introduction

Islanding phenomenon refers to an undesired event in distribution networks consisting of distributed generations (DGs), where the power is cut-off from the main network while DG continues to supply the load. In such a condition, the detached portion of the network, called the island, is possible to not meet the power quality index requirements, such as voltage and frequency. The phenomenon may lead to the destructive effect on the DG, as well as the network equipment. In this respect, the IEEE standard considers a 2-second limit to disconnect DG from the rest of the network when islanding occurs [1]. The islanding detection methods are generally classified into two main groups, local and remote, based on the side in which islanding is detected. Furthermore, the local methods are grouped into two classes as passive and active methods [2, 3]. The passive methods are exclusively based on the measurement of electrical parameters, such as voltage, current, and frequency at the point of common coupling (PCC) [4-6]. On the other hand, in the active methods, a disturbance signal is injected into the PCC so that it facilitates abnormalities detection at the point [7]. In remote islanding detection, a communication infrastructure is required to transfer data from DG to the remote site located on the main power system [2].

Since disturbance signal is not used in the passive methods, there would be no concern about power quality and network security issues. Unfortunately, the methods have non-detection zone (NDZ) in which detection schemes are unable to detect the islanding condition [1]. Technically, NDZs occur when resonant frequency of the local load is matched with the fundamental frequency of the power system [8]. In contrast, active islanding detection algorithms use a disturbance signal providing smaller NDZs; however, this benefit comes at the price of reduction of power quality, as well as installation of appropriate electronic devices.

Heretofore, a variety of passive methods are introduced for islanding detection. The most practiced methods are under voltage/over voltage (UV/OV) and under frequency/over frequency (UF/OF) procedures. In these methods, voltage and frequency variations caused by unbalanced active and reactive powers are employed for islanding detection [9-11]. Unfortunately, the methods are characterized with large NDZs. More sensitive techniques have been proposed to improve their detection abilities, such as phase jump [12], rate-of-change-of-frequency [13], and rate-of-change-of-reactive-power. These are featured with large detection errors. Different techniques, such as total harmonic distortion [14,15], power spectral density [7], and network harmonic impedance [5], also have wide NDZs. Moreover, advanced spectral analysis and filtering approaches, including those based on wavelet singular entropy [16], pattern recognition [17], data mining [18], and Bayesian classification [19], are proposed. In wavelet transform-based solutions, a number of decomposed levels are found by the trial-and-error method, and extracted features are highly sensitive to noise [1]. They also call for classification trainings using such artificial intelligence (AI) techniques as artificial neural networks and support vector machine, which has high computational complexity. Approaches based on S-transform have been proposed to avoid problems of wavelet-based methods in islanding detection [20-22]. Although these techniques have solved the noise problem in a sense, they still involved high processing needs and usage of AIs to distinguish between islanding and normal conditions.

The main part of the voltage signal contains more illustrative information about the events on the power line. The signal decomposition helps to discriminate between the noise/harmonics and the main signal. In the present study, a new islanding detection algorithm is proposed based on variational mode decomposition (VMD). The algorithm is non-recursive and decomposes the voltage signal into a predetermined number of intrinsic modes around central frequencies. It has only a few variables, does not need to determine the mother wavelet function, and is not sensitive to the noise and sampling frequency. In the present study, VMD is used to decompose the voltage into four modes, and then based on computing the energy of each individual mode, the new islanding index will be obtained.

The structure of the study is as follows. VMD is introduced briefly in section 2. The proposed algorithm is presented in section 3. The performance of the algorithm through computer simulation in PSCAD/EMTDC and MATLAB software is illustrated in section 4. Finally, the conclusion is given in section 5.

VMD transform

VMD transform decomposes a signal into a given number of constitutive intrinsic mode functions (IMFs). It is a non-recursive signal processing method, an upgraded version of Empirical Mode Decomposition (EMD), which eliminates EMD limits, such as sensitivity to noise and sampling frequency [23, 24]. In the frequency domain, bandwidth of a mode is spread and limited around a central frequency ω_k (Hz). In the time domain, it corresponds to an AM–FM modulated signal as follows:

$$u_k(t) = A_k(t)\cos \emptyset_k(t). \tag{1}$$

Here, the principle of signal decomposition is the compact bandwidth of IMFs, which will be derived using the following optimization problem [25]:

$$min\left\{\sum_k \left\|\partial_t\left[\left(\delta(t)+\frac{j}{\pi t}\right)*u_k(t)\right]exp^{-i\omega_k t}\right\|_2^2\right\} \tag{2}$$
$$s.t.\sum_k u_k = f(t).$$

Where k is the number of modes that main signal f must be composed to, and $\{u_1,\dots,u_k\}=\{u_k\}$ and$\{\omega_1,\dots,\omega_k\}=\{\omega_k\}$ are sets of all modes and central frequencies, respectively. To solve the problem, both quadratic penalty factors and Lagrange multipliers are used to obtain an unconstrained optimization problem as follows:

$$\mathcal{L}(\{u_k\},\{\omega_k\},\lambda) =$$
$$\alpha\sum_k\left\|\partial_t\left[\left(\delta(t)+\frac{j}{\pi t}\right)*u_k(t)\right]exp^{-i\omega_k t}\right\|_2^2+\left\|f(t)-\sum_k u_k(t)\right\|_2^2+\langle\lambda(t),f(t)-\sum_k u_k(t)\rangle. \tag{3}$$

Where α is the weighting parameter for constraints. The saddle point of augmented Lagrangian (L) must be found through sequentially iterative suboptimizations called alternative direction method of multipliers (ADMMs) to solve this minimization problem in Equation (2).

The algorithm of ADMM optimization concept for VMD is

Initialize $\left\{u_k^1\right\},\left\{\omega_k^1\right\},\lambda^1,n\leftarrow 0$

Repeat

$$n\leftarrow n+1$$

For k=1: K **do**

Update u_k

$$u_k^{n+1}\leftarrow arg_{u_k}min\mathcal{L}\left(\left\{u_{i<k}^{n+1}\right\},\left\{u_{i\geq k}^{n}\right\},\left\{\omega_i^n\right\},\lambda^n\right). \tag{4}$$

End for

For k=1: K **do**

Update ωk

$$\omega_k^{n+1}\leftarrow arg_{\omega_k}min\mathcal{L}\left(\left\{u_i^{n+1}\right\},\left\{\omega_{i<k}^{n+1}\right\},\left\{\omega_{i\geq k}^{n}\right\},\lambda^n\right). \tag{5}$$

End for

Dual ascent

$$\lambda^{n+1}\leftarrow\lambda^n+\tau\left(f-\sum_k u_k^{n+1}\right). \tag{6}$$

Until convergence: $$\sum_k\frac{\left\|u_k^{n+1}-u_k^n\right\|_2^2}{\left\|u_k^n\right\|_2^2}<\epsilon. \tag{7}$$

To update u_k, the first suboptimization in Equation (4) must be rewritten as the following minimization problem:

$$u_k^{n+1} = arg_{u_k \in X} min \left\{ \alpha \left\| \partial_t \left[\left(\delta(t) + \frac{j}{\pi t} \right) * u_k(t) \right] exp^{-j\omega_k t} \right\|_2^2 + \left\| f(t) - \sum_i u_i(t) + \frac{\lambda(t)}{2} \right\|_2^2 \right\}. \quad (8)$$

Then, applying Parseval/Plancherel Fourier isometry, variable changes, and Hermitian symmetry of real signal, the frequency spectrum of each individual mode can be obtained without difficulty. Accordingly, the filtered modes then must go through an inverse Fourier transform to obtain the corresponding time domain signals [25].

$$\hat{u}_k^{n+1}(\omega) = \frac{f(\omega) - \sum_{i \neq k} \hat{u}_i(\omega) + \frac{\lambda(\omega)}{2}}{1 + 2\alpha(\omega - \omega_k)^2} \quad (9)$$

To find the central frequencies, the subproblem in Equation (5) must be rewritten as the following minimization problem:

$$\omega_k^{n+1} = arg_{\omega_k} min \left\{ \left\| \partial_t \left[\left(\delta(t) + \frac{j}{\pi t} \right) * u_k(t) \right] exp^{-j\omega_k t} \right\|_2^2 \right\}, \quad (10)$$

which gives:

$$\omega_k^{n+1} = \frac{\int_0^\infty \omega |\hat{u}_k(\omega)|^2 d\omega}{\int_0^\infty |\hat{u}_k(\omega)|^2 d\omega}, \quad (11)$$

which locates each new ω_k at the gravitational center of each mode spectrum [25].

The proposed algorithm for islanding detection based on VMD

VMD is effective tool to extract feature of signals especially non-stationary ones. To derive the proposed algorithm, the given network is first simulated for various operational states existing in both normal and islanding situations. In the normal operation, different operational scenarios, including change in the network demand with respect to entrance/exit of inductive loads, induction motor starting, and nonlinear load, are applied, whereas in the islanding condition, such scenarios with different power mismatches between local load demand and DG generation are practiced.

An important stage in the classification of various phenomena is the choice of appropriate features. The selected features should have minimum computational burden and low dimension. These objectives are followed in the present study. In all scenarios, voltage at PCC is measured and decomposed into four different modes using VMD, and finally, energy of each mode is calculated as:

$$E(k) = \sum_{i=1}^{n} |V(k,n)|^2, \quad (12)$$

where V refers to decomposed modes of voltage (V), k to the kth mode, n to the number of samples, and E is a value in relation with energy (J). Second, a window of limited length, here 24 samples, is moved along the calculated energies (E) to derive the variation rate of each energy window. If present, the difference between steeps of two consecutive windows is called ΔE_k. Then, based on the exhaustive study of various operational conditions, the following islanding detection index is defined as:

$$IslIndx = \frac{\Delta E_1 * \Delta E_3}{E_4 * \Delta E_2}, \quad (13)$$

where ΔE_i, i , and E_4 are the variation rates of energy of decomposed modes and energy of fourth mode, respectively. An islanding index in the form of Equation (13) gives large thresholds, and therefore, higher reliability. To achieve more accurate and more reliable results, especially in the presence of strong noises and/or higher harmonic distortions, a number of modes can be increased sufficiently. Here, α=2000 and T=0 are assumed for the parameters of VMD, since in this proposed method only the modes whose central frequencies are close to the network operation frequency have considered noise effects substantially resolved. In addition, NDZ is more squeezed into a smaller area. These are the most significant strength points of this proposed algorithm.

The numerical results of the proposed islanding index demonstrate significant differences between islanding and normal

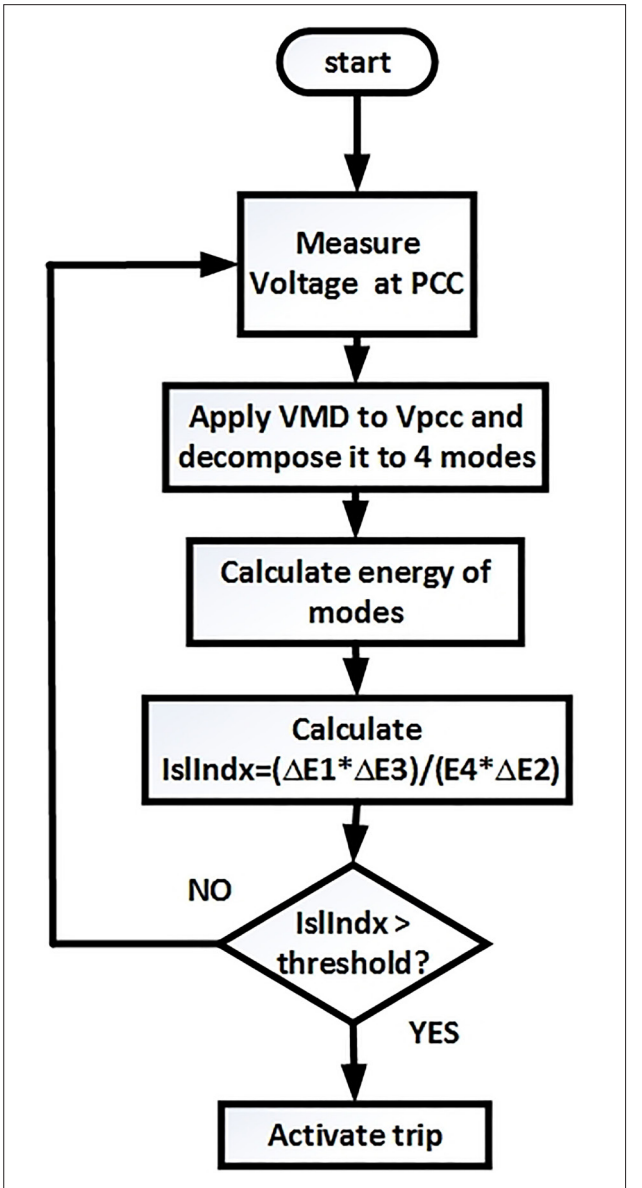

Figure 1. The proposed algorithm for islanding detection

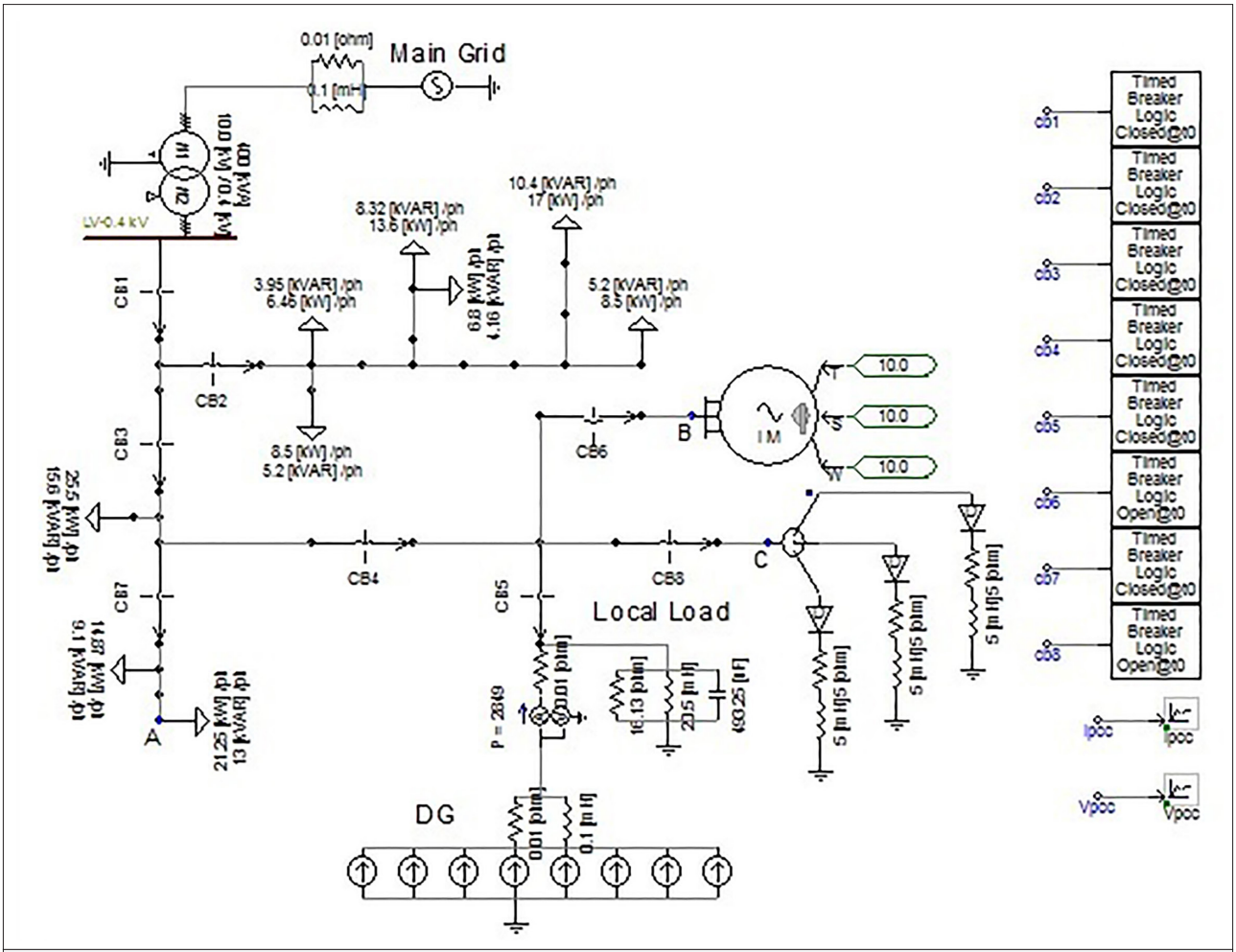

Figure 2. System configuration in PSCAD/EMTDC

conditions of the network. Thus, it can be used as a practical scale for islanding detection. The differences are meaningful, even for the worst-case scenario where DG's power is completely matched to that of its local load. Considering the worst-case results as a reference, one can adjust thresholds to be so small that the islanding detection is possible, even for the most load balanced states, and so large that no false alarm is produced during the normal operation of the network. Figure 1 illustrates the flowchart of the algorithm. In this figure, ΔE_i and i=1, 2, 3 are the changes of energy for modes 1, 2, 3, and E_4 indicates the energy of the 4th mode.

Simulation results

For the purpose of validity, a low voltage distribution network has been simulated within PSCAD/EMTDC software environments (Figure 2). The main side of the network is a feeder that receives power from a 10/0.4 kV transmission substation and delivers it to a commercial region with a variety of loads. A 3 KW inverter-based DG is connected to a branch of the feeder. Local load is an RLC load with R=16.13 Ω, L=20.5 mH, C=493.25 μF, and Q_f=2.5 (quality factor). System parameters are available in reference [6].

Six scenarios are studied to test the performance of the algorithm. In the first scenario, while the network is in the normal state, CB2 is opened at t=0.6 s, resulting in the reconfiguration and disconnection of a large load; however, the network still continues operation normally. In the second and third scenarios, CB4 and CB5 are opened, respectively, and islanding condition occurs. The second scenario encompasses a large imbalance of power, whereas the third scenario remains nearly in the balance condition. The fourth scenario deals with a 37 kVA induction motor at point B and t=0.4 s, for both adding to and removing from the network. In this case, the network remains at its normal state. In the fifth scenario, the proposed algorithm is tested and verified against nonlinear loads. Finally, in the last scenario, the effect of local load quality factor is investigated.

Normal condition with large load switching

When the system operates under normal condition, by the opening of CB2, a large load is removed from the system and creates a change in voltage and impedance seen from the DG viewpoint. Nonetheless, the algorithm performs correctly and produces no trip signal. Figure 3 and 4 depict the simulation results of this

scenario. Figure 3 shows the main voltage and its decomposed modes, in which there are minor changes at the moment of CB2 opening. Figure 4 shows the energy of the decomposed modes and the calculated index. As can be seen from Figure 4, this situation does not lead to activating a trip. According to the figures, when such a large load as 0.3pu is disconnected from the network (i.e., the worst case of load elimination in the present study), higher values must be selected for the threshold of islanding index.

Islanding condition with large power imbalance

Here, CB4 is opened, and an islanding occurs along with a large power imbalance between DG generation and island demand powers (Figure 5, 6). As it is obvious in Figure 5, there are significant changes in PCC voltage and its decomposed modes at 0.6s (islanding occurrence time), which result in considerable changes in their energies in Figure 6. Figure 6 shows higher value of calculated index than selected threshold (0.4), which could activate a trip (Figure 6). The results show that the trip signal is 10ms after islanding occurrence. Sensible changes in islanding index are apparent, and thus the algorithm decides properly. Similarly, openings of CB1 and CB3 result in islands and power imbalances and thus easily detectable.

Islanding condition with low power imbalance

In the worst case where CB5 is opened, the DG's generated power is matched exactly to the demand of the islanded area. In this case, UV/OV- and UF/OF-based methods are not able to detect the islanding phenomenon. However, the proposed algorithm is able to detect islanding occurrence. Figure 7 and 8 illustrate the results of simulation for a local load with a 2.5 quality factor. In addition, changes appear to be small in Figure 7, but there are differences that result in more changes in en-

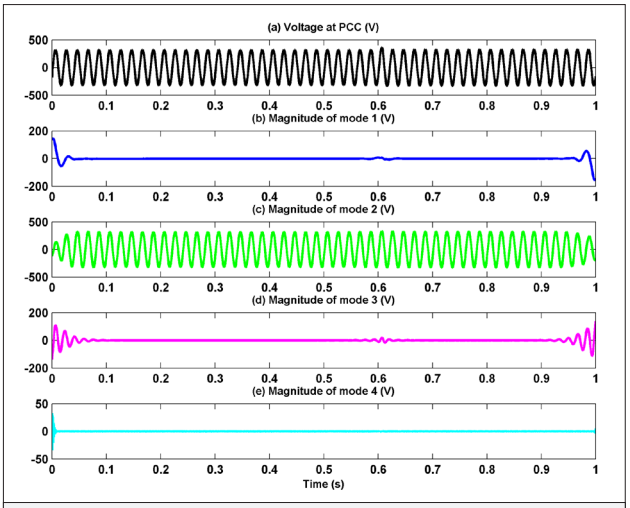

Figure 3. The voltage at PCC and the decomposed modes for large load switching

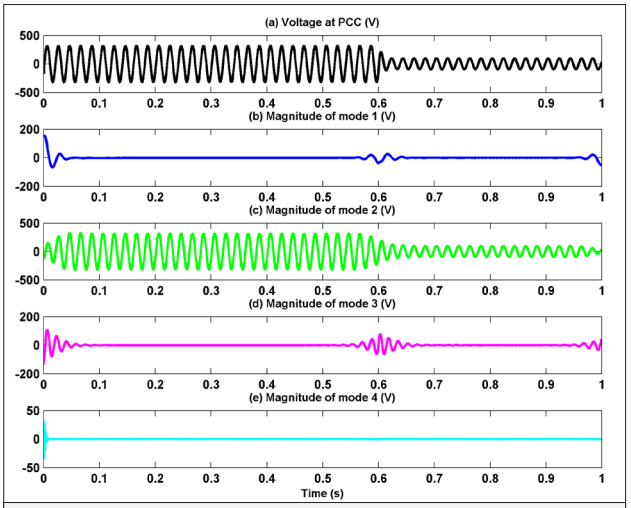

Figure 5. The voltage at PCC and the decomposed modes for large power imbalance

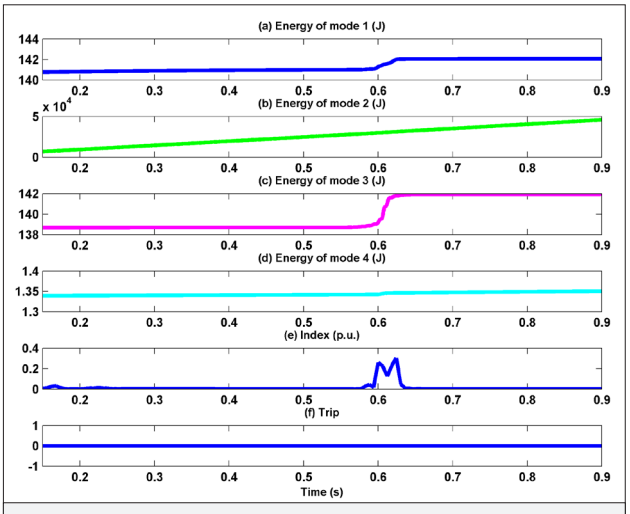

Figure 4. Change in energies of modes, proposed index, and trip signal for large load switching

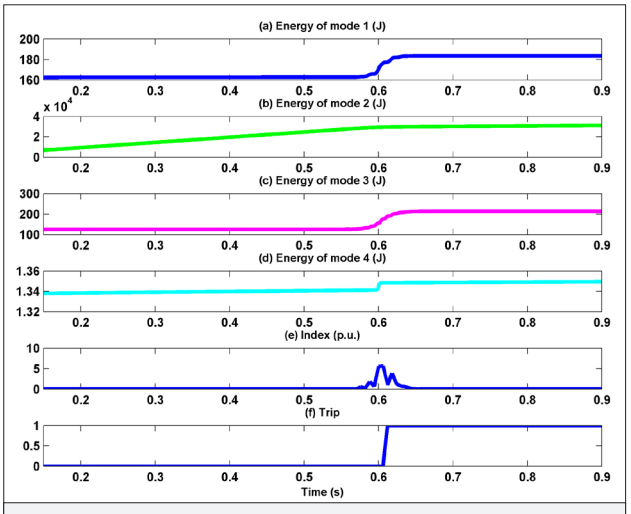

Figure 6. Change in energies of modes, proposed index, and trip signal for large power imbalance

ergies of decomposed modes and produce an effective index (Figure 8). Again, changes in islanding index are sensible, and trip signal is activated in Figure 8. The results show that the algorithm performs successfully in the worst case of islanding.

Normal condition with induction motor starting

Here, a 37kVA induction motor is connected to point B at t=0.4 s. The local load parameters are similar to previous scenarios. Figure 9 shows no meaningful changes in the voltage and decomposed modes. In Figure 10, changes of energies of decomposed modes and the value of islanding index are not considerable. Thus, trip signal is not activated in Figure 10. The results show that the algorithm decision is correct, and no islanding is detected upon the entrance of the induction motor. This scenario is simulated for removing the motor form network. The results show similarly acceptable performance.

Normal condition with nonlinear load switching

In this set-up, a diode nonlinear load is applied to the network at point C and t=0.6 s. Figure 11 and 12 show the corresponding results for this case. The proposed method properly detects no-islanding condition and relatively insensitive to the entrance of the nonlinear load. This scenario is also simulated for the case of the same load exit with similarly acceptable performance.

Effect of the local load quality factor

In the previous scenarios, the quality factor Q_f was assumed to be 2.5. In this section, to analyze the sensitivity of the proposed algorithm to Q_f of local load, the worst-case scenario is repeated to Q_f=3.5. According to Eq. (3) of reference [5], the local load that may lead to worst-case islanding is ($L = \frac{R}{\omega Q_f}, C = \frac{Q_f}{\omega R}$). Thus for R=16.13 Ω and Q_f=3.5, we have L=14.7 mH and C=690.55

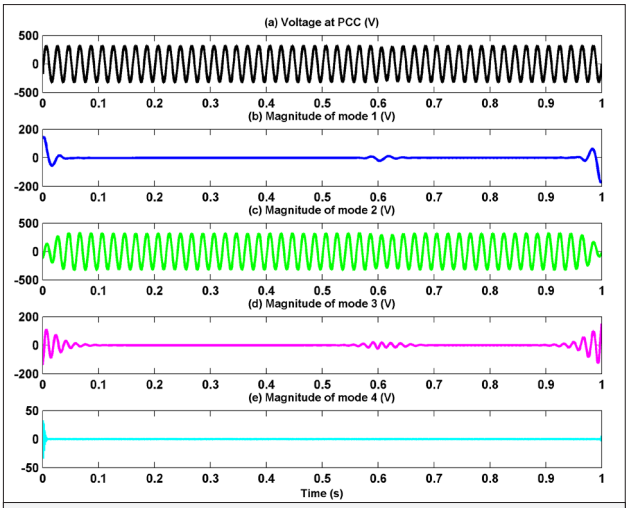

Figure 7. The voltage at PCC and the decomposed modes for low power imbalance

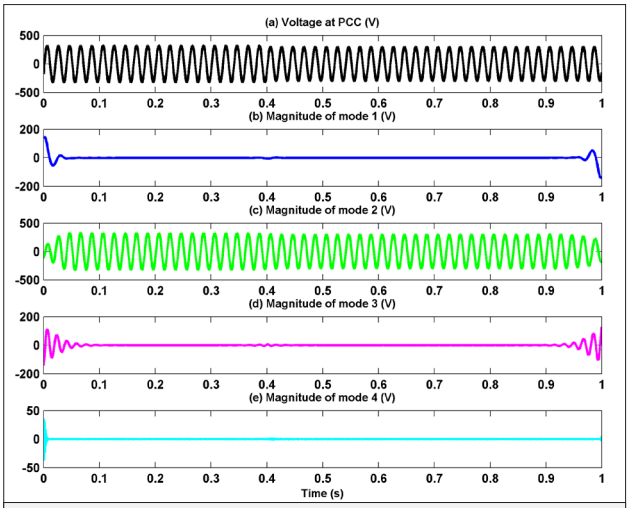

Figure 9. The voltage at PCC and the decomposed modes for induction motor starting

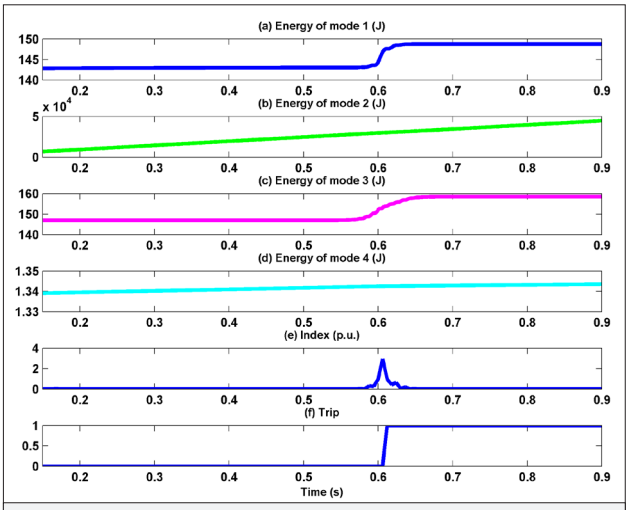

Figure 8. Change in energies of modes, proposed index, and trip signal for low power imbalance

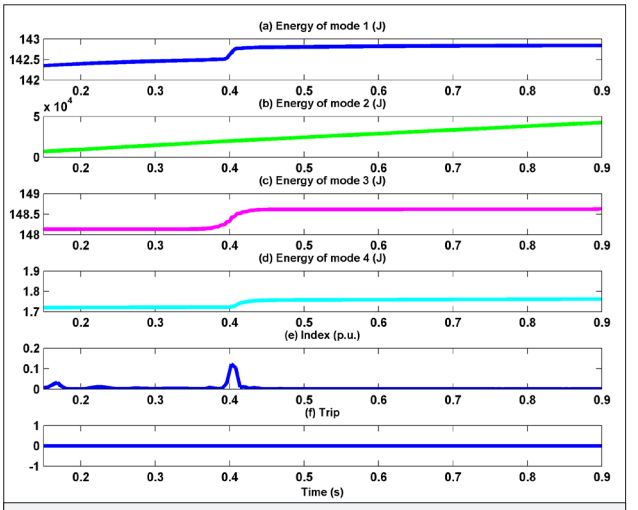

Figure 10. Change in energies of modes, proposed index, and trip signal for induction motor starting

μF. The simulation results for this case show that the suggested islanding index is relatively insensitive to Q_f, and islanding is positively detected (Figure 13).

More specifically, the index decreases versus increases in Q_f, where for extremely high Q_f it enters the NDZ regions. To quantify this effect, simulation was replicated for Q_f=1.5, 4, 5. Although the results of simulation for this case display sensitivity of the new islanding index to the defined thresholds and Q_fs, they also illustrate comparable performance of the index versus other similar methods. In case that the threshold is considered to be 0.4, local load and DG active powers are equal, and Q_f=5, this method faces misjudgment. Since the calculated islanding index is 0.35, the algorithm goes into an NDZ state. Therefore, it is decisive to adjust thresholds against worst-case islanding situation and/or worst-case load connection/disconnection in the network's normal operating condition.

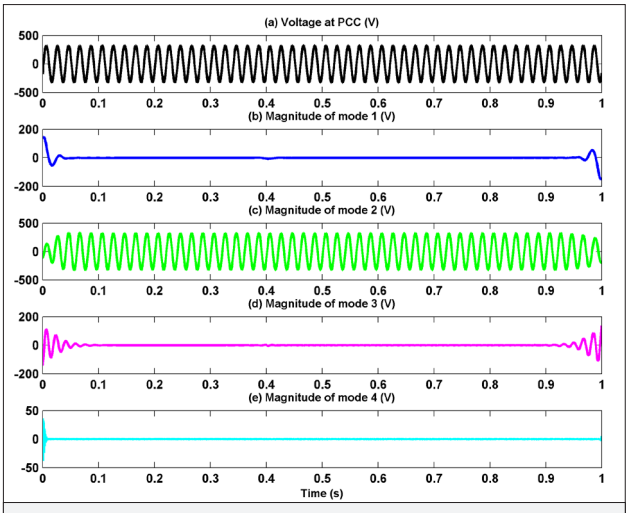

Figure 11. The voltage at PCC and decomposed modes for nonlinear load switching

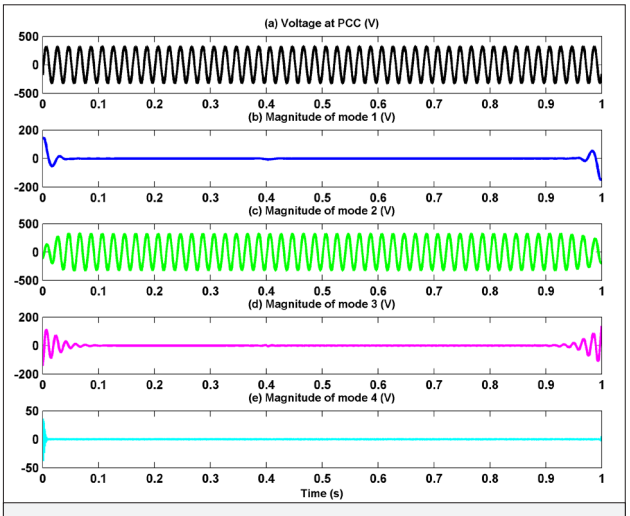

Figure 12. Change in energies of modes ,proposed index, and trip signal for nonlinear load switching

Threshold setting

Threshold setting is an important issue in the passive islanding detection approaches. An inappropriate threshold may lead to NDZ or failing detection zone (FDZ). When powers of load (demanded) and DG (generated) are equal and power factor is one, a remedy to this problem is to assume the worst-case islanding scenarios and consider the minimum value of the index. On the other hand, the most important scenarios to be considered for threshold adjustment are those of connection/disconnection of large load, start-up of induction motors, and nonlinear loads in all of which cases the maximum value of the islanding index is suggested in normal operating conditions. To avoid NDZ and FDZ simultaneously, we must have the following:

$$Max(IslIndx)\,of\ normal < TH < Min(IslIndx)of\ islanding. \quad (14)$$

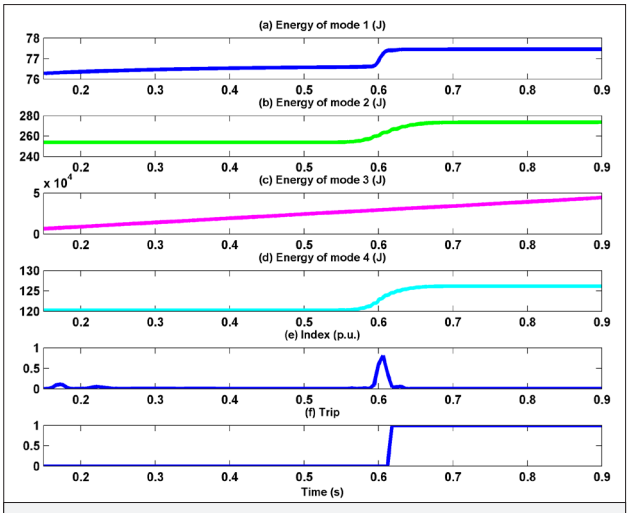

Figure 13. Change in energies of modes, proposed index, and trip signal for Qf=3.5

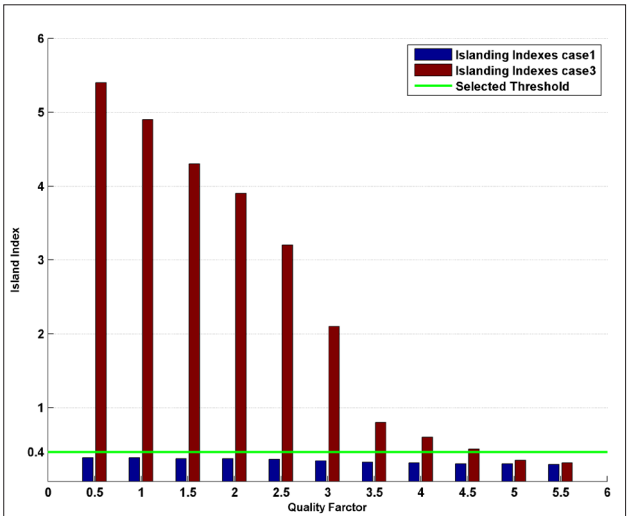

Figure 14. Threshold setting.

Where TH is the threshold. Figure 14 demonstrates an example for the application of Equation (14) for a range of Q_f values. In this situation, R is assumed to be constant, the local Q_f is variable, and the IslIndx index is calculated according to Equation (14). More clearly, if CB2 is opened for any reason, a large load is eliminated from the network while the whole system continues its normal operation. In such a case, thresholds must be tuned for FDZ avoidance. From another point of view, if CB5 is opened, the worst case of islanding phenomenon occurs. In addition, here, thresholds must be adjusted with respect to NDZ avoidance.

As it is shown in Figure 14, a threshold value equal to 0.4 pu makes islanding detection possible except for $Q_f s>5$, whereas for all the cases of normal network conditions, the detector remains silent (no islanding). Altogether, it is suggested to adjust thresholds in such a way that they decrease NDZ and avoid FDZ at the same time.

Analysis of noise effect

The existence of noise in power systems is obvious. It causes susceptibility problems for the previous methods, such as those based on wavelet and S-transforms. The proposed islanding detection relies on VMD transform, which is well known for such desired characteristics as high immunity against noise.

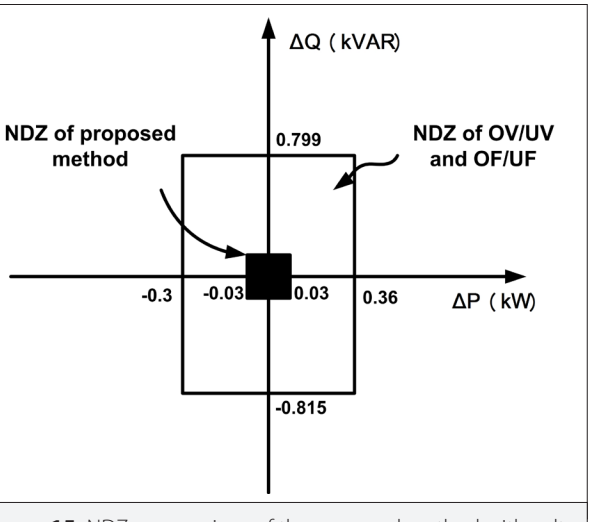

Figure 15. NDZs comparison of the proposed method with voltage- and frequency- based approaches

To analyze our algorithm with respect to this feature, the first simulation (normal condition with large load switching) and third simulation scenarios (islanding condition with low power imbalance) were replicated in the presence of noise where signal-to-noise-ratio is assumed to be 20dB, for both islanding and no-islanding situations. The method is decided properly, in both the presence and absence of islanding phenomenon. In addition, the accuracy of the proposed index has been compared with those of other indexes, numerically, as shown in Table 1. The superior accuracy of the new islanding method is self-expressive. Moreover, contrary to the -wavelet transform and fast discrete S- transform based approaches, it is not dependent to the precision of classifications built upon AIs.

NDZ analysis

NDZ is an important parameter for the diagnosis of islanding occurrence. It specifies a zone/zones in which islanding is not detected in the appropriate time. In the present study, the inverter is of constant-current-controlled type. Thus, to determine the power imbalance levels, the following steps are done leading to islanding detection in OV/UV and OF/UF algorithms. For NDZ detection, the level of the active power imbalance (w) is equal to [28]:

$$\Delta P = -3V \times I \times \Delta V, \quad (15)$$

where V and I are the nominal voltage (V) and current (A) of the DG, respectively. According to IEEE 1547-3003 [29] and

Table 1. Comparison of the proposed islanding method with those of the other methods for SNR=20 dB

Detection time	Average accuracy (%)	Method
0.31 s	97.66	Probabilistic NN [26]
<20 ms	83.63	ST [27]
50 ms	70.6	WT [27]
<20 ms	87.87	FDST+SVM [27]
45 ms	91.5	FDST+BELM [27]
10 ms	98.7	Proposed method

SNR, signal-to-noise-ratio; SVM, support vector machine; NN, neural network; ST, S-transform; WT, wavelet transform; FDST, fast discrete S-transform; BELM, bidirectional extreme learning machine

Table 2. Comparison of the proposed islanding method with some other methods

Principle	Classification	Detection time	NDZ
Frequency	Passive (frequency dependent impedance) [6]	150 ms	Very small
Wavelet	Passive (discrete wavelet transform) [30]	<20 ms	Very small
Frequency	Active (slip mode frequency shift [12]	198 ms	Small
Combination	Passive (rate-of-change-of reactive power and current THD) [14]	60 ms	Not available
Proposed method	Passive (energy index of decomposed voltage)	Approximately 10 ms	Very small

NDZ, non-detection zone; THD, total harmonic distortion

VDE-0126-1-1, if voltage is in the range of 0.88 pu and 1.1 pu, the voltage relays must not take action, i.e., for ΔV=−0.12 and ΔV=0.1 pu. Accordingly, the active power imbalance levels of the present study (when the nominal output power of DG's inverter is 3 kW) would be 0.36 kW and −0.3 kW. In addition, the level of imbalance in the reactive power after islanding equals that of the local reactive demand (VAR) just before the event [28].

$$\Delta Q = \frac{3V^2}{\omega_n L}\left(1 - \frac{\omega_n^2}{\omega_r^2}\right) \quad (16)$$

Where ω_n and ω_r are frequencies (Hz) of the system and load resonance, respectively. The unbalanced reactive power resulted of the islanding provides rises to a drift in the resonance frequency, so:

$$\omega_r = \omega_n + \Delta\omega, \omega_r = {}^{1}/_{\sqrt{LC}}. \quad (17)$$

Moreover, the relationship between the frequency and the reactive power deviations becomes:

$$\Delta Q = \frac{3V^2}{\omega_n L}\left(1 - \frac{f_n^2}{(f_n + \Delta f)^2}\right). \quad (18)$$

According to reference [29], the acceptable ranges of frequency deviations are within 49.7 and 50.3 Hz, i.e., Δf=±0.3 Hz. For the given case study, these are, in order, equivalent to −0.815 and 0.799 kVARs.

Figure 15 compares the NDZs of the proposed method with those of OV/UV and OF/UF for a DG characterized by nominal power and constant-current control mode. For validation purposes, we simulated power imbalances ranging from −10% to 12% of the nominal power, as a result of islanding occurrence, with 0.01 precision totaled to 23 steps in increasing order. It is worth mentioning that both the voltage- and frequency-based approaches have been easily capable of islanding detection. The time duration for an event to be diagnosed as either islanding or normal was assumed to be 1 s. It can be seen clearly from Figure 15 that the NDZ of the suggested method is significantly smaller than those of the other ones. Performance of the proposed method is compared with the other ones as shown in Table 2. The comparison shows that the proposed VMD-based method has better detection time than the other ones; in addition, the NDZ of the method is very small.

Conclusion

A new method for islanding detection based on VMD was proposed. At first, the measured voltage signal was decomposed into its principal modes using VMD. Next, energies of individual modes were calculated as the bases for discrimination between islanding and normal conditions. The algorithm was then applied to various scenarios, including islanding presence, no islanding with different levels of power imbalance, and diversities of load quality factors using simulations. The results of the simulation illustrated acceptable performance of the proposed algorithm with respect to both accuracy and speed, even for the worst-case islanding.

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ISTANBUL UNIVERSITY CERRAHPASA

RESEARCH ARTICLE

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Comparison of Conventional and Modern Controllers for a Gas Turbine Power Plant

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ABSTRACT

Nowadays, many thermal power plants are established for the generation of electrical energy. In this study, the design of a Gas Turbine Power Plant is analyzed in Ambarlı, Turkey. Then, conventional and modern control techniques are applied for comparison. These controllers are conventional proportional and integral (PI), particle swarm optimization based proportional-integral (PSO-PI) and fuzzy gain scheduled proportional-integral (FGPI). The results show that, the performance of the proposed FGPI is better than the conventional controllers on settling time and overshoot of power outputs.

Keywords: Thermal Power Plant, FGPI, Fuzzy Controller, PI Controller, Particle Swarm Optimization

Introduction

The generation of electrical energy has gained more importance with the increasing demand and environmental awareness in recent years. Nowadays, a considerable part of the energy generation is provided by fossil fuel based thermal power plants. However, the coal combustion gases can harm the environment and human health. One of the main reasons for these situations, is the change in the parameters of the gas turbine during the generation of energy. The simplest evidence of this is the contamination of the boiler and heating pipe surfaces of the thermal power plant that has been occured throughout the years by coal-burning [1].

Combined cycle power plants (CCPP) has been proposed in [2]. In this study, the effects of inlet fogging and optimization on performance is considered by energy analysis. Moreover, it is indicated that one of the best methods to reduce CO_2 emissions is decreasing the energy losses.

In addition to [1], the control systems play important role due to natural expectations of consumers and the necessity of generation of electricity. Thus, the importance of the control systems in energy generations are rised drastically as shown in [3]. In recent study, energy optimization is performed by using varies optimization algorithm to minimize the CO_2 values and raise the efficiency of the power plant in [4]. In this study, NSGA-II (Non-dominated Sort Genetic Algorithm-II) is applied to get the final solutions in the multi-objective optimization of the CCPP. In [5], Genetic Algorithm and Artificial Bee Colony Optimization are applied for environmental economic load dispatch. Thus, it provides a great advantage for cost reduction and NO_x emission as a result.

Modern optimization and control techniques are applied with the optimized set values and their effects on the active power-frequency control are analyzed in Ambarlı, Turkey in [6]. In the same study, 6 different controller types are performed; PI, PSO-PI, Artificial Bee Colony based Proportional-Integral (ABC-PI), Proportional-Integral-Derivative (PID), Particle Swarm Optimization based Proportional Integral-Derivative (PSO-PID) and Artificial Bee Colony based Proportional-Integral –Derivative (ABC-PID). According to the mentioned work, PID controller

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optimized with artificial bee colony optimization gives better results when compared to the other controllers. Furthermore, the model of Ankara-Çayırhan Thermal Power Plant is also considered [7]. Two different controller types are performed in the mentioned study which are PSO-PID and FGPI for their effects on overshoot and settling time. If minimum settling time is required, PSO-PID must be employed. On the other hand, FGPI can be utilized if minimum overshoot and soft adaptation are desired.

In [8], linear matrix inequalities are solved by Genetic Algorithm and Particle Swarm Optimization for adaptive sliding mode controller design is presented. The unstable situation in the gas turbine is overcame by this method. In addition to these, Particle Swarm Optimization-based controller is applied to the thermal power plant in [9]. The reason for this is to prove that, the proposed controller provides a better settling time response than the conventional controllers. Furthermore, a gas turbine engine is regulated with the PSO-based PI controller to illustrate the optimal control solution.

A fractional order fuzzy-PID (fuzzy-FOPID) controller is suggested for cycle power plant (CPP) with dynamic particle swarm optimization system [10]. Fuzzy-FOPID offers the best possible results when compared to the other methods in this study.

In our paper, firstly the model of Gas Turbine Power Plant in Ambarlı, Turkey is obtained and the block diagrams of each module are illustrated with different controllers that are conventional PI, PSO-PI and FGPI. Moreover, the responses of the system with respect to these controllers are compared. The two significant parameters for comparison are overshoot and settling time. It is observed that, although PI controller has no overshoot, the settling time is greater than the other controllers. If cost reduction is considered, this can be taken into account. Contrary, FGPI controller has much better settling time when compared to former. Nevertheless, the proposed study showed that modern control techniques are much more proper than the conventional controllers. The parameters of the controllers are determined by the classical methods. Furthermore, FGPI also increases both the performance and service life of the power plant therefore, employment of the these methods is a necessity for the operation of modern power plants.

Basic Mathematical Model for Gas Turbine

One of most popular power generations systems is the natural gas power plant. Here, air is compressed, burned and enlarged in the turbine to obtain power. Operation principle of gas turbine power plants is as follows: the natural gas is passed through the regulation and measuring station (RMS) and reduced to the operation pressure. It is stored or transmitted to the plant for immediate use with a continuous gas cycle. The natural gas passed through the filter station in the power plant field is transferred to the combustion chambers via the emergency stop and regulation valves. The common shaft includes compressor and turbine. In the model, we used two large silo type combustion chambers with a hybrid burner. Combustion technology is of great importance in terms of environmental legislation. The waste NOx generated after combustion, must be below the threshold value (300 mg/Nm3). The required air in the combustion chamber is obtained by open loop and used with air filters.

The whole system consists of a gas turbine compressor, combustion chamber and turbine. In some cases, it only refers as the turbine. Figure 1 shows the simplified model of the gas turbine. When atmospheric air enters the compressor it is compressed and send to the combustion chamber. In the combustion chamber, high-pressure hot gas is burned by fuel injection. Power is obtained by expanding the turbine. Then, a large portion of the power provided by the turbine is used to run the compressor and a small portion is used in auxiliary tools, the remaining portion is the net power obtained from the plant. Simplified gas turbines should provide air standard requirements.

Simplified model,

- The fluid is air, it is assumed as the ideal gas throughout the cycle
- The combustion process is not taken into account, it is assumed that heat is supplied from outside at constant pressure
- The turbine exhaust and compressor suction operations are neglected. The fluid goes out of the turbine under constant pressure is feedbacked into the compressor.

Whereas the power plant is considered as a closed system where the parameters of the system such as turbine and combustion chamber are open loop components. Cycles which depend on assumptions of air standards are defined as ideal air cycles. Besides these assumptions, models have other assumptions such as some of the state changes are considered to be reversible to obtain approximate results.

Figure 1 shows the P-V and T-s graphs of the Brayton cycle, a simple gas turbine. Heat exchanges are made at constant pressure and compression and expansion processes are isotropic. In this graph, the T-s diagram refers to the gas turbine cycle. From the place where entropy increases, it is seen that the constant pressures are separate. What this means is that, the power provided by the compressor is greater than that provided by the turbine. Otherwise, the target cannot be obtained from the turbine.

Turbine power, compressor power, net power and yield are obtained by applying the first law of thermodynamics to the gas turbine cycle. Thus, it is seen that the yield is a function of the pressure ratio. The yield does not depend on the maximum temperature, the change in specific temperatures depends on the yield temperature.

The Brayton and Carnot cycles with the same temperature range and the same entropy changes are shown on the same

T-s diagram in Figure 2. From the graph, it can be seen that the Brayton cycle consists of small Carnot cycles. Thus, the yield of the Carnot cycle is higher than that of Brayton. The simplified gas turbine is based on the Carnot cycle [6, 11].

Speed Regulator

The turbine power is constantly changes by the variation of the load. The imbalance between the generated power and consumed powers is considered as a change in the speed of the turbine. If the load is variable, the generation must be variable to keep the frequency constant. This is done through the by the speed regulator. The speed regulator adjusts the amount of gas to the combustion chamber of the gas turbine. This cycle is a closed cycle which continues until the power and speed error are zero. The amount of gas is controlled by the control valve in the gas turbine. The stop valve is a valve that is connected in front of the control valve and is for protection purposes.

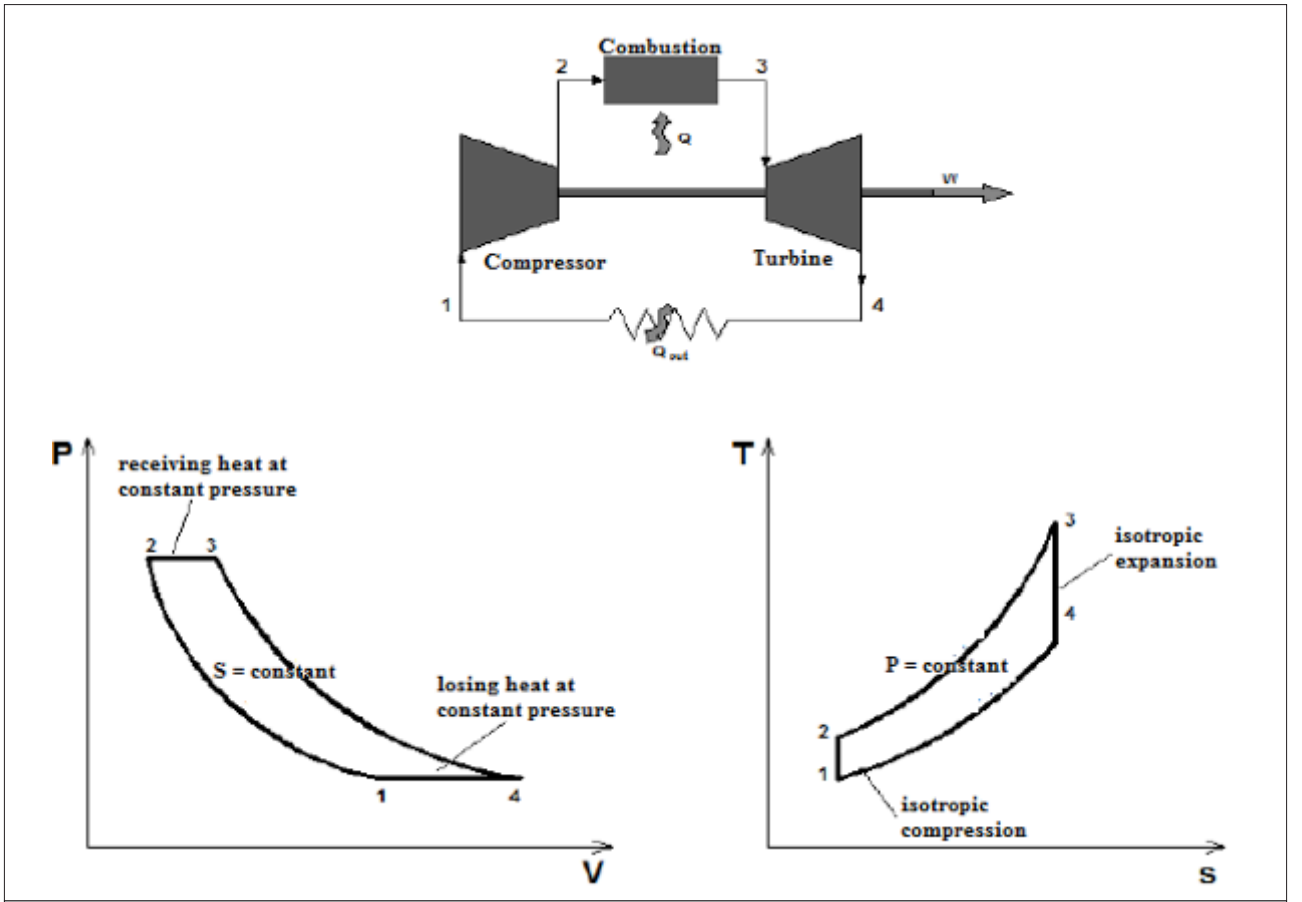


Figure 1. A Simple Gas Turbine Cycle

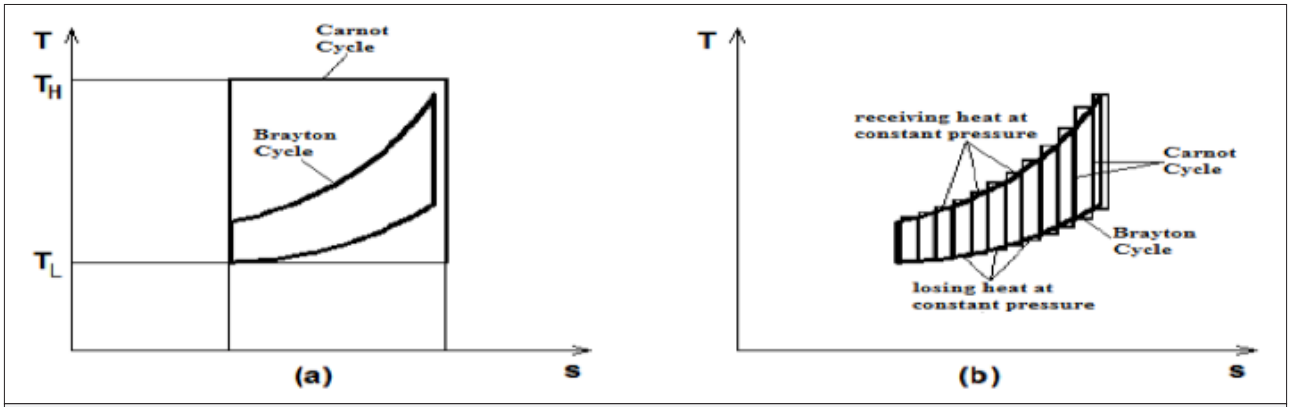


Figure 2. Comparison between Brayton and Carnot Cycles Efficiencies

Block diagram of a simplified Gas Turbine is illustrated in Figure 3 where speed regulator is first order system.

where

Kd: Speer regulator gain

X: Speed regulator primary time (delay) constant

Y: Speed regulator secondary time (delay) constant

a: Burner gain constant

b: Burner time (delay) constant

T_Y: Combustion chamber time (delay) constant

T_GT: Time (delay) constant depends on turbine dynamic characteristics

Calculated values for related parameters are given in Table 1.

Basic Mathematical Model for the Generator

Generators in power systems are generally considered to be large masses with two opposite moments in Figure 4.

The mechanical moment (T_m) is produced in the turbine and this force has an effect that increases the speed of rotation. In contrast, the electrical moment (T_e) generated by the load causes the speed to be reduced. This happens at a constant speed ($\omega = \omega_0$) when the two moments are equal. The electrical load increases $T_e > T_m$ and the generator slows down. In this case, the generator is accelerated again. Otherwise, the generator is decelerated. In power systems, all these operations are repeated continuously, because the load is not stable. Generator equations are as follows,

Table 1. Simplified Gas Turbine Parameter Values[6]

Parameter	K_d	X	Y	a	b	T_Y	T_GT
Value	1	0.65	0.1	1	0.05	0.4	0.1

$$T_T = I\alpha \quad (1)$$

$$M = I\omega \quad (2)$$

$$P_T = \omega T_T = \omega I\alpha = M\alpha \quad (3)$$

where I is current per phase, α is field flux, ω is angular speed, M is momentum and T_T is total torque.

Initially, it is a single rotating machine and the speed is ω_0 and δ_0 is called as phase angle. Due to the increase of the requested load or mechanical and electrical deterioration, the values T_m and T_e will change. Speed of the machine in case of acceleration is obtained in the following term.

$$\omega = \omega_0 + \alpha t \quad (4)$$

and

$$\Delta\delta = \int (\omega_0 + \alpha t)dt - \int \omega_0 dt = \omega_0 t + \frac{1}{2}\alpha t^2 - \omega_0 t = \frac{1}{2}\alpha t^2 \quad (5)$$

$\Delta\omega$ (frequency deviation) can be identified as,

$$\Delta\omega = \alpha t = \left(\frac{d}{dt}\right)\Delta\delta \quad (6)$$

The relation between phase angle deviation, speed deviation and net acceleration moment is given in equation (7).

$$T_T = I\alpha = I\left(\frac{d}{dt}\right)(\Delta\omega) = I\left(\frac{d^2}{dt^2}\right)(\Delta\delta) \quad (7)$$

Thus, we find the net power

$$P_T = P_m - P_e \quad (8)$$

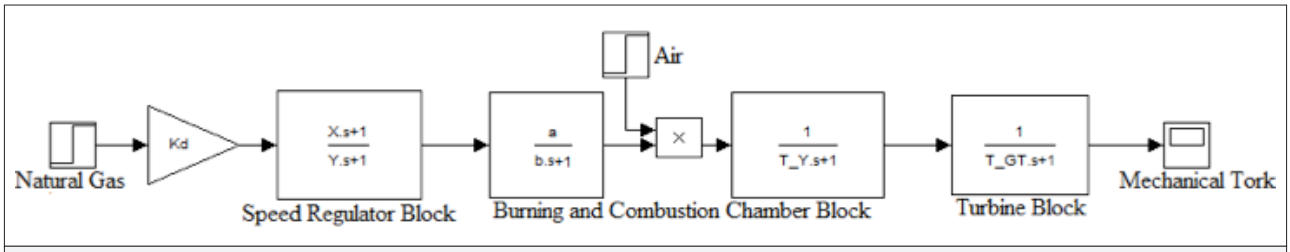


Figure 3. Simplified Gas Turbine Model

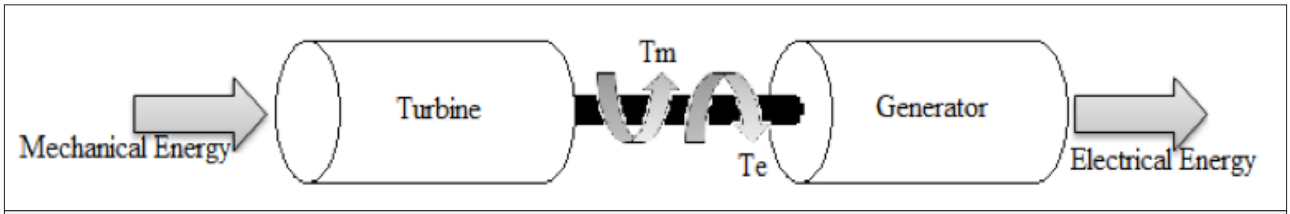


Figure 4. Physical Model of Turbine Generator System

The connection between net power frequency variation is given in equation (9).

$$P_T = \omega_0 I\left(\frac{d\Delta\omega_0}{dt}\right) = M\frac{d\Delta\omega_0}{dt} \quad (9)$$

If equality (9) is written in Laplace form

$$\omega_0 = \frac{1}{Ms}P_T = \frac{1}{Ms}(P_m - P_e) \quad (10)$$

The block diagram of the system obtained from theseequations is shown in Figure 5.

The relation between frequency change Δω and load change ΔP_L is given in equation (11).

$$\Delta P_e = \Delta P_L + \Delta P_D \rightarrow \Delta P_L = D\Delta\omega \rightarrow D = \frac{\Delta P_L}{\Delta\omega} \quad (11)$$

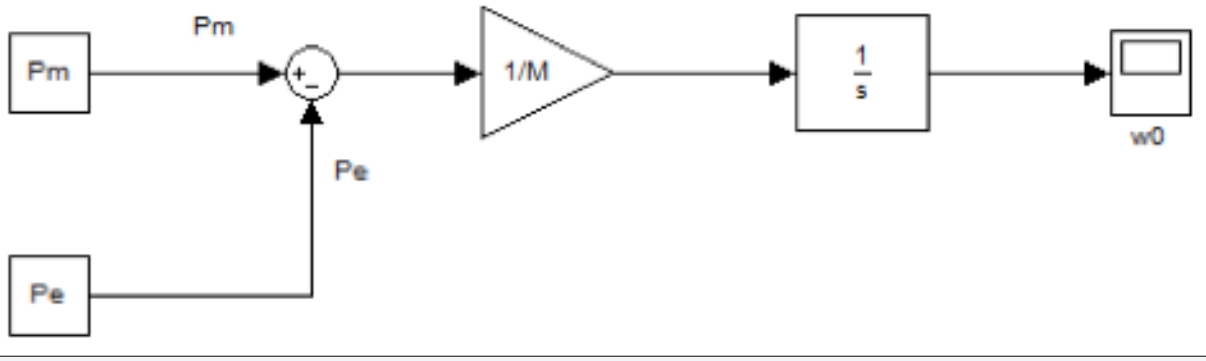


Figure 5. Simplified Block Diagram of Turbine-Generator System

Figure 6. Block Diagram of the Rotating Mass and Load

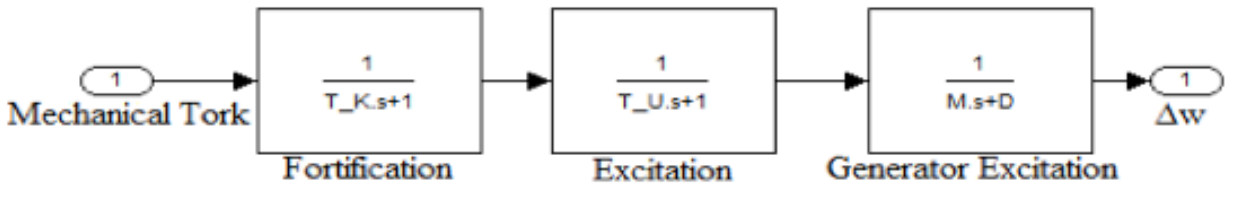


Figure 7. Generator Model

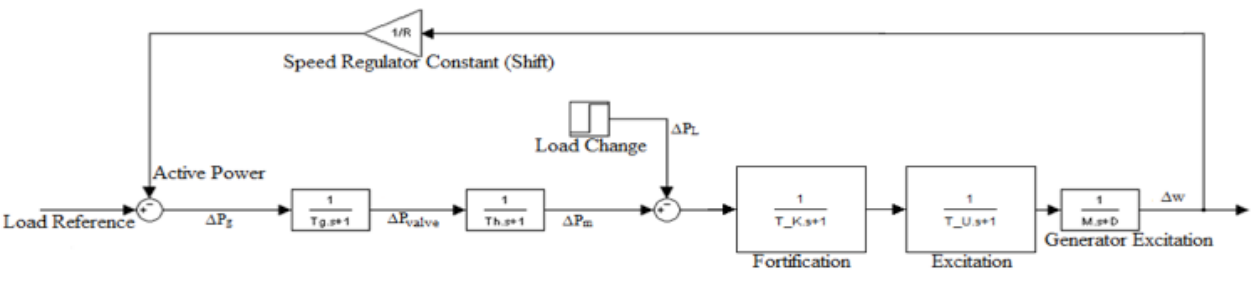


Figure 8. General Model of a Power System

D is the damping constant. It is the percentage of change in frequency which is about 1-2% for the load change. For example, if there is a frequency change of 1% in a load variation of 1%, the damping ratio is obtained from equation (11). The damping factor is D=1/1=1. The load damping model is shown in Figure 6.

If the automatic voltage regulator (AVR) fortification and excitation blocks are added, the diagram becomes as the following in Figure 7.

An overview of the power system can be examined as in Figure 8.

The R value in the figure determines the speed output power characteristics of the production unit. R called as speed regulation constant or shift, shown in equation (12).

$$R = \frac{\Delta\omega}{P_{jn}} = \frac{\Delta f}{P_{jn}} = \frac{f_2 - f_1}{P_{jn}} \quad (12)$$

where

P_{jn}: Nominal active power of the generator unit (MW)

f_2: No load frequency (Hz)

f_1: Frequency in nominal load (Hz)

R: Speed regulation constant or slip (Hz/MW)

Δω: Speed

ΔP: frequency distortion

Thus, the speed regulation constant is added to the system to obtain a simplified generator model in Figure 9.

where

T_K: Fortification time (delay) constant (seconds)

T_U: Excitation time (delay) constant (seconds)

M: Generator time (delay) constant (seconds)

D: Damping Factor

R: Speed regulation constant or slip (Hz/MW)

All values of parameters are given in Table 2.

Table 2. Simplified Generator Parameter Values[6]

Parameter	T_K	T_U	M	D	R
Value	0,25	1	0,1	1	1

Table 2: *Simplified Generator Parameter Values[6]*

Controller Methods

The reason for using control systems, the reference value given in the system dynamics parameter changes and depending on the situation defined at the desired level to perform the control criteria.

Conventional PI Controller

The system's response curve method is employed to obtain the best result of the control system in Figure 10 [12].

In a system, there are parameters that affect the settling time of the controller. These are the time constant T_s, dead time delay T_d and system gain. The parameters of the PI controllers according to the system's response curve method are shown in Table 3.

PI controller structure is given in equations [13, 14].

$$K(s) = K_p e(t) + K_i \int_0^t e(t)dt \quad (13)$$

Table 3. PI Controller's Parameter Values[6]

	K_p	T_i
PI	$\frac{0.9T_s}{K_s.T_d}$	$3,33T_d$

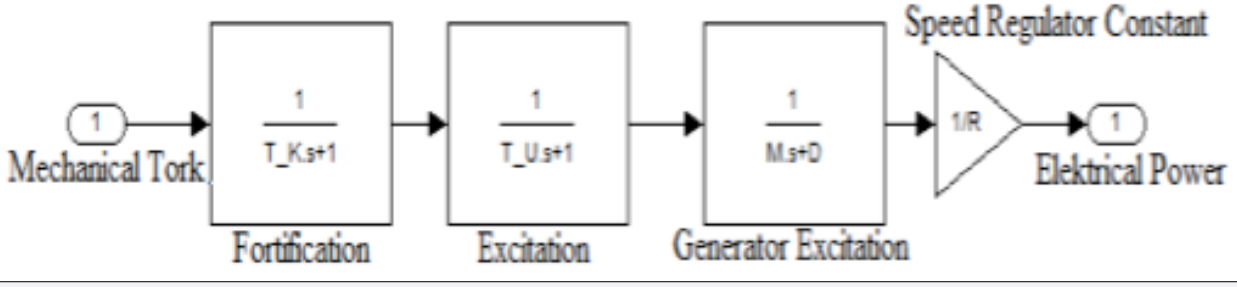


Figure 9. Simplified Generator Model

$$\frac{K_p}{T_i} = K_i \quad (14)$$

K_p is proportional gain coefficient, K_i integral gain coefficient, $e(t)$ is the time error.

PI controller values were obtained by using equation (14) for Gas Turbine.

Result of PI controller parameters are calculated as K_p = 0.680 and K_i= 0.6.

Particle Swarm Optimization Based PI Controller

In literature, particle swarm optimization (PSO) is proposed to find the best results of numerical problems based on the social behavior of bird flocks. In the PSO, each individual or particle travels through the solution space that is identified. Each individual keeps the places it ever visited and best one among them in its mind as well as all the other members of the flock. Then, the total best individual experiences are taken into account and compared to each other in order to reach the global best.

Each individual seeks a solution in the XY coordinate plane in a two-dimensional solution space. The speed of the individual is defined by v_x and v_y (moving along the X and Y axes). Each individual keeps its best value as the best "pbest" value in memory. In addition, each individual keeps the information of the best value, gbest information and pbest information. The position and velocities of each individual are shown in equation (15) and equation (16) as the following term in [13].

$$\vartheta_i^{k+1} = \vartheta_i^{k} + c_1 \mathrm{rand}_1 . \left(p_{best_i} - s_i^{k}\right) + c_2 \mathrm{rand}_2 . \left(g_{best} - s_i^{k}\right) \quad (15)$$

$$s_i^{k+1} = s_i^{k} + \vartheta_i^{k+1} \quad (16)$$

The PSO shows the movement of the search point in a two-dimensional solution space. s^k and ve s^{k+1} shows the current and new individual locations. Moreover, ϑ^k and ϑ^{k+1} shows current and new speeds respectively. ϑ_{pbest} and ϑ_{gbest}, p_{best} and g_{best} shows the speeds according to their location. Changes in the individual position of these vectors are shown in Figure 11.

The equation (17), (18) which are kept within a certain limit for the damping and oscillation at certain points of the speed, are shown [14].

$$V^{max} = (x^{max} - x^{min})(\%10 - \%20) \quad (17)$$

$$V^{min} = -V^{max} \quad (18)$$

It is kept between certain values by using the coefficients of the particles

$$\vartheta_i^{k+1} = X.\left[\vartheta_i^{k} + c_1 \mathrm{rand}_1 . \left(p_{best_i} - s_i^{k}\right) + c_2 \mathrm{rand}_2 . \left(g_{best} - s_i^{k}\right)\right] \quad (19)$$

X is the constraint coefficient that is given in equation (20).

$$X = \frac{2}{\left|2-\varphi-\sqrt{\varphi^2-4\varphi}\right|}, \varphi = c_1 + c_2 , \varphi > 4 \quad (20)$$

Through the restriction coefficient, individuals will be collected at a single point in the future. Figure 12 shows the particle swarm optimization algorithm scheme [15].

The optimization software is designed to approach the fitness function which indeed is the sum of absolute values of errors to zero.

In the simulation stage, the speed ranges of the individuals are determined as in equation (17) and equation (18). In order to compensate local and global search performances, the *X* coefficient of equation (19) and equation (20) is used. For simulation, the number of individuals is 5 and the number of iterations is 20. The sum of the absolute values of the error function is used as the target function. The goal of optimization is to find the most appropriate PI gain values. Figure 13 shows a block diagram of the control of particle swarming

As the result of optimization K_p and K_i are found 0.5880, 0.7156.

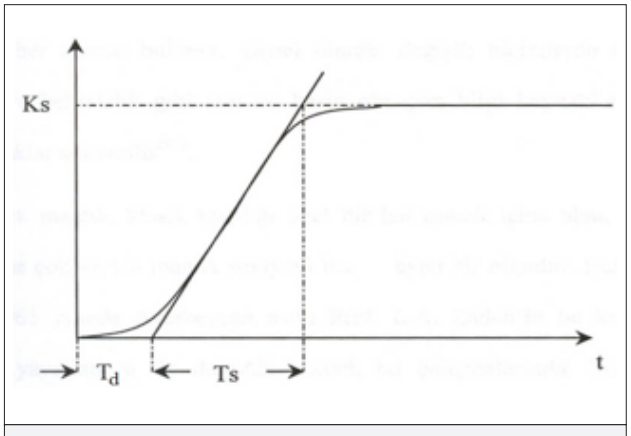


Figure 10. Response Curve

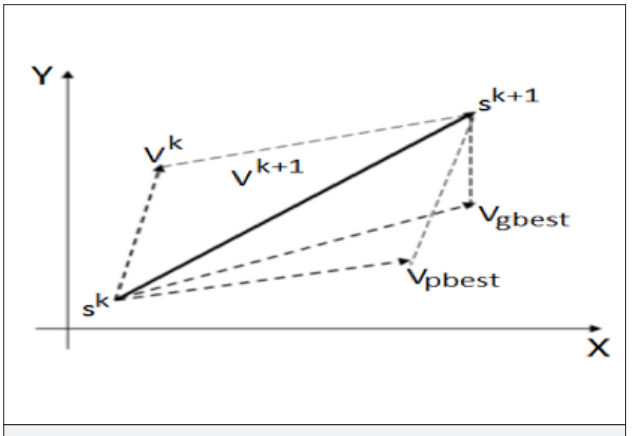


Figure 11. Particles Movement

The Proposed FGPI Controller

An alternative to Boolean algebra, fuzzy logic system is more suitable for human thought. In particular, it provides great convenience in complex and uncertain control systems.

Fuzzy gain scheduling proportional and integral (FGPI) control generated in the system for each entry and output. Seven membership function has been created. The membership functions created are expressed as follows; NB (Negative Large), NO (Negative Medium), NK (Negative Small), S (Zero), PK (Positive Small), PO (Positive Medium), PB (Positive Large). All membership are chosen as trimf (triangle membership function) because of the more sensitive control range. The value ranges of all membership functions are arranged in sensitive intervals according to the response of the system to the control response. Fuzzy logic rules and membership functions for determining PI control gain ranges are obtained according to the unit step response of the system.

The fuzzy logic control algorithm is the most important factor in the errors and derivative of errors.To operate a control system at the desired level, the range of the error and the derivative of the error must be adjusted precisely. The variance of the error and derivation of error for the gas turbine is shown in Figure 14 [7].

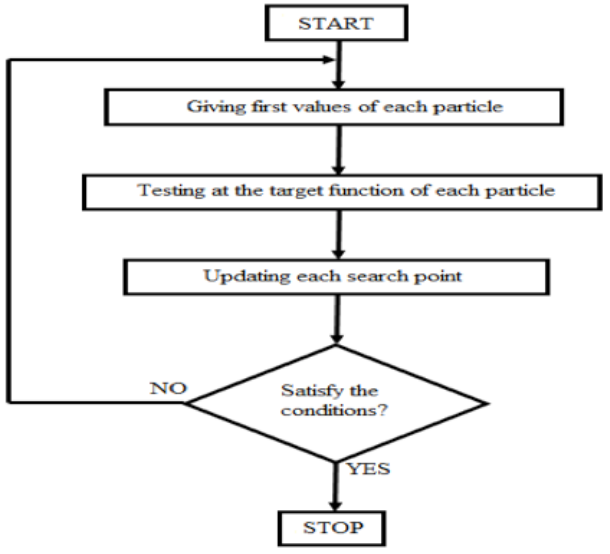
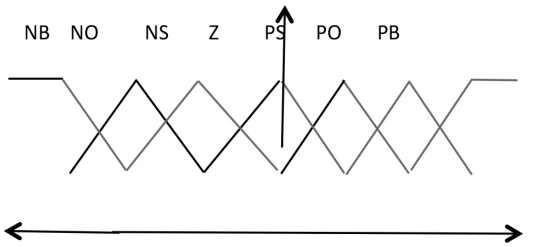


Figure 12. PSO Algorithm [15]



-30.6 20 10 0 10 20 30.6

(a)

e_1

NB NO NS Z PS PO PB

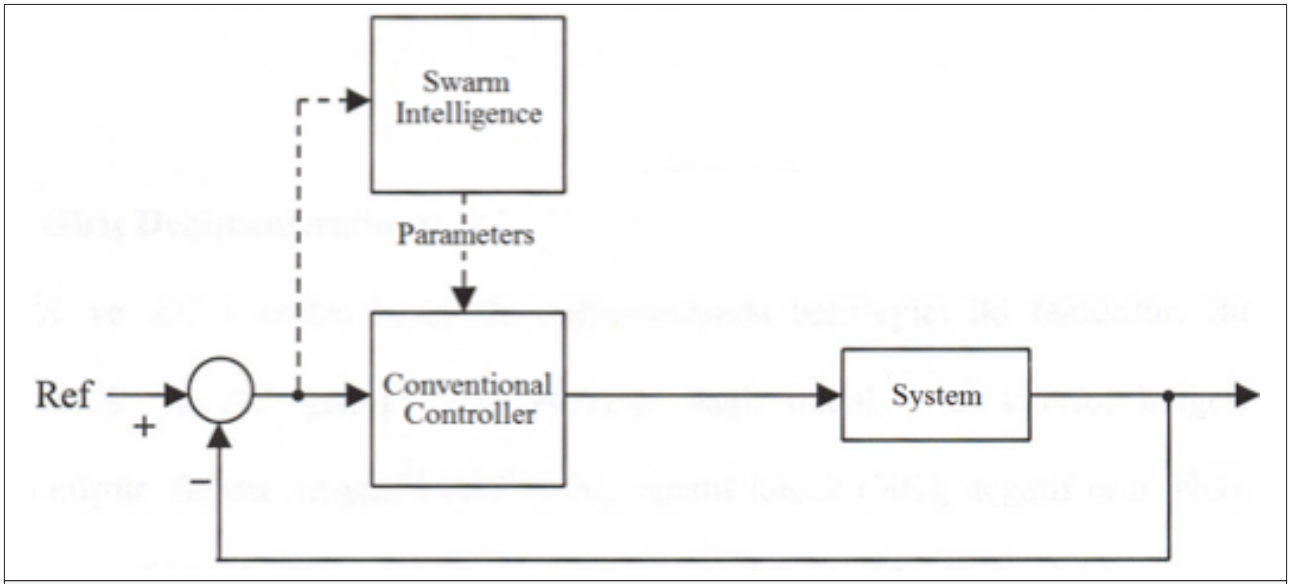
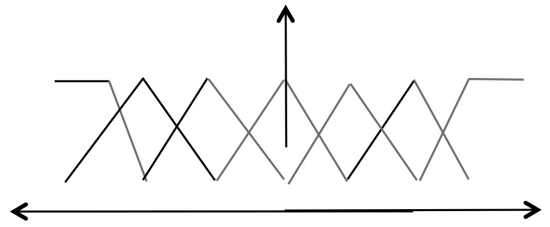


Figure 13. Block Diagram of Particle Swarm Optimization



-.0.01 -0.006 -0.004 0 0.004 0.006 0.01

de_1

(b)

Figure 14. a, b. Ranges of Input Variables. Error (a), Derivation of Error (b)

Here, e_1 expresses the error value of the system. The error values are set to -30.6 to 30.6. de_1 represents the derivative of the error which varies from -0.01 to 0.01.

Proposed control system gain values K_p and K_i regulate the Gas Turbine by the selected PI parameters of the controller. The control gain ranges are also precisely arranged. The defuzzification rules of this system are given in Table 4 and Table 5.

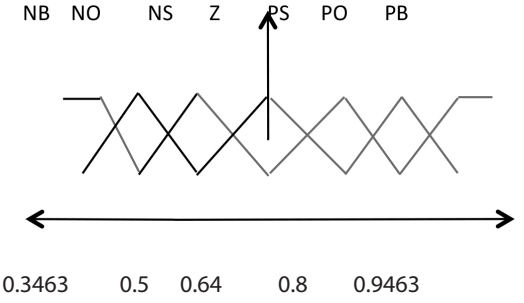
The membership functions for fuzzification of the output values of the gas turbine are shown in Figure 15.a and 15.b.

Table 4: Rules of K_p parameters for power output [7]

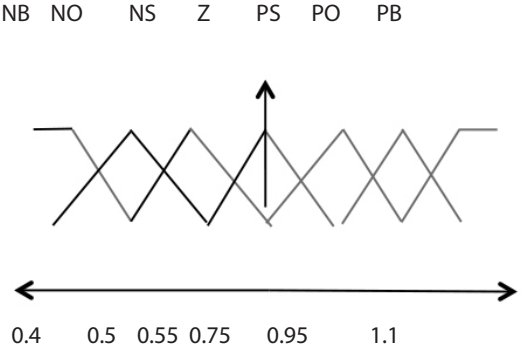
de e	NB	NM	NS	Z	PS	PM	PB
NB	*PB*	*PB*	*PB*	*PB*	*PB*	*PM*	*PM*
NM	*PM*	*PM*	*PM*	*PM*	*PM*	*PS*	*PS*
NS	*PS*	*PS*	*PS*	*PS*	*PS*	*Z*	*Z*
Z	*Z*	*Z*	*Z*	*Z*	*Z*	*NS*	*NS*
PS	*NS*	*NS*	*NS*	*NS*	*NS*	*NM*	*NM*
PM	*NM*	*NM*	*NM*	*NM*	*NM*	*NM*	*NB*
PB	*NB*	*NB*	*NB*	*NB*	*NB*	*NB*	*NB*

Table 5: Rules of K_i parameters for power output [7]

de e	NB	NM	NS	Z	PS	PM	PB
NB	*NB*	*NB*	*NB*	*NB*	*NB*	*NM*	*NM*
NM	*NM*	*NM*	*NM*	*NM*	*NM*	*NS*	*NS*
NS	*NS*	*NS*	*NS*	*NS*	*NS*	*Z*	*Z*
Z	*Z*	*Z*	*Z*	*Z*	*Z*	*PS*	*PS*
PS	*PS*	*PS*	*PS*	*PS*	*PS*	*PM*	*PM*
PM	*PM*	*PM*	*PM*	*PM*	*PM*	*PM*	*PB*
PB	*PB*	*PB*	*PB*	*PB*	*PB*	*PB*	*PB*



(a)



(b)

Figure 15. a, b. Ranges of Output Variables

a) K_p b) K_i

K_p range of the designed Gas Turbine is [0.3463 0.9463] where K_i are designed as [0.4 1.1].

Simulation and Results

In this study, the design of PI, PSO-PI and FGPI controllers are employed. These controllers are applied into the Gas Turbine Power Plant which reduced the mathematical model. The set values of the power plant are used to in the comparison of the results. Response curves obtained from all proposed controllers are shown in Figure 16. The set value is 1 MW and the period is 200 second as a square wave which is suitable to compare the results.

If we focus on the graph, Figure 17 and Figure 18 will be obtained.

The overshoot and settling time are presemnted in Table 6. One can see that, there is no overshoot in Conventional PI controller, the power overshoots of FGPI and PSO controllers are %0.1

Table 6. System performance

	Overshoot (%)	Settling Time (s)
PI	-	16
PSO-PI	0.2	10
FGPI	0.1	8

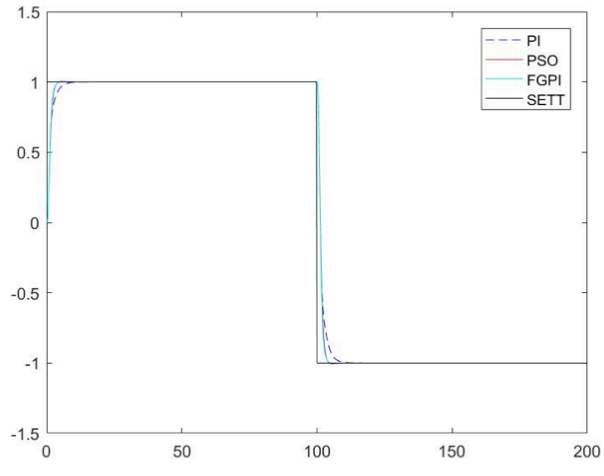


Figure 16. Power Output with All Controllers

and % 0.2 respectively. However, if the settling times for power output are taken into account, it will be realized that FGPI controller is less than both PI and PSO-PI controllers. According to the Figures and Table, FGPI controller is better than Conventional PI controller as well as PSO-PI controller. Since the settling time is extremely minimum to the reference signal in the Gas Turbine Power Plant.

Conclusion

In this paper, the model of Gas Turbine Power Plant in Ambarlı, Turkey is analyzed. The controller gain parameters employed in this system are obtained by conventional methods. Afterwards, three controllers namely conventional PI, PSO-PI and FGPI are proposed and compared to each other. In this comparison,minimization of the settling time is desired and it is seen that FGPI is the best among the others. Moreover, conventional PI and PSO-PI parameters reduce the performance and efficiency of

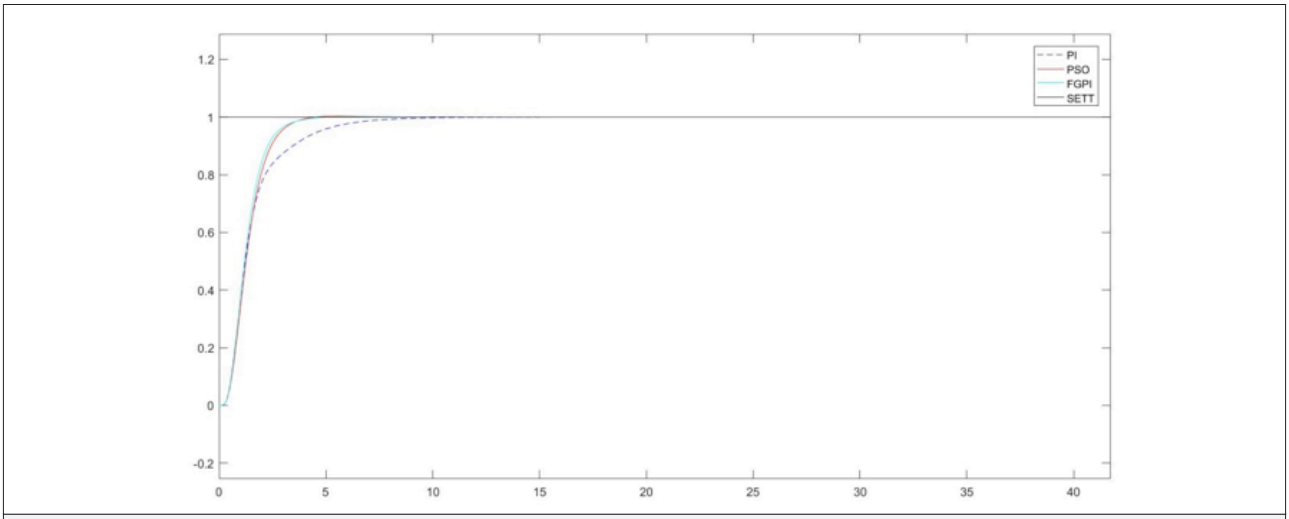


Figure 17. Rise Time Output

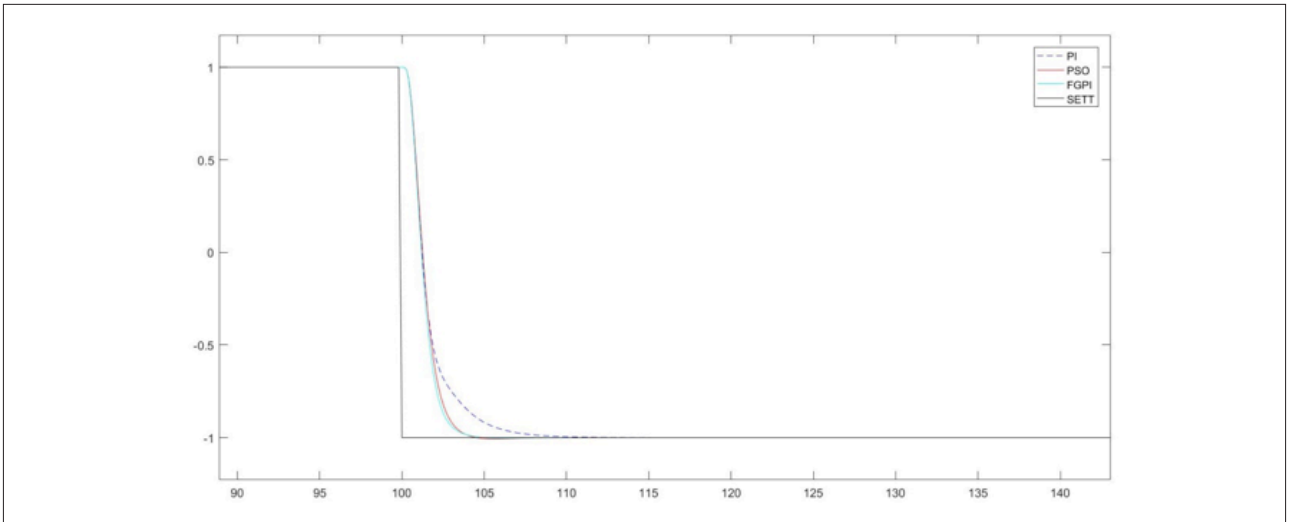


Figure 18. Fall Time Output

the plant throughout in its service life. Consequently, it is observed that, FGPI controller achieved satisfactory performance in Gas Turbines.

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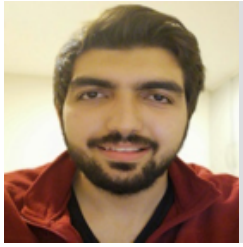

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ISTANBUL UNIVERSITY CERRAHPASA

RESEARCH ARTICLE

Electrica 2019; 19(2): 158-165

Design and Simulation of 64 Bit FPGA Based Arithmetic Logic Unit

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ABSTRACT

Arithmetic Logic Unit (ALU) is the essential part of the Central Processing Unit (CPU) core which performs arithmetical operations such as addition, subtraction, division, multiplication etc., logical operations such as and, or, xor etc. and shift-rotate operations. The CPU performance is directly related to the performance of ALU. In this study, the 64-bit ALU has been designed by using the Very High Speed Integrated Circuits Hardware Description Language (VHDL) and Altera Field Programmable Gate Array (FPGA) families, synthesized and simulated with the help of Altera Quartus II (Intel, Santa Clara, CA, USA) v13.0sp1 and Modelsim-Altera v10.1d (Intel, Santa Clara, CA, USA) software. Many different studies are given about ALU Design and Implementation with the use of FPGA architecture and VHDL language. The difference of this study from recent studies is that the proposed design allows the processing of the signed numbers. Also, Conditional Sum Adder (COSA) is used in addition operation instead of Carry Ripple Adder (CRA) or Carry Look-ahead Adder (CLA) because of its benefit in fast addition and less propagation delay of Carry Chain.

Keywords: FPGA, VHDL, arithmetic logic unit design

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Introduction

In a computer system, Arithmetic Logic Unit (ALU) is the vital structure of the Central Processing Unit (CPU). Modern CPUs contain very powerful and complex ALUs. In addition to ALUs, today's CPUs have a control unit (CU) which operates the ALU through the control signals. These signals tell to ALU which operations will be performed and the ALU stores results of these operations in output registers. Also, the CU moves the data between these registers, the ALU, and memory through the control signals.

Very High Speed Integrated Circuits Hardware Description Language (VHDL) is one of the most popular languages of an industry for the modeling, description, and synthesis of digital circuits and systems. It is a high-level language that is difficult to learn, and suitable for the design of complex systems. Also, this language allows users to create complex data types. Design units, also called library units, are the main components of the VHDL language. It consists of 4 different notifications which are package, entity, architecture and configuration-component. Also, new library creation and library management which are two of the most valuable features is allowed in VHDL language [1, 2].

The main reason of using VHDL in this study is that the language allows us to manage the library and create a special structure such as package, block, function, procedure, and component etc. This feature made the design simpler and easy to manage. Also, using these structures provide portable and reusable designs.

A basic field programmable gate array (FPGA) is an integrated circuit with logic blocks which are arranged in a matrix. In addition to logic blocks, modern FPGAs have multiplier blocks and memory blocks inside them. In an FPGA structure, logic blocks and interconnections between them, input/output elements (IOE) etc. are configurable. When an FPGA is configured, the internal circuitry is connected in a way that creates a hardware implementation of our design. If

the FPGA needs to be reprogrammed, the configuration data in it can be deleted and programmed again and again, and this is the most important reason why FPGA is so valuable in the market. Unlike CPUs, FPGAs do not have a fixed hardware design. In contrast, they can be programmed from scratch according to user applications. The functions that logical cells perform and the connections between these functions are determined by the user. Some of other important features of an FPGA have made its use popular include parallel processing capability, design testing and validation, and the ability to embed a processor in an FPGA as discussed by [3, 4].

Many different studies are given about ALU Design and Implementation with the use of FPGA architecture and VHDL language. In these studies carry ripple adder (CRA) or carry look-ahead adder (CLA) is used in addition operation and unsigned numbers are processed in ALU. Also, Xilinx's software and hardware are used as a development environment as discussed elsewhere [5-10].

Adder cell is the primary unit of an ALU. Power, speed and area requirements need to be satisfied by the adder cell. The delay in the adder circuit originates from the carry bit calculation. Previous studies used CRA structure in their adder unit [7-10].

Carry ripple adder is the simplest but the slowest adder structure and constructed by cascading full adders (FA) blocks in series. In the CRA technique, a sequential addition is performed from the less significant bit (LSB) to the most significant bit (MSB) using the FA structures. In this addition, the initial carry bit input is taken as zero during the sum of the LSB bit. While performing the sum of the next two bits, the new carry bit which is calculated from the sum of the previous two bits is used here as a carry bit input. This process runs until the sum of the MSB bits is reached, and the carry bit inputs are calculated from the sum of the two previous bits each time. Thus, in order to generate the carry bit input to be used in the sum of the MSB bits, all carry bits, from the LSB bit, have to be calculated. In this carry bit calculation process, a delay occurs and as the size of the processed data grows, this delay also increases in parallel. The worst-case delay of the CRA is approximated by equation 1.

$$t = (n-1)\,t_c + t_s \qquad \text{Eq (1)}$$

t_c stands for the delay through the carry stage of a FA, t_s stands for the delay to compute the sum of the last stage and n stands for the number of bits. The delay of CRA is linearly proportional to the number of bits; therefore the performance of the CRA is limited when the number of bits increases [11].

Other conventional types of adders are carry-look-ahead adder, carry-skip adder, carry select adder, conditional sum adder (COSA), and Manchester Carry Chain adder. In these conventional types of adders including CRA, COSA is the extension of Carry Select Adder and has less delay in its operation because of the carry bit computation method.

The basic idea in the COSA is to calculate two different outputs for a given group of input bits, for instance, n bits. In each calculation, n bits addition result and a carry bit out are obtained. In one of the addition operations, the carry input is taken as zero and the other is taken as one. By using a multiplexer structure, the correct carry input is selected and the correct addition result is obtained through this carry bit selection. Thus, the result is calculated without waiting for the calculation of the carry bit. The addition is much faster as higher bit addition operations [12]. Block diagram of 4 Bit COSA is given in Figure 1 [13].

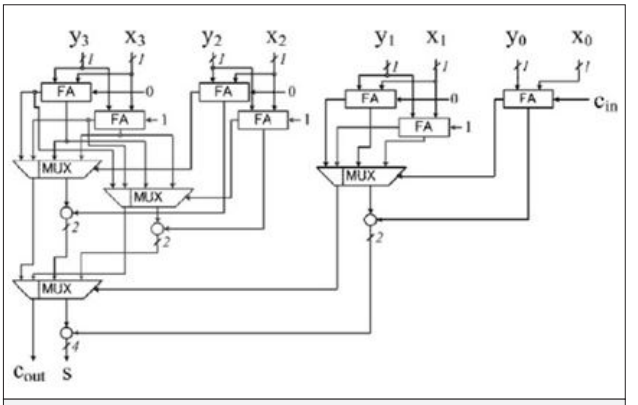

Figure 1. 4 Bit Conditional Sum Adder (COSA)

Material and Method

In the study, the main ALU structure is divided into three subunits as an arithmetic unit, a logic unit, and a shift-rotate unit. Each subunit is introduced as a component to the system. Each component consists of different components.

One of the Altera's FPGA families, Cyclone II EP2C70F896C6 (Intel, Santa Clara, CA, USA) device is targeted in the design platform namely Quartus II (Intel, Santa Clara, CA, USA) and Modelsim-Altera (Intel, Santa Clara, CA, USA) is used as a simulation tool. In EP2C70F896C6 device, 2C means that this device belongs to Cyclone II family, 70F means that this device has approximately 70 thousand logic elements (LEs), 896C refers to the total number of pins both dedicated pins and user pins and last number in the device code refers to the speed grade of this device. In addition to these features, EP2C70F896C6 device includes 250 M4K random access memory (RAM) blocks, approximately 1.1Mbit RAM bits, 150 18x18 embedded multiplier and 4 phase lock loop (PLL) structures [14].

Altera Quartus II software which is developed by ALTERA is the most comprehensive environment available for a programmable chip design. It allows users to design both at gate level and register transfer level (RTL), also allows you to use mega function and intellectual property (IP) and synthesis their HDL files and also you can use this software to implement timing analysis of your design. After the synthesis and analysis of the design with the Quartus II software, the functional and temporal simulation is realized with the use of Modelsim-Altera software.

Simulations can be performed manually and directly via Modelsim-Altera or indirectly by using the testbench file written in Quartus II [15].

In this study we used RTL design which is done with use of VHDL language and wrote a testbench VHDL file for simulation process of the proposed design via Modelsim-Altera.

Design diagram of proposed ALU is given in Figure 2.

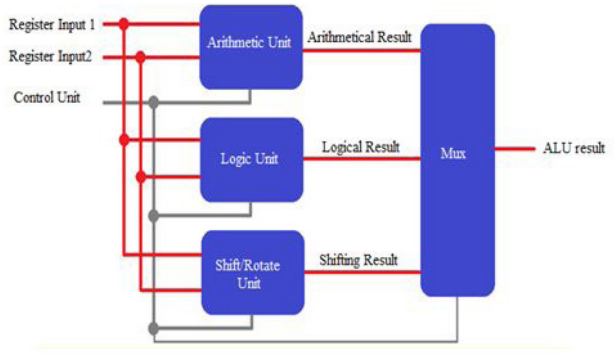

Figure 2. Arithmetic Logic Unit Design Diagram

The source code of design is written with VHDL hardware description language and behavioural and structural modelling is adopted as a modelling method. The design flow is selected as bottom to top.

Arithmetic Unit of proposed design contains signed addition, signed subtraction, signed multiplication, signed division and signed mod operations.

Logical Unit of proposed design contains and, or, xor, not, nand, nor and xnor operations.

Shift/Rotate Unit of proposed design contains arithmetic left and right shifting, logical left and right shifting and right and left rotation operations.

Operations and select lines of proposed ALU is given in Table 1. These 19 operations in the Table were defined as a component in the specific unit where the operation belongs. But each operation could be defined as a procedure, block or function. Each of this structure has different syntax and usage.

After the target device was selected as Cyclone II EP-2C70F896C6, as a first part, arithmetic unit is designed. The arithmetic unit has 4 inputs, namely inpu1, input 2, clk (clock) and ALU control (select input from the control unit of CPU) and 3 outputs namely arithmetic unit out, error (for division errors such as "0/0" and "data/0", overflow errors and size out errors of the multiplication operation) and flag register out (parity, overflow, sign and zero flags). Data inputs and arithmetic unit out are 64 bits long, clock input (in simulation 50MHz clock frequency is used), arithmetic unit control(selection lines) is 3 bits long (first 3 bits of ALU control input) and error output are 1 bit long and flag register output is 4 bits long.

Conditional sum adder which is used in addition operation is the most important part of the arithmetic unit. After the comparison of CRA and COSA structures, COSA is selected as main structure of the addition operation. CRA and COSA simulation result is given in Figure 3 respectively, and delay and LE usage comparison of these two adders is given in Figure 4.

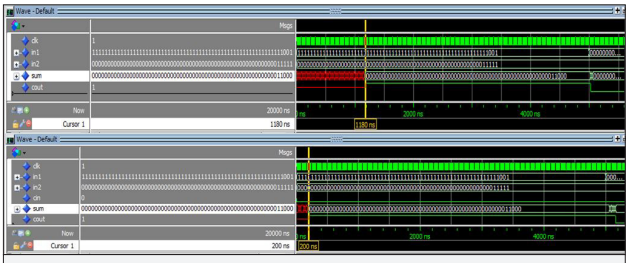

Figure 3. 64 Bit Carry Ripple Adder (CRA) and Conditional Sum Adder (COSA) Simulation Results Respectively

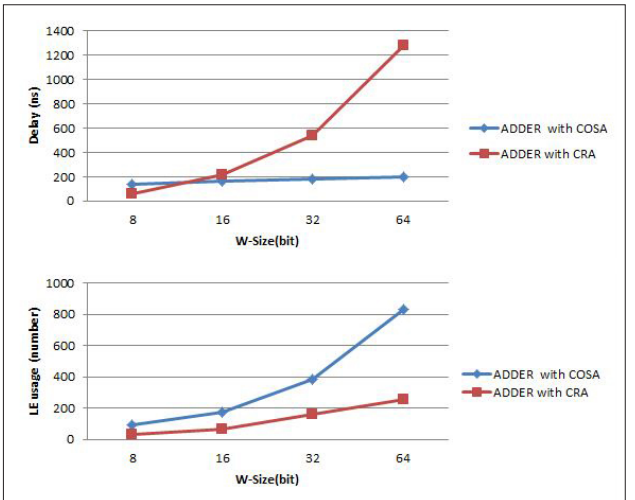

Figure 4. Delay and LE Usage Comparison of CRA and COSA

N bits COSA type addition device is composed of a two-bit COSA consisting of essentially three full adders and a multiplexer structure. One of the full adders collects the first bits of the input data with the "0" carry in. Other two full adders collect the last bits of the input data. One of them with "0" carry in and the other one uses "1" carry in. The selection of the carry-bit which is going to be used in the sum of the last bits is selected by looking at the carry bit result from the sum of the first bits with the usage of multiplexer structure. 64-bit COSA is designed as an extension of two-bit COSA structure. RTL schema of 64 Bit COSA with Overflow Detection component is given in Figure 5.

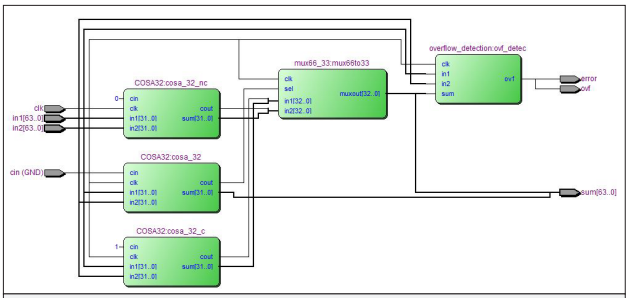

Figure 5. RTL Schema of 64 Bit COSA with Overflow Detection

Table 1. Operations and Select Lines

Function	Operation	Select Lines				
Signed ADD	(±A)+(±B)	0	0	0	0	0
Signed SUB	(±A)-(±B)	0	0	0	0	1
Signed MULT	(±A)*(±B)	0	0	0	1	0
Signed DIV	(±A)/(±B)	0	0	0	1	1
Signed MOD	(±A)mod(±B)	0	0	1	0	0
AND	A and B	0	1	0	0	0
OR	A or B	0	1	0	0	1
XOR	A xor B	0	1	0	1	0
NOT A	not A	0	1	0	1	1
NOT B	not B	0	1	1	0	0
NAND	A nand B	0	1	1	0	1
NOR	A nor B	0	1	1	1	0
XNOR	A xnor B	0	1	1	1	1
Logic left shift	±A sll ±B	1	0	0	0	0
Logic right shift	±A srl ±B	1	0	0	0	1
Arith. left shift	±A sla ±B	1	0	0	1	0
Arith right shift	±A sra ±B	1	0	0	1	1
Left Rotate	±A rotl ±B	1	0	1	0	0
Right Rotate	±A rotr ±B	1	0	1	0	1

A, B: data inputs; ADD: addition; SUB: subtraction; MULT: multiplication; DIV: division; MOD: modular, sll: shift left logical; srl: shift right logical; sla: shift left arithmetical; sra: shift right arithmetical; rotl: rotation to left; rotr: rotation to right

Subtraction component is designed with the usage of COSA.

Another important operation is multiplication operation. The Booth's Algorithm which provides great convenience in two signed number multiplication is used for multiplier component.

In the Table 1, data A and B are both 64 bits long data. In the multiplication operation, first 32 bits of data A and B are used. The multiplication operation in proposed design allows multiplying two 32 bits long data. Also, several functions has been used for checking the data if it is greater than the number which is the biggest number in 32 bit long data or not. These function checks the second 32 bits of 64 bit data. When the data is negative and if there are '0' bits in the second 32 bits of data, these functions tell us that we can't multiply this data due to the size out in the multiplication result, and this process works in positive numbers differently.

A Similar algorithm to the multiplication algorithm is used in division component design.

The last component of the arithmetic unit is a modular component and it is designed with the usage of the division component. The only difference is that the remainder of the division operation is taken as an output of the component.

After components of all operations are defined, these components are called under the arithmetic unit. The output of the arithmetic unit is taken as the output of the multiplexer structure according to the value of the selection input which is related to the ALU control input port. After the source code of the arithmetic unit was written, the design is analysed and synthesized with the help of the Altera Quartus II v13.0sp1 software. RTL schema of 64 Bit Arithmetic Unit is given in Figure 6.

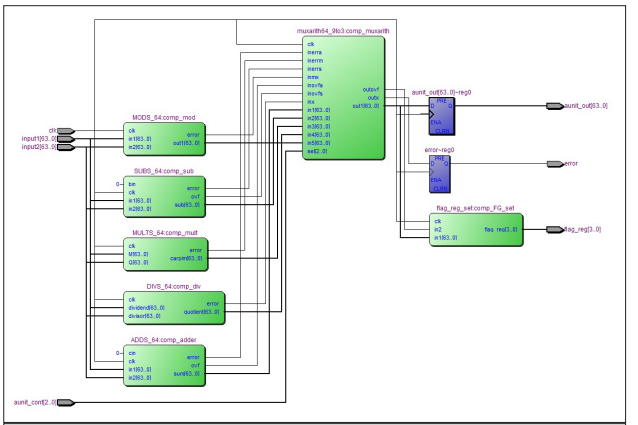

Figure 6. RTL Schema of 64 Bit Arithmetic Unit

64 Bit Arithmetic unit's simulation is implemented with the help of Modelsim- Altera v10.1d software. The simulation results of this unit are shown Figure 7 and Figure 8.

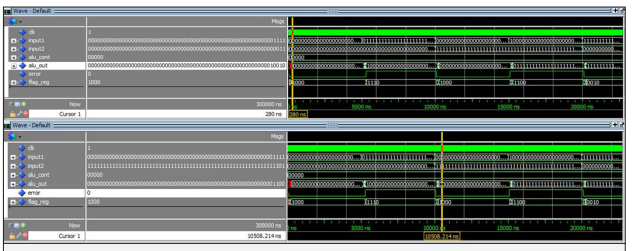

Figure 7. Positive Simulation Results of the 64 Bit Arithmetic Unit

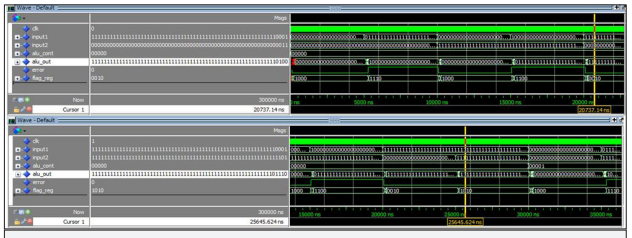

Figure 8. Negative Simulation Results of the 64 Bit Arithmetic Unit

Logic Unit and Rotate/Shift Unit which are second and third parts of ALU are designed respectively. RTL schema of Logic Unit is given in Figure 9. After the source code of the logic unit was written, the design is analysed and synthesized. The simulation result of Logic Unit is shown in Figure 10. 64 Bit Rotate/Shift Unit's RTL scheme is shown in Figure 11. After the source code of the Rotate/Shift unit was written, the design is analysed and synthesized. The simulation result of this unit is shown in Figure 12.

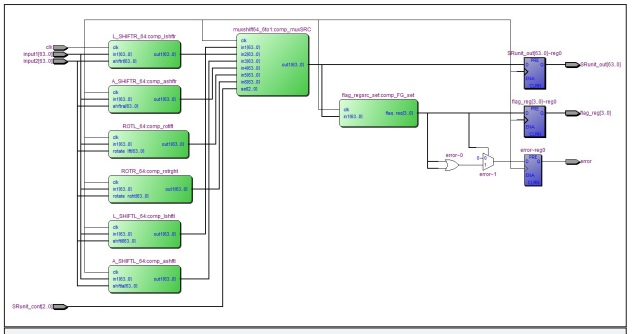

Figure 9. RTL Schema of 64 Bit Logic Unit

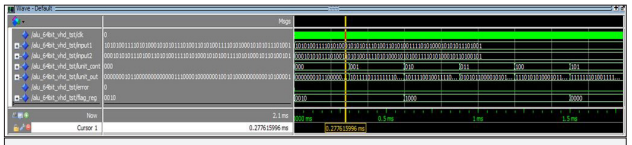

Figure 10. Simulation Result of the 64 Bit Logic Unit

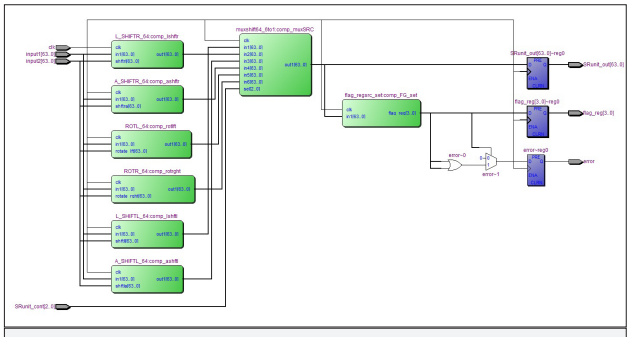

Figure 11. RTL Schema of 64 Bit Rotate/Shift Unit

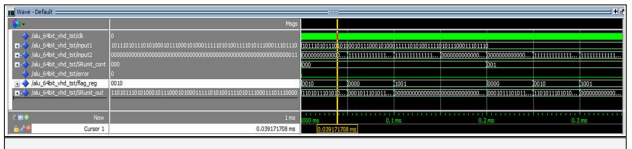

Figure 12. Simulation Results of 64 Bit Rotate/Shift Unit

These three subunits are defined as a component and called under the Arithmetic Logic Unit. The outputs of these subunits supply a multiplexer structure defined in the top-level design. Last 2 bits of ALU control input port is used as a select line and this select line supply the multiplexer selection inputs. These two bits should be "00" when we want to activate Arithmetic Unit, "01" when we want to activate Logic Unit and "10" when we want to activate Shift/rotate unit.

Arithmetic Logic Unit Output is taken from the output of the multiplexer structure according to the value of the selection input of the top-level multiplexer structure which is related to the last two bits of ALU control input port. Flag register output from MSB bit to LSB bit defines respectively parity flag, an overflow flag, sign flag, and Zero flag.

In the last case, the Arithmetic Logic Unit is defined as a single component in the most-level design and can be called and executed as a component in any design. Top-level design of 64 Bit Arithmetic Logic Unit's RTL scheme is shown in Figure 13.

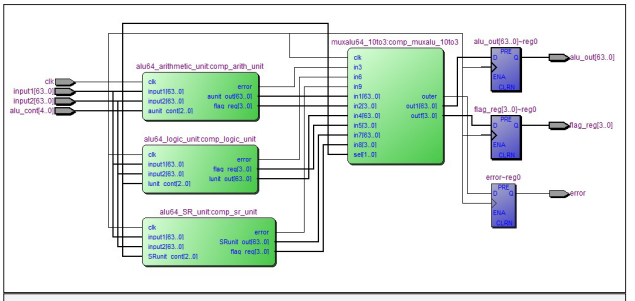

Figure 13. RTL Schema of 64 Bit Arithmetic Logic Unit

The top-level, Arithmetic Logic Unit, module is analysed and synthesized and then simulated with the help of Modelsim-Altera software. 64 Bit Arithmetic Logic Unit's compilation report is given in Figure 14.

Analysis & Synthesis Summary	
Analysis & Synthesis Status	Successful - Wed Dec 05 23:06:10 2018
Quartus II 64-Bit Version	13.0.1 Build 232 06/12/2013 SP 1 SJ Web Edition
Revision Name	alu_64bit
Top-level Entity Name	alu_64bit
Family	Cyclone II
Total logic elements	24,619
Total combinational functions	23,939
Dedicated logic registers	2,893
Total registers	2893
Total pins	203
Total virtual pins	0
Total memory bits	399
Embedded Multiplier 9-bit elements	0
Total PLLs	0

Figure 14. Compilation Report of 64 Bit ALU

Results

The 64-bit arithmetic logic unit for signed numbers processing is designed using VHDL language and synthesized using Altera Quartus II v13.0sp1 platform. The ALU is implemented us-

Table 2. Comparison between previous studies and proposed design

Design	Operation (number)	FPGA Family	Data Type	Clock Rate (Hz)	Adder Type	Delay on Adder (ns)
Previous studies	Max. 16	Xilinx FPGAs	Unsigned	Max. 10 MHz	CRA or CLA	Min. 5900
Proposed Design	19	Altera Cyclone II	Signed	50 MHz	COSA	280

FPGA: Field Programmable Gate Arrays; Hz: hertz; MHz: megahertz; ns: nanosecond; CRA: Carry Ripple Adder; CLA: Carry Look-ahead Adder; COSA: Conditional Sum Adder

ing parallel implementation of three different subunits which perform various functions such as arithmetic, logical, shift and rotate operations. At first step components of subunits are designed to handle unsigned numbers. Then with the use of process structures these components are arranged to handle signed numbers. After this arrangement, the overflow control circuit is designed.

Data are received from the data input ports and these data fed to the three different subunits. These subunits calculate their result in each clock cycle and send them into top-level multiplexer structure. This multiplexer structure generates an output according to the value of the signal from the control unit which is defined as an input port named ALU control. This generated outputs from the multiplexer fed to the output ports of ALU. The synthesized most-level module is targeted to Cyclone II device.

The most level design has 4 input ports as two data input, a clock input and select input which is assumed to come from the control unit of CPU and has 3 output ports as ALU operation output, error output, and flag register output.

50 MHz clock is used as clock input in testbench simulation. Clock frequency can be increased up to 250 MHz with the PLL structure usage. Error output port shows errors which occurs in signed addition and subtraction when overflow occurs and incorrect result calculated, in multiplication of two numbers which are exceeding the maximum value expressed in 32 bits and in division operation when data inputs are selected as both zero or second input is selected as zero (these selections causes "0/0" uncertainty and "number/0" undefined state). Flag register output is 4 bits long and shows from MSB bit to LSB bit respectively parity flag status, overflow flag status, sign flag status, and zero flag status.

After testbench simulation, the first result of The ALU is taken after 280 ns. This operation is signed addition operation. Some of the simulation results of the 64 Bit Arithmetic Logic Unit are shown in Figure 15. After the simulation was completed, the results obtained from the Altera Quartus II Design Suit were confirmed by the theoretical results for all the operations with signed numbers and we found that they matched the theoretical values.

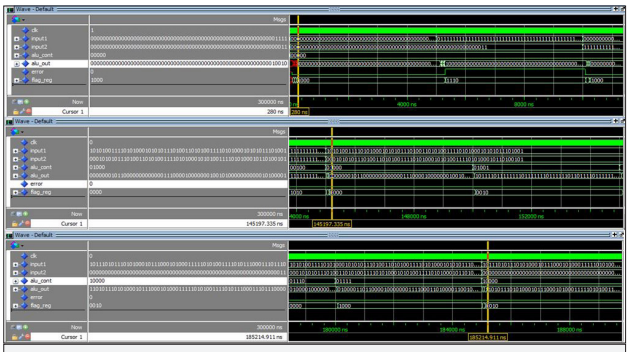

Figure 15. Simulation Results of 64 Bit ALU

Conclusion

In the addition operation, instead of CRA or CLA type of adder, the usage of COSA structure reduced the delay which consists of carry bit calculation. As a result, the output of the addition operation was obtained in a shorter time (adder with COSA is approximately 6 times faster than adder with CRA). In spite of this positive development - the increase of the multiplexer structures used in the addition circuit caused the number of logic elements used in the FPGA increase.

The 64-bit arithmetic logic unit which is designed for the processing of signed numbers has been successful in all operations regardless of whether the number is positive or negative. In case of overflow in the addition and subtraction operations, indefinite and undefined situations occurring in the division process and the result of multiplication operation exceeding 64 bits, errors are shown successfully with the error output as a result of the simulation.

The design is shaped around the "component" structure in the VHDL language. The usage of this structure has enabled us to manage our design easily and make the design simpler. In addition, all "components" can be easily used in other designs because of the special benefit of the component structure in the VHDL language. The most important disadvantage of the usage of these structures is the calculation of all operation results regardless of the process priority and this causes extended simulation time. The design can be implemented using "procedure" structures with a different approach. But with the usage of this structure, the size of the source code will increase

and the readability will decrease and the design will be complicated.

Therefore, the structure to be used should be chosen according to the purpose. The main reason for us to use the "component" structure in our design is to eliminate some of the complexity resulting from the use of signed numbers which caused the addition of new structures to the design, the number of operation and the large size of the processed data. Comparison between previous studies and proposed design is given in Table 2. If the clock rate of proposed design is lowered to 10 MHz, delay on the adder unit will be 1400ns, and this delay is also lower than delay on the adder with CRA or CLA structure in previous studies. Also, when we use the PLL structure in the FPGA, clock frequency can increase up to 250 MHz and delay in the adder operation can decrease down to 60 ns.

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ISTANBUL UNIVERSITY CERRAHPASA

RESEARCH ARTICLE

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Performance Analysis of a Secondary User in Cognitive Radio over Generalized-Gamma Fading Channels

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ABSTRACT

In this paper, the performance of a secondary user (SU) in an underlay cognitive radio (CR) network over a generalized-gamma (GG) fading channel in terms of three performance metrics, namely, outage probability, ergodic capacity, and bit error rate (BER), is investigated. According to the underlay approach, the transmit power of the SU should be limited to avoid interference to primary users (PUs). The performance metrics of the SU in the underlay CR network are theoretically derived and also obtained with Monte Carlo simulations for a GG fading channel with different fading parameters. To demonstrate the effect of limited power on the performance metrics, three different maximum transmit power levels (P_{max}), namely, 10, 20, and 30 dB, are used. The simulation results lead to three conclusions: First, when high values are chosen for the fading parameters (α, c), the fading channel gets less distorted and the performance metrics improve. The second conclusion is that the BER performance gets better as the limited power increases. The final conclusion is that the BER performance of SUs improves as the interference power that PUs can tolerate increases..

Keywords: Cognitive radio, generalized-gamma fading channel, underlay approach.

Introduction

Cognitive radio (CR) was proposed by Mitola afforded an opportunity for unlicensed users to efficiently use the spectrum without any destructive effect on licensed users [1, 2]. A large number of authors have been studying the CR concept to cope with the spectrum scarcity problem due to the increasing demand for wireless communications and the use of new-generation communication systems [3, 4]. There are three different approaches in CR: underlay, overlay, and interweave. In the underlay approach, while both licensed (primary) and unlicensed (secondary) users simultaneously transmit their signals, the transmission power of secondary users (SUs) is limited within a predefined threshold. Therefore, they do not have any disruptive effect on primary users (PUs). However, in the interweave approach, SUs need to seek an opportunity to exploit the spectrum when it is not being utilized by PUs. Finally, in the overlay approach, PUs and SUs behave as partners and PUs share their transmission parameters (e.g., modulation settings) with SUs. This approach can be practical for an operator-aided CR network, where all the SUs and PUs are serviced by the same operator.

Recently, the generalized-gamma (GG) fading channel, which covers a large number of well-known fading channel models, has become popular, and many researchers have been studying the wireless system performance over this type of channel [5-10]. In [5], in 2005, Aalo et al. studied the bit error rate (BER) of modulation schemes in GG channels. Then, in 2009, Malhotra et al. investigated the receiver performance over GG fading channels and derived the analytical BER results for M-ary phase-shift keying (M-PSK) and M-ary quadrature amplitude modulation (M-QAM) schemes using moment-generating function (MGF) approach and Padé approximation technique [6]. Later, in 2011, Gazi derived the upper bounds for outage probability and MGF [7]. A cognitive relay network was studied in [8] and the outage probability was derived for different tolerable interference levels. Additionally, in [9], outage probability was studied for a dual-hop decode-and-forward relay over a GG fading channel. In 2015,

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physical layer security was studied over a GG fading channel in [10]; further, the channels between the receiver and an eavesdropper, as well as that between the receiver and transmitter, were characterized with different GG fading parameters. The outage probability of a cognitive relay network under interference constraints was studied in [11, 12]. A multiple-input multiple-output cognitive relay network, which uses an underlay approach, was considered in [11], and the outage/error performance analysis was presented by means of closed-form expressions over Rayleigh fading channels. The same scenario is also analyzed over composite asymmetric multipath/shadowing fading channels in [12]. Moreover, the outage performance of cognitive DF relay networks for nonidentical independent Rayleigh fading channels, nonidentical interference power limits of PUs, and nonidentical maximum transmission power limits of SUs have been analyzed in [13,14,15]. A similar work is also presented in [16] involving cognitive AF relay networks.

In this paper, it is assumed that the CR network employs the underlay approach; therefore, the transmit power of SUs is limited to guarantee that SU transmission is not harmful to PU transmission. The channels between the SU transmitter and SU receiver, as well as those between the SU transmitter and PU receiver, are modeled with GG fading distribution. Simulations are performed for various values of the fading parameters of the GG fading distribution. The contribution of this study is the investigation of the effect of limited SU power on the BER performance as well as on ergodic capacity over a GG fading channel, which is not represented in earlier studies.

This paper is organized as follows. Section 2 describes the system model under consideration. Section 3 presents the analysis of outage probability, ergodic capacity, and BER performance. Section 4 provides the simulation results. Finally, the paper concludes with Section 5.

System Model

The CR network model under consideration is shown in Figure 1. While the transmitter of the SU is denoted by SU_{TX}, the PU and SU receivers are denoted by PU_{RX} and SU_{RX}, respectively. Each node has a single antenna. The transmit power of the SU, P_s, is determined by $P_s = \min\left(\frac{Q_p}{E\left\{\left|h_{SU,TX\to PU,RX}\right|^2\right\}}, P_{max}\right)$, where Q_p and P_{max} denote the maximum tolerable interference level and maximum transmit power level, respectively. $h_{SU,TX\to PU,RX}$ represents the fading channel information between SU_{TX} and PU_{RX}. The transmission channel is modeled as a GG random variable. The GG distribution is given by [7, 10]

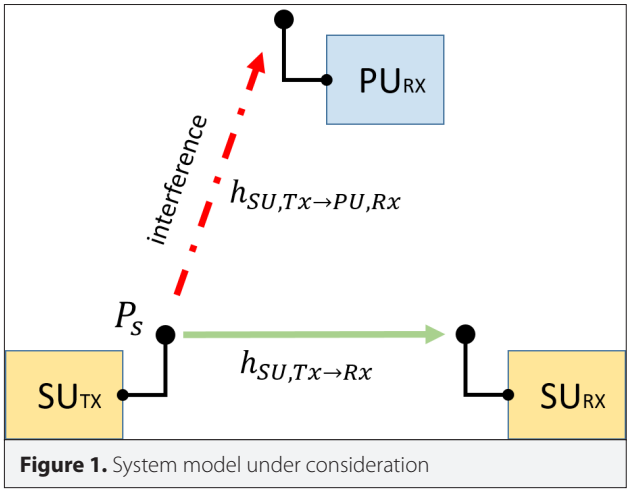

Figure 1. System model under consideration

$$f_R(r) = \frac{\alpha c^c r^{\alpha c-1}}{\Gamma(c)\bar{r}^{\alpha c}} \exp\left(-c\left(\frac{r}{\bar{r}}\right)^{\alpha}\right),\ \alpha > 0, c > 0, \tag{1}$$

where α denotes the fading parameter; c and $\bar{r}$ represent the normalized variance and α-root mean value of the channel envelope R, respectively. Finally, $\Gamma(c) = \int_0^\infty t^{c-1}e^{-t}dt$ is the well-known gamma function. A GG fading channel can be transformed into other distributions through the use of different fading parameters and variance values. Table 1 lists the corresponding distributions of a GG fading channel with different α and c values.

Because the fading channel is modeled as GG, the probability density function and cumulative distribution function (CDF) of the signal-to-noise ratio (SNR) is expressed as [10]

$$f(\gamma) = \frac{\alpha c^c \gamma^{\alpha c/2-1}}{2(\bar{\gamma})^{\alpha c/2}\Gamma(c)} \exp\left(-c\left(\frac{\gamma}{\bar{\gamma}}\right)^{\alpha/2}\right), \tag{2}$$

$$F(\gamma) = \frac{\Upsilon\left(c, c\left(\frac{\gamma}{\bar{\gamma}}\right)^{\alpha/2}\right)}{\Gamma(c)} \tag{3}$$

where $\Upsilon(\alpha, x) = \int_0^x e^{-t}t^{\alpha-1}dt$ is the lower incomplete gamma function, as defined in [17, Eq.(8.350/1)]. SNR is expressed as

$$\gamma = \min\left(\frac{Q_p}{E\left\{\left|h_{SU,TX\to PU,RX}\right|^2\right\}}, P_{max}\right)|h_{SU,TX\to SU,RX}|^2, \tag{4}$$

where $h_{SU,TX\to SU,RX}$ denotes the fading channel information between SU_{TX} and SU_{RX}. Let x_s denote the transmitted symbol of the SU. The received signal at the SU receiver can be expressed as

$$y = P_s h_{SU,TX\to SU,RX} x_s + n_s, \tag{5}$$

where n_s denotes the complex additive white Gaussian noise (AWGN) with zero mean and unit variance *CN(0, No/2)*. Here the interference of PU on the SU is neglected.

Table 1. Various *α* and *c* values of a GG fading channel

α[1]	*c*[2]	Corresponding Distributions
2	1	Rayleigh
2	*c*	Nakagami-m
α/2	1	Weibull

α[1]Denotes a GG fading parameter
c[2]Represents the normalized variance of a GG channel envelope

Performance Analysis

In this paper, the outage probability, ergodic capacity, and BER for the SU are analyzed. These performance metrics are derived for the considered scenario in GG channels.

Outage Probability

One of the important performance criteria is the outage probability. It can be easily obtained from

$$P_{out} = p(\gamma \le \gamma_{thr}) = \int_0^{\gamma_{thr}} f_\gamma(\gamma) d\gamma, \quad (6)$$

where γ_{thr} denotes the predefined threshold value. In GG fading channels, the outage probability can be calculated by using the CDF of SNR, which is given in Eq.(3). In [10], the lower incomplete gamma function is given in the form of Meijer's G-function [17, Eq.(9.301)] as

$$\Upsilon\left(c, c\left(\frac{\gamma}{\bar{\gamma}}\right)^{\alpha/2}\right) = \frac{\Gamma(c+1)}{\Gamma(c)c}\left(c\left(\frac{\gamma}{\bar{\gamma}}\right)^{\alpha/2}\right)^c G_{1,2}^{1,1}\left[c\left(\frac{\gamma}{\bar{\gamma}}\right)^{\alpha/2}\middle|\begin{matrix}1-c\\0,c\end{matrix}\right]. \quad (7)$$

By using Eq.(7), the outage probability can be calculated for GG fading channels.

Ergodic Capacity

The well-known capacity equation is given in Eq.(8):

$$C = \mathrm{E}\left[\log_2(1+\gamma)\right], \quad (8)$$

where γ represents the SNR value of the SU, which depends on the random fading channel. By using Jensen's inequality, the upper bound of Eq.(8) can be expressed as

$$C \le \log_2(1+\bar{\gamma}), \quad (9)$$

where $\bar{\gamma}$ represents the average SNR. By using Meijer's G-function representation of $F_\gamma(\gamma)$ in Eq.(7), $\bar{\gamma}$ can be calculated as

$$\bar{\gamma} = \int_0^\infty (1 - F(\gamma)) d\gamma = \int_0^\infty \left(1 - \Upsilon\left(c, c\left(\frac{\gamma}{\bar{\gamma}}\right)^{\alpha/2}\right)\right) d\gamma. \quad (10)$$

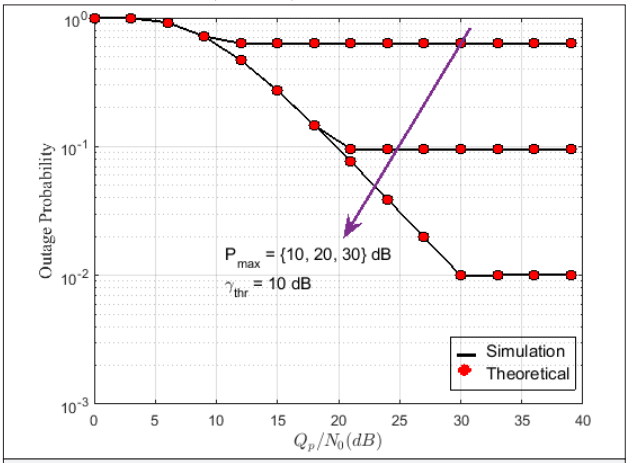

Figure 2. Outage probability vs. $\bar{Q}_p$ for different P_{max} values over a Rayleigh fading channel (a_s=2, a_d=2 c=1)

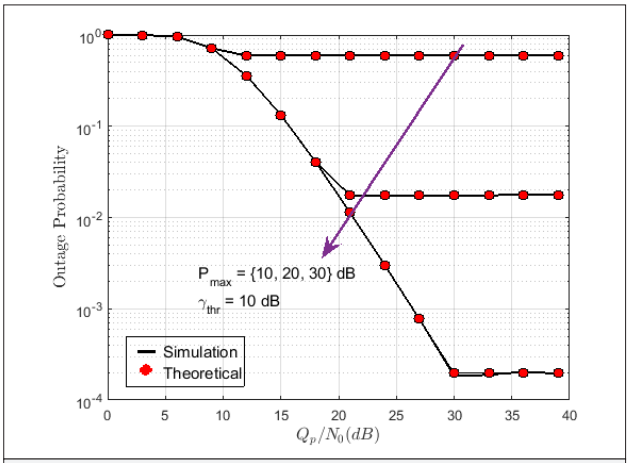

Figure 4. Outage probability vs. $\bar{Q}_p$ for different P_{max} values over a Nakagami fading channel (a_s=2, a_d=2 c= 2)

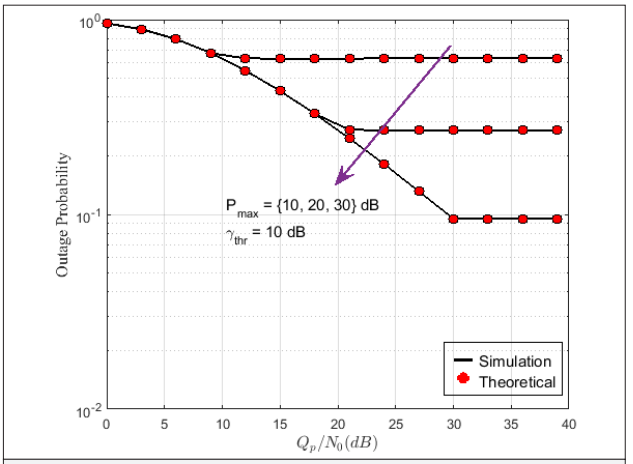

Figure 3. Outage probability vs. $\bar{Q}_p$ for different P_{max} values over a GG fading channel (a_s=1, a_d=1 c=1).

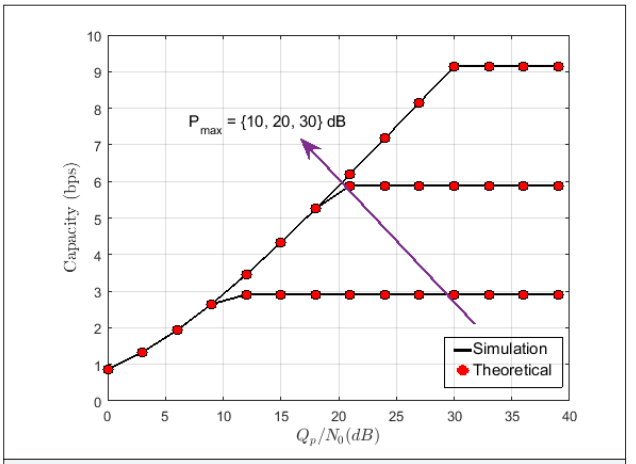

Figure 5. Capacity variation vs. $\bar{Q}_p$ for different P_{max} values over a Rayleigh fading channel (a_s=2, a_d=2, c=1)

When the fading parameters are chosen as a_s=2, a_d=2, and c=1, the GG fading channel turns into a Rayleigh channel, and therefore, the capacity can be calculated as

$$C = \frac{1}{\ln 2}\int_x^\infty \frac{e^{-t}}{t}dt. \quad (11)$$

The theoretical curve is only given for the Rayleigh fading case (a_s=2, a_d=2, and c=1). For the other cases, the capacity results are obtained with Monte Carlo simulations.

Bit Error Rate Analysis

In the system model under consideration, the average BER can be calculated by averaging over the fading channel:

$$\bar{P}_E = \int_0^\infty P_E(\gamma) f_\gamma(\gamma)\,\mathrm{d}\gamma\,, \quad (12)$$

where $P_E(\gamma) = \frac{\Gamma(b, a\gamma)}{2\Gamma(b)}$ denotes the conditional BER in the AWGN channel [18, Eq.(8.100)]. Further, a and b values depend on the modulation type and demodulation process. For BPSK modulation and coherent detection, $a = 1$ and $b = 0.5$. The average BER is obtained from [5]:

$$\bar{P}_E = A(\mathrm{k},\mathrm{l})\,\mathrm{G}_{2l,k+l}^{k,2l}\left[\left(\frac{l\beta}{k^{k/l}a\bar{\gamma}}\right)^{l}\middle|\begin{matrix}\alpha_1,\mathrm{K}\,,a_{2l}\\ \beta_1,\mathrm{K}\,,\beta_{k+l}\end{matrix}\right], \quad (13)$$

where

$$\alpha_n = \begin{cases} 1-\frac{n+b-1}{l} & n = 1,2,\mathrm{K}\,,l \\ 1-\frac{n-l-1}{l} & n = l+1, l+2,\mathrm{K}\,,2l \end{cases}, \quad (14)$$

and

$$\beta_n = \begin{cases} \frac{n+c-1}{k} & n = 1,2,\mathrm{K}\,,k \\ 1-\frac{n-k}{l} & n = k+1,\ k+2,\mathrm{K}\,,\mathrm{k}+l \end{cases}. \quad (15)$$

Moreover, $\beta = \frac{\Gamma(c+2/\alpha)}{\Gamma(c)}$ and $\alpha/2 = l/k$.

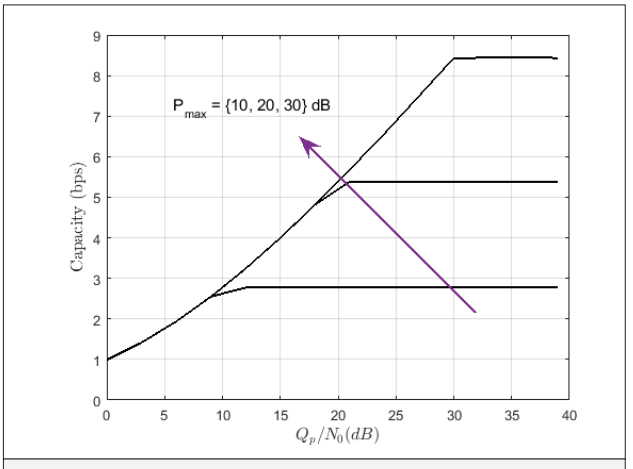

Figure 6. Capacity variation vs. $\bar{Q}_p$ for different P_{max} values over a GG fading channel (a_s=1, a_d=1, c=1)

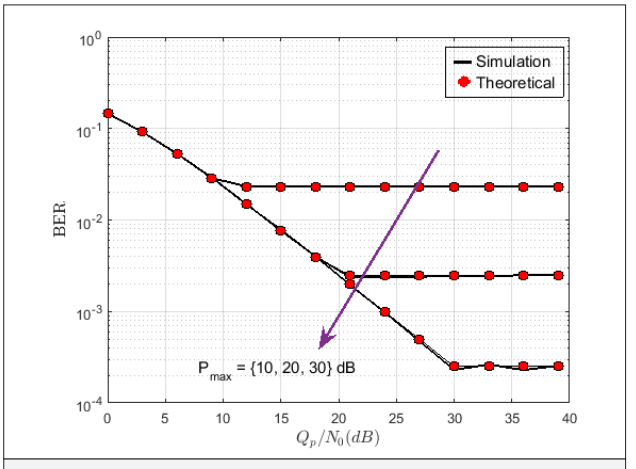

Figure 8. Bit error probability vs. $\bar{Q}_p$ for different P_{max} values over a Rayleigh fading channel (a_s=2, a_d=2, c=1)

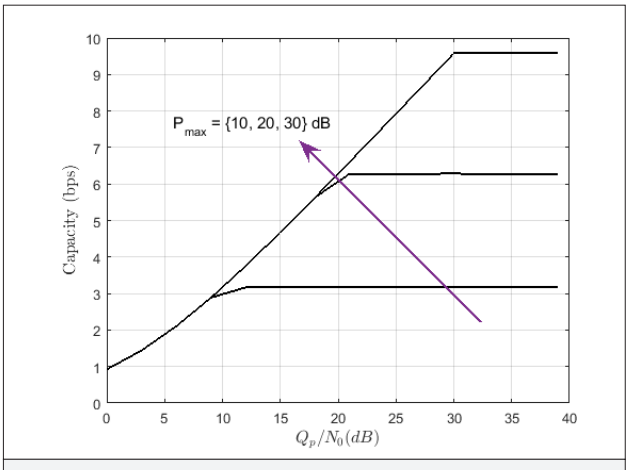

Figure 7. Capacity variation vs. $\bar{Q}_p$ for different P_{max} values over a Nakagami fading channel (a_s=2, a_d=2, c=2)

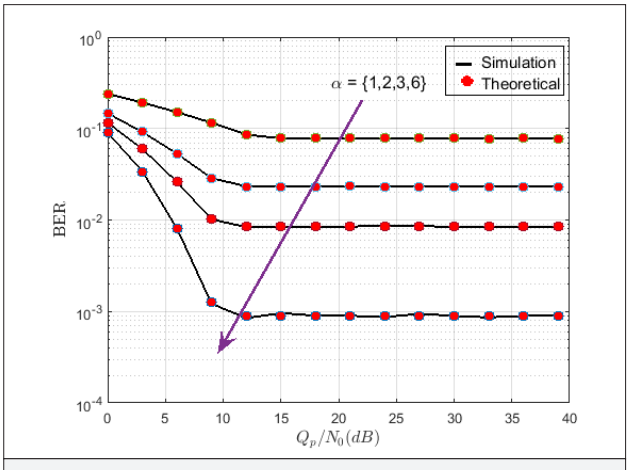

Figure 9. Bit error probability for various a fading parameters (P_{max}=10 dB, c=1)

Simulation Results

In this section, the outage probability, capacity, and BER performance of the SU in the underlay CR network are investigated. In all the simulations, it is assumed that the SU's modulation type is BPSK, $N_0 = 1$, and the tolerable interference-to-noise ratio $\bar{Q}_p = Q_p / N_0$ changes from 0 to 40 dB. However, the SU's power is limited to $P_{\max}$ to avoid causing interference to the PU. In the simulations, three different $P_{\max}$ values are considered, namely, P_{max}={10, 20, 30} dB. All the simulations are performed by using Monte Carlo with 10^6 iterations (except for the last one, which is obtained with 10^7 iterations) using MATLAB (MathWorks, Natick, Massachusetts, U.S.A). The outage probability, capacity, and BER performance are investigated for various α values (α=1, 2, 3, and 6). To simplify the notation, the α values of $h_{SU,TX \to PU,RX}$ and $h_{SU,TX \to SU,RX}$ are represented as α_d and α_s (α_d, α_s), respectively.

Outage probability, capacity, and BER performance are obtained for different $\bar{Q}_p$ and $P_{\max}$ values. First, theoretical and simulation outage probability values are shown in Figure 2, Figure 3, and Figure 4 for various channel fading parameters. When the fading channel parameters are chosen as α_s=2, α_d=2, and c=1 (Figure 2), the GG fading channel turns into a Rayleigh fading channel. In addition, Figure 4 shows the outage probability over a Nakagami-m fading channel (α_s=2, α_d=2, and c=2). In all these figures, the threshold value γ_{thr} is chosen as 10 dB. It is clear that the theoretical results match very well with the simulation curves. As the transmission power increases, the outage probability improves. The worst outage probability is obtained in Figure 3, because the channel fading effect is severe as compared to those of the analyzed channels shown in Figure 2 and Figure 4. The lowest outage probability value is obtained as almost 10^{-2} for the Rayleigh fading channel, while this value is close to 10^{-4} for the Nakagami fading channel when P_{max}=30 dB.

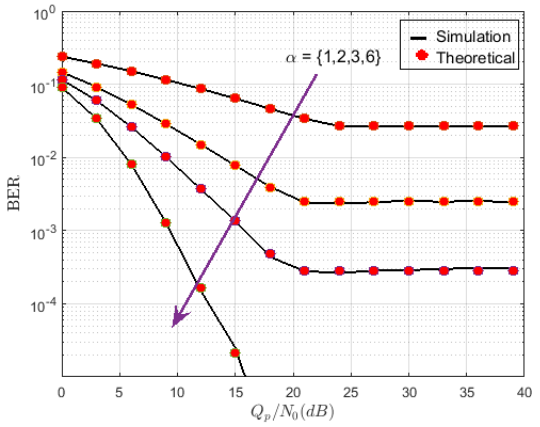

Figure 10. Bit error probability for different fading parameters (P_{max}=20 dB, c=1)

Figure 5 shows the capacity variations for different $P_{\max}$ values in a Rayleigh fading channel (α_s=2, α_d=2, and c=1). As shown in the figure, for all the $P_{\max}$ values, the capacity first increases as $\bar{Q}_p$ increases and then it saturates when it reaches the predefined threshold value. The theoretical capacity values perfectly match with the simulation results for all the $P_{\max}$ values.

Figure 6 and Figure 7 show the capacity performance of SUs in different fading channels. Evidently, when the c value is 2 instead of 1, higher capacity values can be reached. Further, when all the fading parameters are 1, the worst channel is obtained. For example, when $P_{\max}$ is selected as 30 dB, while the capacity value equals 7 bps at 25 dB (Figure 6), the capacity equals 8 bps at the same $\bar{Q}_p$ value (25 dB) (Figure 7).

Finally, the theoretical and simulation BER results are given for different α fading channel parameters and various maximum limited transmit power values. In all the simulation setups, the simulated BER results perfectly match with the theoretical results. First, the channel parameters are chosen as α_s=2, α_d=2, and c=1 (Rayleigh fading), and the BER results are obtained both via simulation and analysis. These results are shown in

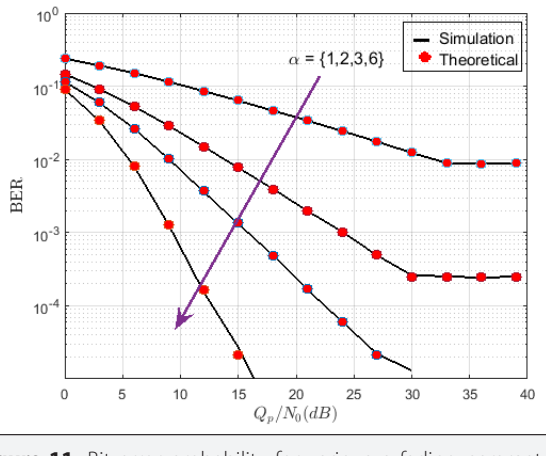

Figure 11. Bit error probability for various α fading parameters (P_{max}=30 dB, c=1)

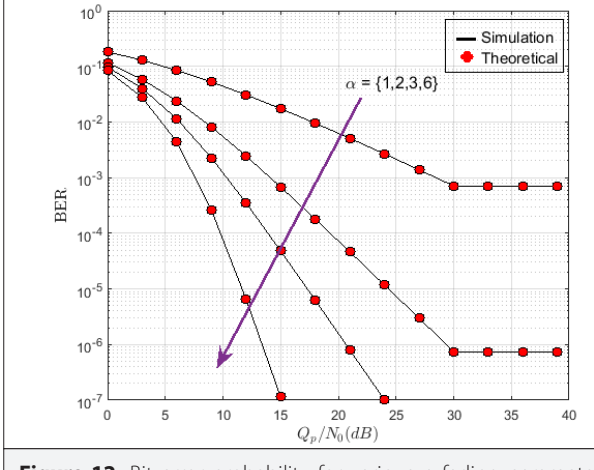

Figure 12. Bit error probability for various α fading parameters (P_{max}=30 dB, c=2)

Figure 8. As expected, for P_{max} =30 dB, the BER performance remarkably improves. All the BER curves perform almost the same until $\bar{Q}_p = 10dB$; then, the smallest P_{max} value (P_{max} =10 dB) is saturated. At $\bar{Q}_p = 18dB$, the BER performance for P_{max} =20 dB is saturated. The BER value at this saturation point is 0.0024. For P_{max} =30 dB, the curve outperforms P_{max} =10 and 20 dB. In Figures 9–11, it is assumed that c =1 and α values are set to α ={1, 2, 3, 6} to evaluate the BER performance with various limited SU transmit power (P_{max}) values. The dominant effect on BER depends on the selection of P_{max}. In Figure 12, c is set to 2. Evidently, as α increases, the BER performance significantly improves. To determine the effect of c on the BER performance, Figure 11 and Figure 12 can be compared. Evidently, while the SNR gap equals 12 dB at BER=10^{-2} when α=1, this gap equals 9 dB at BER=10^{-3}. The SNR gap decreases with increasing α.

Conclusion

In this paper, the outage probability, ergodic capacity, and BER performance of SUs over a GG fading channel in the underlay CR system are investigated. The closed-form expressions are also given, and the obtained results closely match with those obtained from the simulations. Because of the limited transmit power of SUs, the performance indicators, namely, outage probability, BER, and ergodic capacity, saturate with the P_{max} value. When this limited power is increased, all the performance metrics improve.

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ISTANBUL UNIVERSITY CERRAHPASA

RESEARCH ARTICLE

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Effects of RTV Coating on the Discharge Characteristics of A Suspension Glass Insulator

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ABSTRACT

The present study shows the effects of room temperature vulcanizing (RTV) silicone rubber high voltage insulator coatings on the discharge characteristics of a cap-and-pin type suspension glass insulator. The study covers both laboratory investigations and 3D electric field analysis, considering the coated and uncoated glass insulators. An ultraviolet corona camera is used to detect the location of the discharges, and a partial discharge test system is used to obtain the discharge patterns and pulse magnitudes. The experimental work is only conducted for 50 Hz power frequency voltage. In addition to the laboratory investigations, 3D electrostatic field analysis is performed to determine how the RTV coatings on the glass insulators affect the field distributions.

Keywords: RTV coating, Partial discharge, Electric field

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Introduction

Pollution is a common problem especially for outdoor high voltage insulators, operated near industrial regions, as well as coastal areas. Pollution-related problems are frequently observed for the conventional porcelain and/or glass insulators due to their hydrophilic surface properties. Several solutions have been developed to eliminate or to at least minimize the pollution-related problems for conventional insulators. Using silicone rubber insulators and applying room temperature vulcanizing (RTV) silicone rubber high voltage insulator coating (HVIC) to the porcelain and glass insulators are the main solutions to improve the pollution performance of outdoor high voltage insulation systems [1-5].

RTV silicone rubber coatings have gained considerable interest to increase the pollution performance of conventional outdoor porcelain and glass insulators. The first field trial and the first large-scale applications of RTV coatings were conducted in 1973 and 1987, respectively [1-5].

Owing to the hydrophobic surface feature, RTV coatings suppress the leakage current, and therefore the flashover due to the pollution, which is the most important property of the coatings [6]. Many studies have been conducted on the suppression ability of the RTV coatings on the development of the leakage current by using several accelerated weathering tests. Salt-fog tests and rotating wheel tests are the beneficial tests to characterize the RTV coating materials [7-10]. The available researches related to RTV coatings are mainly concentrated on the hydrophobicity, and therefore, the suppression ability of RTV coatings upon the leakage current developments along the insulators.

It is known that electrical discharges become an important design factor not only due to the losses but also due to the electromagnetic interferences, commonly known as radio interferences [11]. The basic motivation of the present study is that there is a limited research about the effects of RTV coatings on the discharge characteristics of suspension insulators. As indicated in reference [12], audible noise from the towers located in the vicinity of residential areas can be extremely annoying to residents especially in case of fog and/or dew weather conditions, and RTV coatings can reduce the noise level.

In the present study, the effects of RTV silicone coatings on the discharge characteristics of cap-and-pin type suspension glass insulators are investigated by using laboratory tests, as well as 3D electrostatic field analysis. An ultraviolet (UV) corona camera is used to detect both the location of the discharges and the number of pulses due to the discharges. Moreover, a partial discharge (PD) detector is

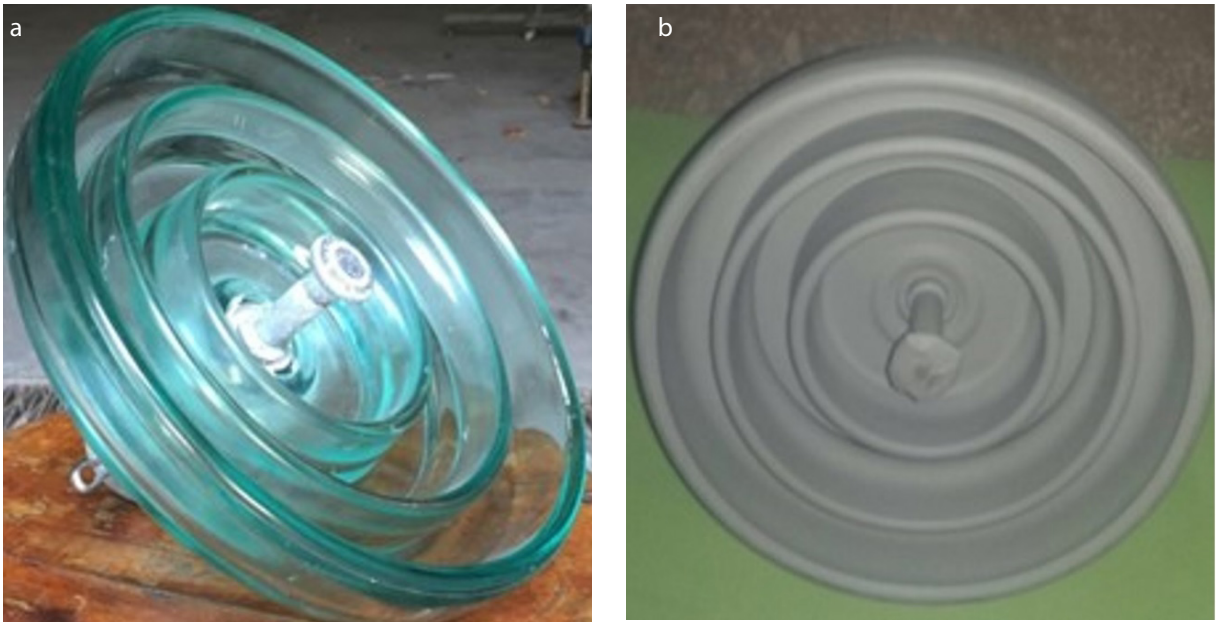

Figure 1. a, b. Uncoated glass insulator unit (a), RTV-coated glass insulator uni (b)

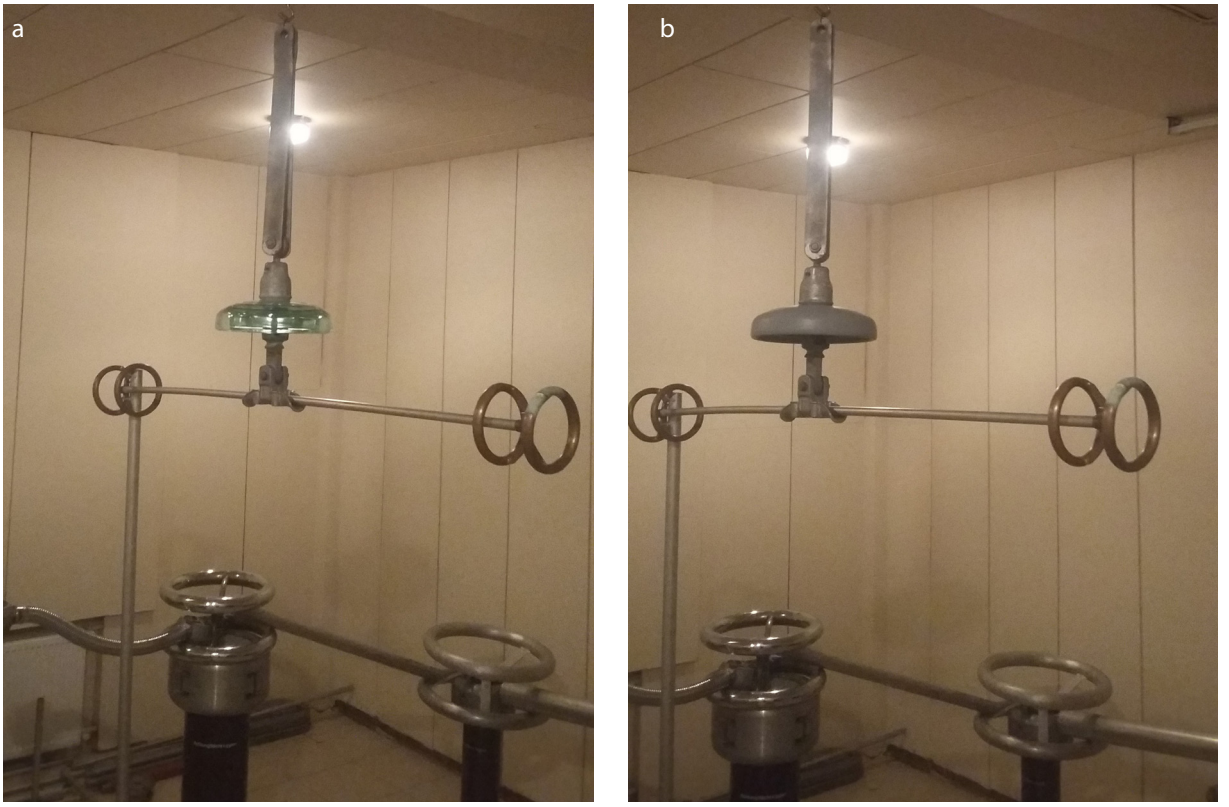

Figure 2. a, b. Laboratory test setup for (a) uncoated glass insulator unit and (b) RTV-coated glass insulator unit

Table 1. Maximum PD magnitudes for the uncoated glass insulator units

	Maximum PD magnitudes (pC)			
Voltage (kV_{rms})	1st unit	2nd unit	3rd unit	Average
0.0	0.2	0.2	0.2	0.2
2.5	0.7	0.5	0.3	0.5
5.0	0.6	0.5	0.6	0.6
7.5	0.6	0.5	0.8	0.6
10.0	0.6	1.3	1.2	1.0
12.5	1.8	16	40	19.3
15.0	2.1	66	150	72.7
17.5	110	290	320	240.0
20.0	400	1100	770	756.7
22.5	500	1500	1100	1033.3
25.0	800	1800	1200	1266.7
27.5	1200	1900	1500	1533.3
30.0	1500	2100	1700	1766.7
32.5	2000	2300	1900	2000.0
35.0	2200	2500	2000	2233.3
37.5	3000	100000	4000	35666.7
40.0	200000	150000	175000	175000

Table 2. Maximum PD magnitudes for the RTV-coated glass insulator units

	Maximum PD magnitudes (pC)			
Voltage (kV_{rms})	1st unit	2nd unit	3rd unit	Average
0.0	0.3	0.2	0.2	0.2
2.5	0.3	0.3	0.3	0.3
5.0	0.5	0.5	1.4	0.8
7.5	1.6	0.6	1.5	1.2
10.0	1.6	1.0	9.0	3.9
12.5	1.6	1.2	11	4.6
15.0	1.6	25	14	13.5
17.5	200	180	330	236.7
20.0	800	800	600	733.3
22.5	1100	1000	800	966.7
25.0	1600	1100	1000	1233.3
27.5	1800	1250	1200	1416.7
30.0	1800	1300	1600	1566.7
32.5	3300	1400	1700	2133.3
35.0	4000	1300	1800	2366.7
37.5	4800	1600	2100	2833.3
40.0	4800	2000	3000	3266.7

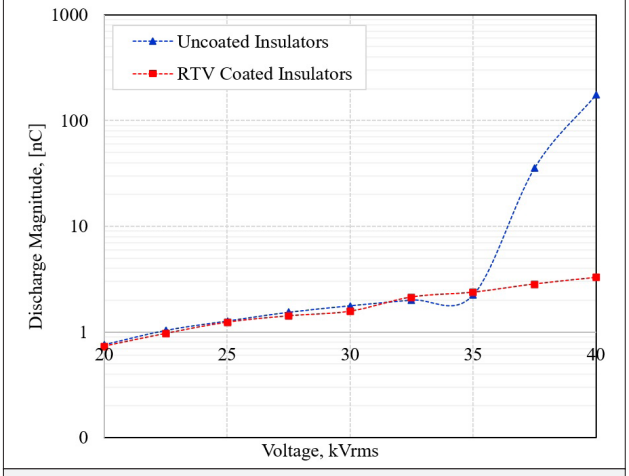

Figure 3. Maximum discharge magnitudes for RTV-coated and -uncoated glass insulator units

utilized to obtain the discharge magnitudes, as well as its patterns. In addition to the laboratory studies, the laboratory system is modeled in 3D geometry, and the field distributions corresponding to the coated and uncoated glass insulators are obtained to determine the effects of the RTV coatings on the field distributions.

Experimental study

Cap-and-pin type suspension glass insulators were used in the present study. The diameter of the insulator is 280 mm, the spacing is 146 mm, and the nominal creepage distance is 445 mm. RTV-HVIC was applied to the glass insulators by using the spraying method. Three thin RTV coatings were applied consecutively in a 15-minute interval, and average wet thickness was obtained at approximately 0.5 mm. Figure 1 shows the RTV-coated and -uncoated glass insulator units.

The experimental studies were performed at Istanbul Technical University, Fuat Kulunk High Voltage laboratory. A shielded test room with 6 m×6 m×3 m dimensions was used to implement the experiments. A noise-free testing transformer with 50 Hz, 100 kV maximum output voltage, and 20 kVA rating was used for the tests. The background noise level of the test room was <1 pC up to 100 kV testing voltage.

The insulator unit was suspended from the grounded ceiling through a 50 cm long metallic extension link. A 150 cm long smooth aluminum conductor was used to consider the line effect, and necessary hardware elements (e.g., suspension clamp) were used to connect the insulator unit to the line. The conductor was terminated by corona rings with 15 cm diameters at both ends to eliminate the terminal effects. The laboratory test setup of the insulator unit is illustrated in Figure 2.

The discharge characteristics of the glass insulator units were analyzed under AC voltage condition. Ambient conditions would be very effective on the discharge characteristics; therefore, the temperature and humidity of the test room were kept constant. The laboratory conditions were observed at a tem-

perature of 26 °C and a relative humidity of 45%. The experiments were repeated by using three identical units for both RTV-uncoated and -coated glass insulators to increase the reliability of the test results. Discharge levels of the insulators were measured by using a PD test system, with a fiber-optical measuring cable, and the discharge measurements were obtained through a quadrupole by using a 1007 pF coupling capacitor. In addition to the PD test system, a daylight UV corona camera

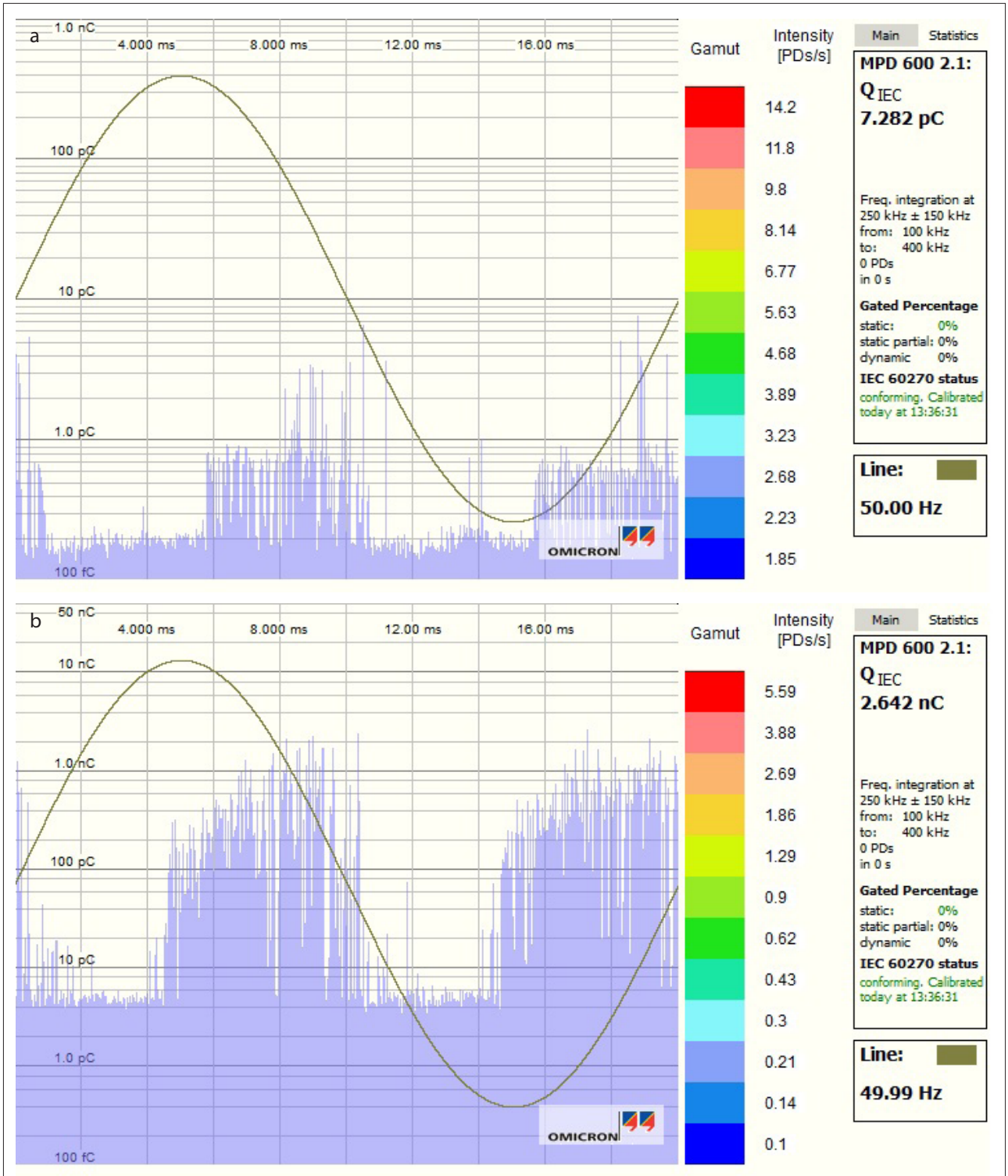

Figure 4. a, b. PD characteristics of the uncoated glass insulator unit for test voltage of (a) 10 kV_{rms} and (b) 30 kV_{rms}

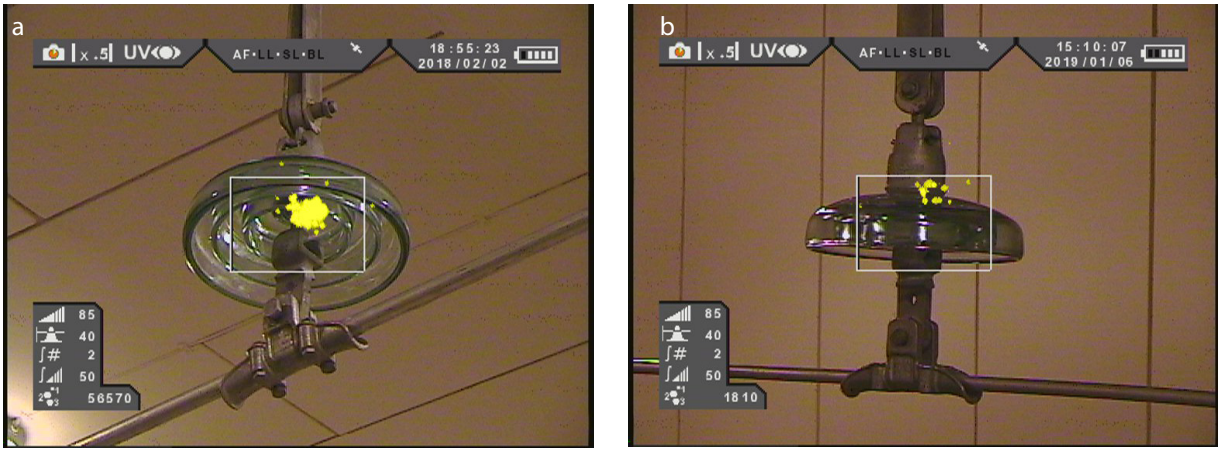

Figure 5. a, b. Discharges around the pin side of the uncoated unit (a). Discharges around the cap side of the uncoated unit (b)

Figure 6. a, b. Discharges around the pin side of the RTV-coated unit (a). Discharges around the cap side of the RTV-coated unit (b)

was used to indicate the location of the corona discharges and to detect the corona pulse counts. The UV corona camera has 10^{-8} W/cm^2 minimum UV sensitivity.

The experimental studies were conducted up to 40 kV_{rms}, 50 Hz voltage. The voltage was increased from 0 to 40 kV_{rms} voltage, and discharge characteristics were measured at voltages corresponding to 2.5, 5.0, 7.5, 10… 40 kV_{rms} voltage levels, with a total number of 17 measurement points. The PD test system was calibrated by using an external calibrator before starting the discharge measurements. For each voltage condition, at least 60 s of waiting time was considered. The averaged pulse magnitudes corresponding to the waiting time were recorded as pulse magnitudes for the relevant voltage condition. This procedure was applied for all the measurements. The measured discharge magnitudes for the uncoated and RTV silicone rubber-coated three glass insulator units are provided in Tables 1 and 2, respectively.

Figure 3 shows the discharge magnitude for coated and uncoated insulators for 20–40 kV voltage range in a logarithmic scale. As shown in Figure 3, the surface PDs corresponding to the uncoated insulators are very severe, especially for voltage >35 kV. Moreover, the discharge magnitudes for the uncoated insulators are relatively high as compared with the coated ones for test voltages up to 15 kV.

Surface discharge patterns for the uncoated glass insulator units are illustrated in Figure 4 for two different voltage levels. As shown in Figure 4, there is an increase in the maximum discharge magnitudes as the test voltage increases.

It is clear from Figure 4 that the discharge pulses appear on the first half cycle after the peak of the voltage. Similarly, the same discharge patterns occur for the second half cycle of the voltage.

The discharges captured by the daylight UV corona camera around the pin side and for the cap side for uncoated glass insulator unit are presented in Figure 5.

The discharges were also captured for the RTV-coated glass insulator units, and the recorded pictures are illustrated in Figure 6.

It is clear from Figures 5 to 6 that for both coated and uncoated insulator elements, the pin side and cap side of the insulators are critical with respect to electrical discharges. In addition to the location of the corona discharges, the UV corona camera also measures the corona pulse counts, which indicate the discharge intensity. Corona pulse counts corresponding to the pin regions (Figures 5 and 6(a)) and the cap regions (Figures 5 and 6(b)) were measured. The measurements showed that the discharges around the cap side of the insulators became visible at an earlier voltage than those of the pin side of the units. Moreover, the corona pulses on the UV corona camera screen would be visible when the PD magnitude was approximately 500–1000 pC. Note that the UV camera only detects the discharges on the visible part of the insulator, and due to this reason, pulse count results were not reported.

Simulation study

Several studies were conducted on the numerical analysis of electric fields along the silicone rubber insulators, and electric field and potential distributions were analyzed [13-15]. In the present study, similar electric field analysis was implemented for the RTV-coated glass insulators. The laboratory test setup as shown in Figure 2 was considered in the simulation studies. The glass insulator, a 0.5 mm thick RTV coating, the connections, and the smooth aluminum conductor were taken into account. A finite element method-based commercial software (Comsol Multiphysics) was used for the 3D simulation studies. Owing to the thin RTV silicone rubber coating on the glass insulator surface, a large number of meshing elements were required to discretize the 3D geometry. To reduce the meshing elements, and therefore the computational time, the symmetry condition of the test setup was considered. With the help of the plane symmetry condition, only 1/4 portion of the geometry was modeled. Figure 7 shows the insulator element with coated surface and the simulation model considering the symmetry conditions.

The 3D model had approximately three million meshing elements. Relative dielectric permittivity of the glass shell, RTV silicone rubber coting, and cement region of the insulator were assigned as 4.2, 3.2, and 10.0, respectively. Electric potential and electric field distributions were obtained for both RTV-coated and -uncoated glass insulator units. Figure 8 shows the mesh distribution of the RTV-coated insulator, as well as the electric potential distribution.

Figure 9 illustrates the electric field distribution along the creepage path of the insulator unit for both RTV-uncoated and -coated insulator, considering a 1 kV peak AC voltage. Maximum electric field strengths occur around the pin and cap regions, as shown in Figure 9, and the magnitude of the electric field around the cap region is the highest. It is clear that the RTV coating suppresses the maximum electric field strengths around both the pin region and the cap region.

As indicated in the experimental studies, corona discharges occurred around the cap and pin regions of the insulator unit, and the discharges around the cap region started earlier than those of the pin region. 3D electric field analysis results supported the

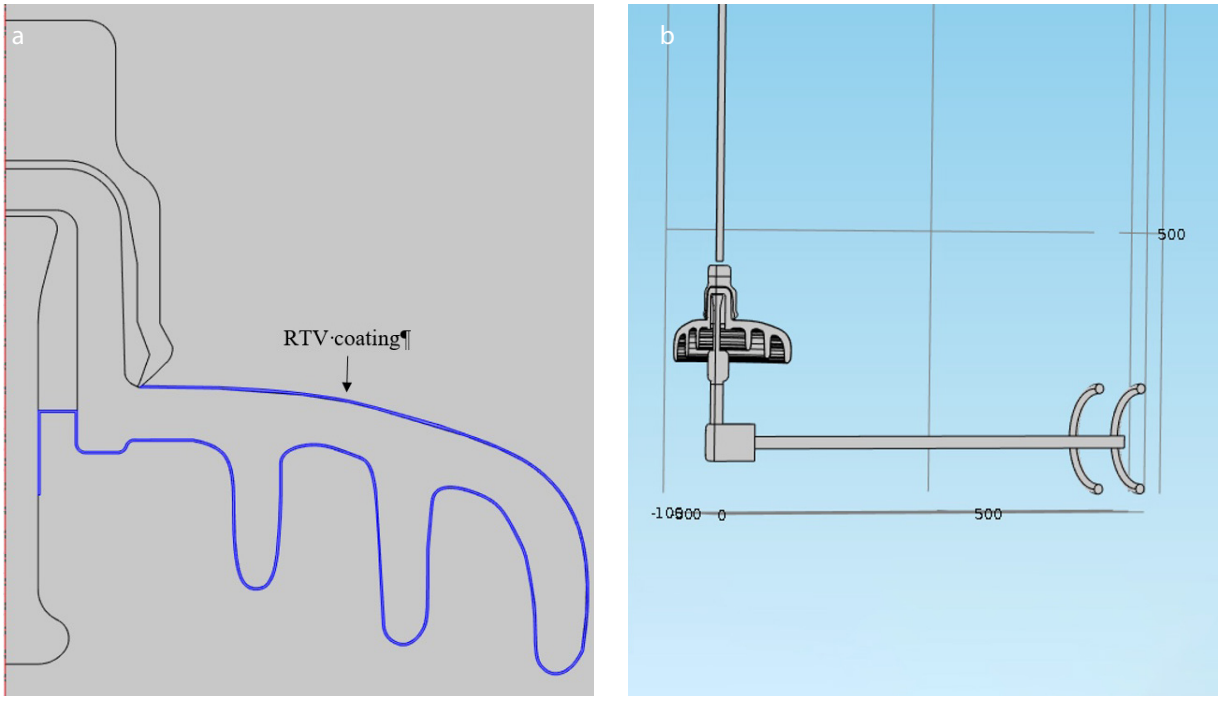

Figure 7. a, b. Model of the RTV-coated glass insulator (a). 3D laboratory model of the insulator unit (b)

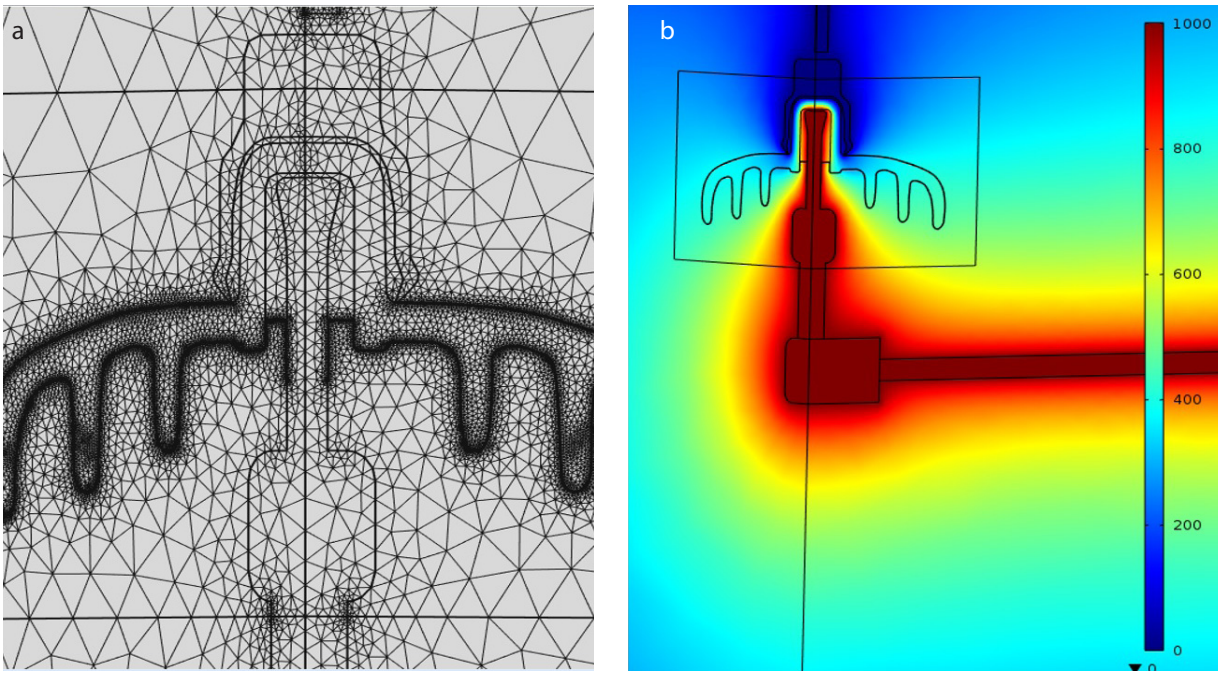

Figure 8. a, b. Mesh distribution of the insulator (a). 3D electric potential distribution around the insulator (b)

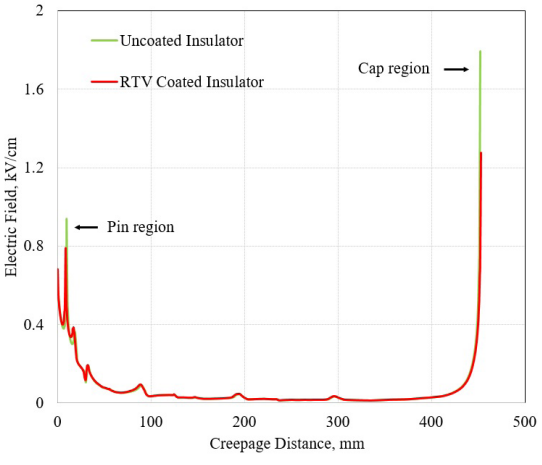

Figure 9. Electric field distribution along the creepage path of the insulator unit

experimental results. The cap region and pin region were found to be the critical ones with respect to high electric field strengths. Moreover, the magnitude of the field strengths around the cap region is the highest, which indicates that the discharges around the cap region would start at an earlier voltage.

The experimental results showed that the magnitude of the surface PDs for the uncoated insulator is greater than that for the RTV silicone-coated insulator case, especially for voltage >35 kV. Reduction in the maximum electric field strengths on the critical regions due to the RTV coating would be the reason for this condition.

Conclusion

The effects of the RTV silicone rubber coating on the discharge characteristics of a cap-and-pin type suspension glass insulator units are presented. Both the experimental and 3D simulation studies are conducted. The following summarize the research results:

- UV corona camera measurements indicated that the discharges occurred around the pin region and cap region of the insulator for both RTV-uncoated and -coated conditions. The discharges around the cap region started earlier than those of the pin region.
- In the case of the RTV silicone rubber coating condition, the magnitude of the surface discharge would be less as compared with the uncoated condition, especially for test voltages >35 kV.
- The patterns of the surface discharges for the RTV-uncoated and -coated conditions showed similar behaviors.
- 3D electric field analysis showed that maximum electric field strengths occurred around the cap and the pin regions of the insulator, and the highest electric field strengths were obtained around the cap region. These results were also verified by the experimental measurements.
- The application of the RTV coatings on the insulator unit reduced the maximum electric field strengths on the cap and the pin regions of the insulator.

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ISTANBUL UNIVERSITY CERRAHPASA

RESEARCH ARTICLE

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Performance Analysis of Tree-Based Tag Anti-Collision Protocols for RFID Systems

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ABSTRACT

In today's fast-changing competitive environment, companies and organizations need to develop their services, applications, and business processes continuously in order to benefit more from time and resources. Radio Frequency Identification (RFID), as one of the technological innovations, is an auto-id technology that enables many new application domains in diverse scientific fields and provides important opportunities to build efficient industrial systems. It is capable of identifying, locating, tracking and monitoring objects, and offers companies and organizations important advantages to develop efficient and successful business applications. In RFID systems, tag identification is a critical process. However, tag collisions occur when multiple tags transmit their IDs to a reader simultaneously, and thus affect the stability of the RFID system. Therefore, a powerful tag anti-collision mechanism is required to accelerate the tag identification process while minimizing the collision effects. In this paper, we presented a performance analysis of some of the tree-based tag anti-collision protocols (binary tree, query tree, adaptive binary tree, and adaptive query tree) to evaluate the tag identification process for the RFID system in an IoT environment. In our experiments, we observed that adaptive tree-based tag anti-collision protocols have better performance than the binary tree protcol and the query tree protocol.
Keywords: RFID, IoT, RFID tags, anti-collision, tag identification, identification delay, communication overhead

Introduction

Radio Frequency Identification (RFID) is a wireless automatic identification (Auto-ID) and data gathering technology that gives the opportunity to track and monitor objects by using tags that carry information (Figure 1). The main feature of RFID technology is its ability to identify, locate, track, and monitor objects without a clear line of sight between the tag and the reader [1, 2].

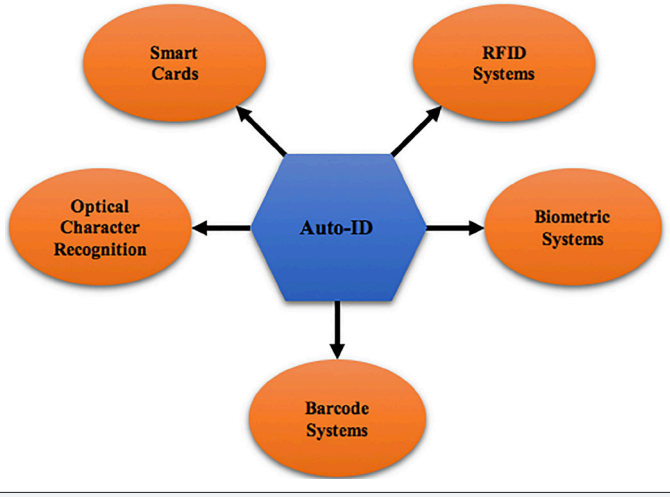

Figure 1. Auto-ID technologies

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The architectural structure of RFID is much more similar to smart cards that contain microchips. As in smart card systems, object-related information (data) is stored in an electronic data storage device which is called RFID tag consisting of a microprocessor and an antenna [2]. RFID tags can be active or passive. Active tags use a battery to supply power. On the other hand, the power of passive tags is provided by signals from the reader. The data exchange between the tag and the reader and the tag and other tags is performed by an electromagnetic field or wireless communication (radio frequencies) [3, 4].

In an RFID system, the data communication and the energy transfer occur between the reader and the tag. The electromagnetic waves emitted by the reader meet the antenna and activate the microchip inside the tag. The microchip modulates the received signals and sends it back to the reader via the tag antenna [1, 2]. Figure 2 illustrates a basic RFID system and provides an information about how it works. In an RFID system, tags are detected by the reader when they enter the reader's interrogation area. The tags send their data to the reader through RF signals. The reader converts these signals into digital data. The information generated by the RFID reader is transmitted to the related services/units within the system via middleware, software, controllers, servers, and network devices [1, 2, 4-6].

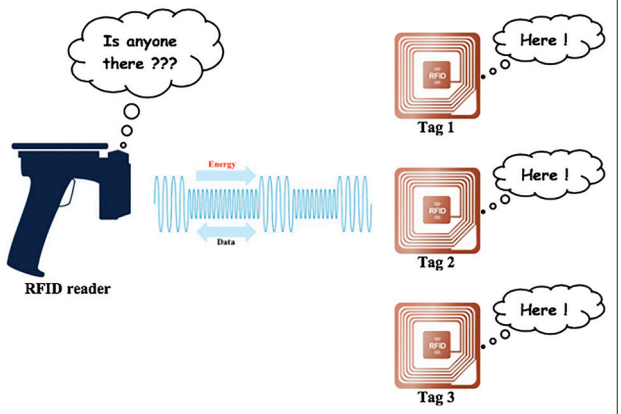

Figure 2. Data communication in an RFID system

RFID systems can be divided into two major groups, as mobile and immobile applications. Immobile RFID systems include RFID readers, antennas, hosts, servers, middleware, and external units such as light and sensors. These systems are also called RFID gates. In these systems, readers serve as gates, receive information from tagged objects and send these information to servers or controllers. Mobile systems employ wireless communication to gather data and monitor objects. They are similar to fixed systems due to the RFID system structure. They provide advantages such as data gathering and managing, reading/writing ranges and communication technologies. Reading/writing data from/to RFID tags is done by radio frequency. Passive tags are activated by the energy that is generated by the RFID readers, and send their own information to the readers. RFID readers receive information and transfer this information to related units (controllers, servers, database systems) in an IoT ecosystem [1, 2, 7, 8].

The differences in data communication techniques, the production and the application purposes of RFID show why these systems are very special applications. If the advanced features of RFID systems, the different application options are well understood and examined, strategies can be developed for how these systems can be used efficiently in enterprises or institutions [9, 10].

Figure 3 shows the various features of RFID systems that can be used to differentiate one RFID application from another. Hence, the basic design criterias and parameters in RFID system features can be stated as capacity of data read, the distance of variable read, tag durability, life expectancy, potential barier, tag diversity, capcity of data storage, data flexibility, etc. Some of these features are briefly explained as below [1, 4]:

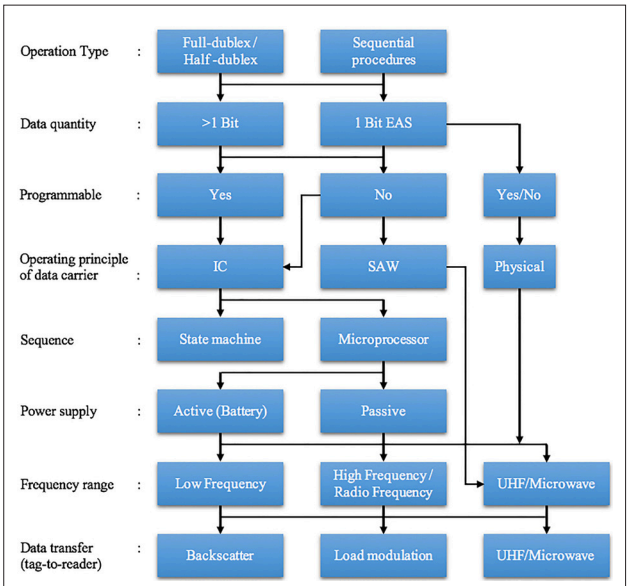

Figure 3. The various features of RFID systems [4]

Operation frequency: When selecting a frequency for an RFID system, the characteristic of several available frequency ranges must be taken into account. The availability of applicable frequencies and frequency bands in the operating area of the system has a significant impact on the system parameters [1, 4].

Modification: The ability to change or to write data to the tag.

Potential barriers: Factors that prevent the tag to be read properly.

Data security: It is the ability to encrypt data in the tag. In RFID applications, security requirements such as encryption, identification, authorization, etc. must be fully evaluated at the implementation stage [1, 4, 10].

Tag memory capacity: The amount of useful data the tag can store. The chip size of the data storage is specified by capacity of the memory. So, encrypted read-only data storages (tags) are used in price-oriented mass applications with low local information requirements. However, only one object description can be identified by using such a data carrier. Additional data are stored in the central database of the host computer. If the data needs to be rewrite to the tag, tags which have EEPROM or RAM memory technology can be used [1, 4, 10].

Cost: The costs of basic and auxiliary devices in the system needed.

International Standards: The ability to include a set of open standards accepted by many manufacturers and users is that it can meet technology-based global data and application standards.

Range: Range concerns whether the tag requires a line of sight for reading and how much remote signal it collects. The distance between tags should be set so that there is only one tag at a time in the reader's query area. The range required in an application depends on several factors such as the correct tag position, the minimum distance between many tags and the speed of the tag in the reader's query area [1, 4].

Instant number of readings: Data of an object should not be read only one time. Multiple data should be allowed to be read at a specific time. The maximum read/write distance and the time spent by the tag in the reader's query area determine the speed at which tags are associated with readers. The time and distance required to define objects, the time spent in the interrogation area at the maximum object passing speed, and the range required for the RFID system should be designed to be sufficient to transmit the needed data [1, 4].

Operational lifetime: The length of time that the tags used in an RFID system are readable.

Multiple-access and Anti-collision in RFID Systems

The processing of RFID systems usually involves a situation where multiple tags are present at the same time in the query region of a single reader. There are two main communication protocols as broadcast and multiple access in such a system. Broadcast communication is applied to transmit data from the reader to the tags. The data sent by the reader is taken simultaneously by all the tags in the query area of the reader (Figure 4). This comminication protocol can be imagened as the simultaneous reception of a news program transmitted by a radio station to the hundreds of radio receivers [1, 11].

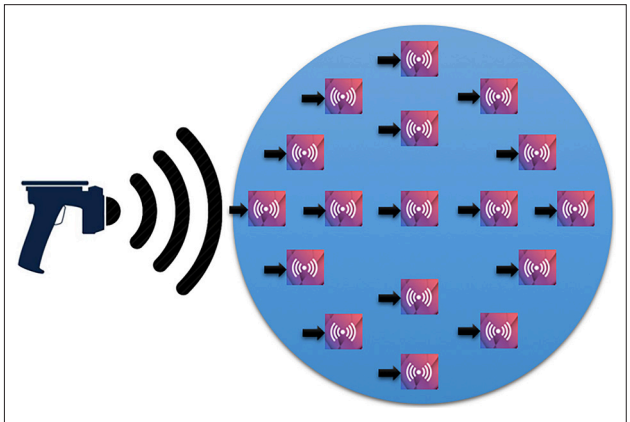

Figure 4. Broadcast communication

The multiple access protocol involves the transmitting data to tags in the query area of the reader (Figure 5). In multiple accesses protocol, many tags try to transfer data to a reader simultaneously [12].

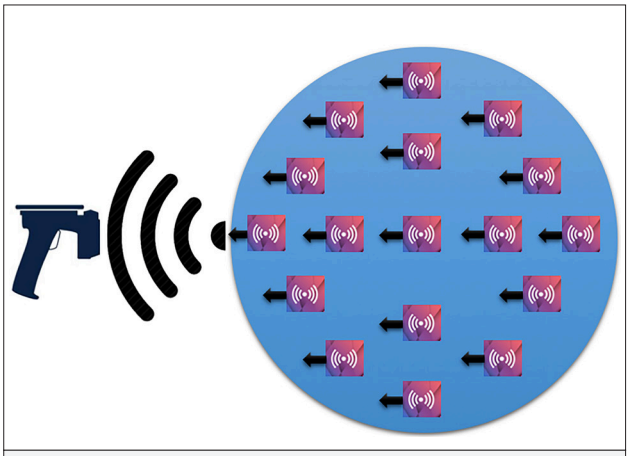

Figure 5. Multiple acces

The communication channels have specific channel capacities that are specified by the maximum data rate of the channel and the usability period. The channel capacity must be divided between individual receivers to transmit the mutual data without collision from the tags to the reader. For example; In an integrated passive RFID system, only the receiver portion in the reader can be used by all tags in the query area, as a common channel for data transfer to the reader. The maximum data rate is calculated via effective bandwidth of the antennas which are on the tag and the reader [1, 4, 7].

The multiple access problem is one of the most studied issues in the radio technology researches such as satellites and mobile technologies. The problem is that many participants attempt to access a single satellite or base station. So, it has crucial importance to differentiate individual participant signals. Although several protocols have been developed, mainly there are four multiple access protocols such as Space Division Multiple Access (SDMA), Frequency Domain Multiple Access (FDMA), Time Domain Multiple Access (TDMA), and Code Division Multiple Access (CDMA). These protocols are based on the assumption that there is a continuous flow of data from the participants. When a channel capacity is divided for communication, the channel remains divided until the communication is over [1, 7, 8].

The tags used in RFID systems are characterized by short-term activities in which unequal length gaps are entered. Tags are a particular problem in almost all RFID systems because, a tag cannot immediately be detected among the other tags in the reader's query area. The tag in the query area of a reader needs to be verified, read and written within a few milliseconds. After this process, the tags may not enter into the reader's query area for a long period of time. However, this situation does not mean that the multiple access protocol is not necessary for such an application. It should be considered that there are more tags of the same type at any location and that they are detected by the reader antenna. The activities on the transmission channels between the reader and the tag have high bursting factors. So, a packet access protocol must be used. The channel capacity should be divided only when really necessary. A powerful multi-access protocol can provide succesfull tag recognition by selecting the correct label without significant delay [1, 9, 10].

The implementation of the multiple access protocol in RFID systems contains some difficulties for the tag and reader. The implementation procedure should reliably prevent the collision that causes the unreadable of the tag data by the reader. Also, this process should not lead a noticeable delay. In RFID systems, the procedure that facilitates multiple access without collision is called as anti-collision protocol. Anti-collision protocols can be classified in two general groups as probabilistic approach protocols (ALOHA based) and deterministic approach protocols (tree based). In ALOHA based protocols, each tag attempts to send its own identification data (ID) at choosen time randomly. Although ALOHA based protocols reduce the probability of tag collisions, they cannot abolish completely [13]. So, They create a crucial problem, such as the failure to identify a particular tag for a long time that is known as starvation problem. Tree-based protocols create a conceptual binary tree during the tag recognition process. In this approach, the tags are divided into two subgroups at once and tried to recognize the subsets individually [14]. All tags in the reader's query area can be recognized by dividing to the subsets until each tag series has a single tag. Tree-based protocols do not lead to starvation problem, but delays in identifying tags are longer compared to ALOHA based protocols [15].

Tree-based Tag Anti-collision Protocols

Tree-based protocols perform the tag recognition within read cycle units. A query has been transmitted in a read cycle to the tags by the reader, then one or several tag send the IDs. The collisions cannot be perceived by the passive tags. However, the reader can detect the collisions among the responses of the tags. The reader determines the content of the query according to the result of this detection in the next read cycle [10, 13]. The tag decides whether transmit data or not when it receives a query from the reader. If a single tag transmits data only in one read cycle, the reader can recognize the tag successfully [10, 16].

In tree-based protocols, the reader recognizes all tags within the query area during a recognition frame consisting of several read cycles. The reader attempts to recognize a group of tags that transmit the data in the same read cycle [10, 13]. If there is more than one tag in the group, tag transmissions cause collision. When a collision occurs, the binary tree algorithm divides the tags in the group into two subsets by using tag IDs or random binary numbers [10, 16]. Then, the reader attempts to identify the two subgroups in the same frame individually. Tree-based protocols attempt to recognize all tags within range of the reader by continuing the division until a single tag remains in each group [10, 17].

A recognition frame in tree-based anti-collision protocols can be represented by different types of tree structures shown in Figure 6. Each node in the trees corresponds to a reading cycle. The numbers in the nodes are the count of tag transmissions in the read cycle. Depending on the number of tag transmissions, the read cycles can be seen in three cases [13, 16, 17]:

Idle cycle: There is no transmission attempts. An unnecessary recognition delay occurs. It does not cause the reader not to notice a tag.

Readable cycle: A transmission attempt occurs and the reader successfully recognizes the tag.

Collision cycle: More than one transmission attempt are seen and collision occurs. The reader cannot recognize any tags. The collision cycle delays tag recognition. The reader sends a query

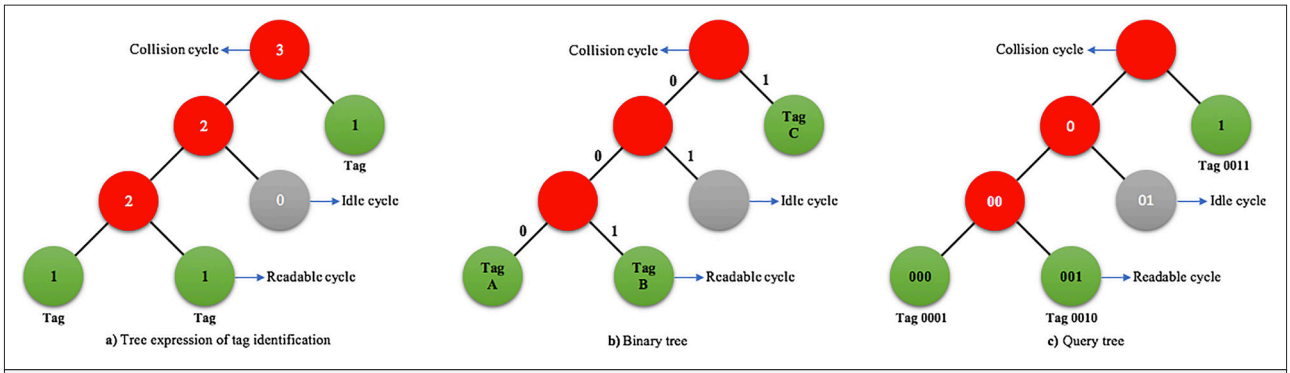

Figure 6. Tag identification in tree-based protocols

to all tags and performs segmentation of the tag set, including colliding tags [18].

Since a group is divided into two subsets in the recognition frame tree, the node of the collision cycle has only two sub-nodes that called leaf node. In tree-based protocols, collision cycles correspond to the nodes while readable cycles or null cycles correspond to leaf nodes. The tag recognition is a search process that to realized on the roots of the tree to find nodes of readable cycles. The performance of the recognition process depends on how effectively the group divides and how efficient the search works [10, 17].

Binary Tree Protocol

The binary tree protocol uses random binary numbers generated by collision of tags for the division procedure. The tag has a counter value loaded with 0 at the beginning of the frame. When the counter value is 0, the tag transmits the own ID. All tags create a group at the beginning of the frame and they transmit the data at the same time. The reader informs the tags about the collisions by creating a query. According to the reader's query, all tags change their counter values [19]. When the transmission of a tag causes collision, the tag selects a random binary number. The group is divided into two subgroups by adding the selected binary number to the counter value. When a collision occurs, the non-collision tag that counter value is not 0 increases the counter value by 1. If the reader's query does not indicate a collision, all tags reduce the counter values by one. The tag understands that the transmission is successful and that there is no collision. The tag that a reader does not recognize does not transmit any signals until the frame is terminated [16-19]. Figure 7 shows the tag recognition process in the binary tree protocol, and the numbers next to the lines indicate binary numbers randomly selected by the colliding tags. The reader also has a counter to end the frame [13]. The reader loads the counter value with 0 in each frame. The reader's counter value indicates the number of tag sets that are not yet recognized in a frame. If a collision occurs, the reader adds 1 to the counter value because of the increasing the number of tag sets that the reader should recognize. Otherwise, the reader decreases the counter value by 1. When the reader's counter value is less than 0 (counter value<0), the reader terminates the frame [10, 13, 17].

The binary tree protocol uses a random number generator. The RFID reader emits a signal and prompts the tags to generate random numbers. Each tag produces 0 or 1 and adds this value to the counter and sends a reply to the reader. The reader groups the tags based on the number values in the tags' counter. Whenever any collision occurs, the tags causing the collision increase their counters again by generating a random number. This process continues until each tag in the tree remains alone on a leaf node. The tag, which becomes readable at the end of the process, transfers its contents to the RFID reader. Binary tree protocol gives better performance even most of the tag IDs are the same. However, if tags that generate random numbers produce the same number continuously, the long reading time can be seen in this protocol [1, 10, 19].

Query Tree Protocol

The query tree protocol uses tag IDs to subdivide tags. The reader sends a query containing a bit series to the tags. Tags, which the IDs start with this bit series, send the ID information to the reader in response. The first tag, which has equual ID bits with the bit series, responds by passing the ID to the reader. If there is a collision while receiving the answers, the reader will send the query to the next reading cycle by increasing the length of the bit series by 1. [1, 20]

In the query tree protocol, the reader has the Q queue for the bit series. At the start of the frame, Q is started with two strings which have 1 bit length and values are 0 and 1. The reader removes a bit series from Q and passes only one query every time. If the tag responses collide, the reader adds two series which are 1 bit long to the Q. All tags are recognized by expanding the query until a response or no response is received [5, 10, 13]. Figure 8 shows the tag recognition procedures in

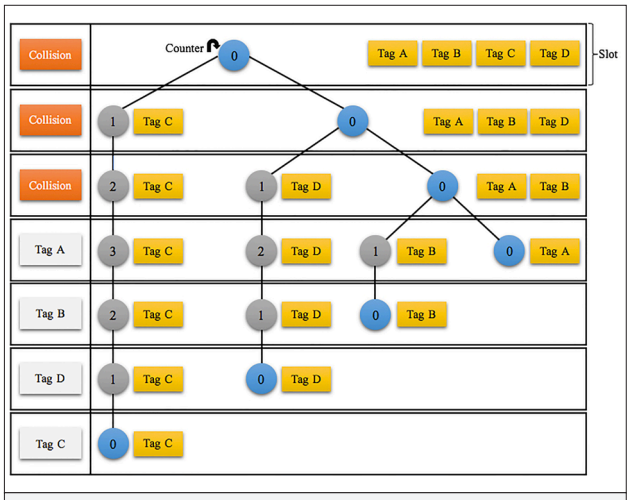

Figure 7. Tag identification using the binary tree protocol

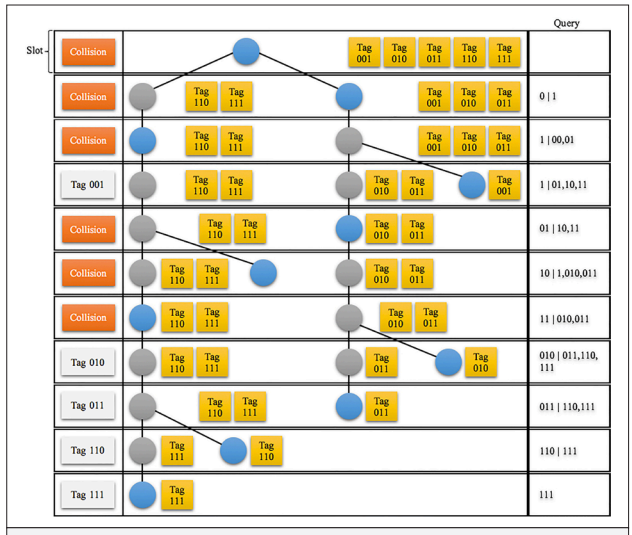

Figure 8. Tag identification using the query tree protocol

the query tree protocol. The number inside the nodes defines the query that the reader transmits [10]. The reader first sends a signal to the tags in the query area. With this signal, tags which the first bit is 1, are queried. The tags compare their IDs with the query, and the appropriate ones send the response to the reader. The tags are then grouped according to their IDs and the query tree is divided into two subnodes. These operations are repeated on each node. Thus, each tag is placed on a node.

For example; If the tag responses of the q1q2. . . qx query (qi € {0, 1}, 1 <x <b, and b have the number of bits in the tag ID) collide, the reader uses two queries longer than 1 bit in subsequent read cycles as (q1q2 . . . qx0) and (q1q2 . . . qx1) [17]. The tag group that matches (q1q2.. qx) is divided into two subgroups. One of the subgroups is the tag group that matches (q1q2 . . . qx0), the other is the tag groups matching (q1q2 . . . qx1) [17]. Because each tag has a unique ID as a result of the query, tags can be queued according to the query string. The reader will read all the tags by contacting the tags in the ID queue one by one. If there is a collision again, the reader will query again by adding 1 bit to the query parameter. All the tags will be read with this process that continues until the response is received [10, 17].

Compared to the binary tree protocol, the query tree protocol performs simple operations on tags. The query tree protocol is also known as the non-memory protocol because the tags only need to hold the ID information [21]. The shortness of the delay time in this protocol varies depending on the similarity of the IDs of the tags. If the majority of tag IDs are the same, reading with this method may take a long time. The delay time increases as the number of similar IDs increases [1].

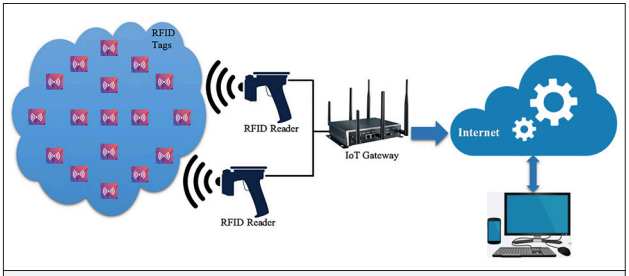

Figure 9. System architecture

Adaptive Tree-based Protocols

These protocols are improvements of tree-based protocols. They use the information provided by the last frame in the reader to avoid tag collisions. They have fast tag identification characteristics by decreasing not only collisions but also unnecessary cycles. They suppress the occurrence of collisions, shorten the total delay for tag identification, and preserve low communication overhead, while still identifying all tags [13]. In these protocols, RFID readers accomplish tag identification processes repeatedly, and RFID tags are classified into three groups based on the tag mobility (i.e, object tracking and monitoring): staying tags, arriving tags, and leaving tags. There are two types of adaptive splitting protocols: adaptive binary splitting [21, 22] and adaptive query splitting [23, 24]. In adaptive binary splitting, tag identification process is started from only readable cycles of the last frame and random numbers are used to split tag sets. In adaptive query splitting, tag transmissions are controlled by reader interrogations analogous to query tree. Tags are memoryless and store only their own IDs. To eliminate collisions between staying tags, the reader does not transmit queries that multiple tags responded in the last frame [13, 16, 17].

System Model

We consider an RFID-based tracking system for mobile objects in an indoor environment. As shown in Figure 9, the system contains a reader and passive UHF tags. Tags enter and leave the reader interrogation area. When tags are not inside the reader interrogation area, they are all passive. Tags are only activated when they are in the reader interrogation area. We assume that the tags move with a relative low speed (serious packet loss can be occured when the tags move with a high speed, resulting that several tags cannot be detected), and the reader can perform tag identification process repeatedly.

Tag identification is a dynamic and continuous process consisting of reader request and tag response. The primary consideration when selecting the RFID tags is to find the optimal balance between the tag size and the read range. The right read range depends on the distance between the reader and tags. Figure 10 illustrates the data tranmission in a basic RFID

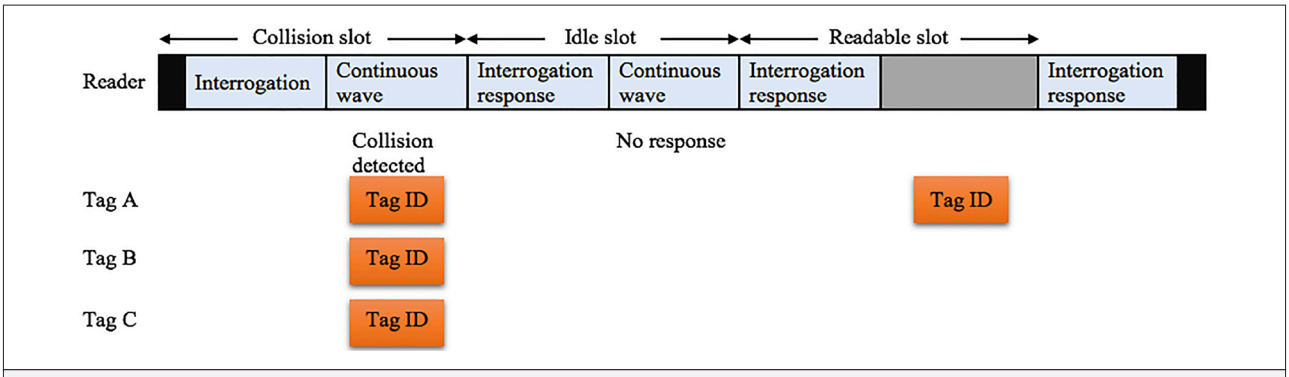

Figure 10. Tag identification process

system. Based on the number of tag ID transmissions in a query period, the tag reading process is divided into three parts on the reader side:

- Readable slot: Just one tag responds to the reader. The reader successfully recognizes the tag.
- Collision slot: Reader receives signals but cannot recognize any tag. Two or more tags respond to reader simultaneously. Tag identification process fails depending on the collision.
- Idle slot: The reader does not receive any tag signal. Unnecessary increment of the identification delay occurs.

In our system, the reader can recognize multiple tags. When tags enter the reader interrogation area, all that they have to perform is to become active and respond with the data corresponding to the reader signal. The communication between the tags is impossible, and the tags cannot decide whether the channel is busy or not. The medium is shared by two or more tags, and thus collisions occur at the reader side when these tags transmit data simultaneously. Since collisions make the collided signals be retransmitted, the power consumption of the tags and the time elapsed for recognizing the tags increase. Therefore, an efficient tag anti-collision scheme with fast identification and low computational complexity is required.

Performance Analysis

We evaluated the performance of the tree-based tag anti-collision protocols: binary tree, query tree, adaptive binary tree, and adaptive query tree. These protocols employ the binary search tree to identify the RFID tags. We make use of the methods presented in [1, 10, 13]. We take into account the following aspects in order to analysis the tag identification process [1, 10, 13]:

- Number of collisions: Collisions prevent the tag identification and increase the tag power consumption.
- Tag identification delay: Total delay required for the reader to recognize all tags in its own query area.
- Number of idle cycles: This affects the tag identification delay.
- Tag communication overhead: The average number of bits in a frame. It affects the tag power consumption.

We assume that T_x indicates tag x, N is the number of tags in our simulation environment, $T_{R,i}$ denotes the set of tags in the interrogation area of reader R during i^{th} frame F_i, and $|T_{R,i}|$ is the number of tags in set $T_{R,i}$. In order to take tag mobility into account, we classify the tags into three groups: remaining tags (stay inside the interrogation area), arriving tags (pass through the interrogation area), and leaving tags (leave the interrogation area). We can give the following definitions for our system model:

- Frame F_i: The i^{th} identification process that a reader executes. It is the period from the moment the reader starts identifying tags in its interrogation area to the moment it completes the tag identification.
- Slot: The duration reader R sends an interrogation signal to tags and tags send their IDs to reader R. It can be idle, readable, or collision.
- T_x:$T_x \in \{T_{R,i} \cap T_{R,i}\}$, T_x is a remaining tag.
- T_x:$T_x \in \{T_{R,i+1} - T_{R,i}\}$, T_x is an arriving tag
- T_x:$T_x \in \{T_{R,i} - T_{R,i+1}\}$, T_x is a leaving tag.

Table 1 shows the simulation setup. We assume that there are 250 tags attached to the objects moving at a constant speed in an area of 50 x 50 m^2. Tag ID length is 128 bits. Tag IDs are randomly generated for every simulation scene. At the start of the simulation, all tags are randomly distributed in the simulation environment. The reader is placed in the middle of the simulation area. The interrogation range of the reader is 5 m. Since the reader's interrogation range is 5 m, some tags enter and leave the interrogation area. In order to evaluate the system performance, we considered several factors such as number of tags, tag ID similarity, tag mobility, tag communication overhead, tag identification delay, number of readers, reader interrogation area, tag moving speed, number of collisions, number of idle cycles, and tag stationary probability.

Table 1. Simulation setup

Parameters	Values
Simulation area (m^2)	50 x 50
Tag ID (randomly generated)	128 bit
Number of tags	250 (max. 3000)
Tag moving speed (m/frame)	1 (max. 5)
Number of readers	1 (max. 5)
Read range (m)	3 (max. 10)

Tag moving speed indicates the physical distance which a tag moves during one frame. To evaluate tag identification process, we define the moving speed for a tag as follows [10, 13]:

$$v(T_x) = d_{Tx}(t)/F_{prtcl}(t) \quad (1)$$

- t: represents a specific time interval $[t_i, t_{i+1}]$.
- $d_{Tx}(t)$: the distance that T_x moves in t.
- $F_{prtcl}(t)$: The number of frames that the anti-collision protocol executes in t.

Figure 11, 12, and 13 present the effect of varying the number of tags in the reader interrogation area. When the number of

tags increases, collisions take place more often and tag identification delay increases. Binary tree and query tree give similar delay results. Small differences in delay between these protocols result from the initial points of the identification process. On the other hand, adaptive tree protocols have shorter identification delay than the binary tree and query tree. In addition, the number of collisions and the communication overhead in adaptive tree protocols is less than the binary tree and query tree [1, 10, 13].

Figure 14 and Figure 15 illustrate the impact of tag ID similarity on the anti-collision protocols presented. Binary tree-based protocols are not affected by tag ID similarity because they do not employ tag ID patterns. On the other hand, since query tree-based protocols use tag IDs to split the tag set, they are affected by tag ID similarity. As the number of identical bit increases, the performance of query tree-based protocols deteriorates. Query tree-based protocols, as compared to binary tree-based protocols, have long tag identification delay and high tag communication overhead because the reader sends all interrogations leading to collisions in every frame and the number of idle cycles increases [1, 10, 13].

Figure 16 shows the impact of tag moving speed for the anti-collision protocols presented. When tags move at low speed, adaptive tree protocols have good performance than the binary tree and query tree. When $v(T_x) = 0$, adaptive tree protocols prevent collisions between remaining tags because they do not allocate more than one remaining tag to a set. When tags have high speed (or move faster), there are some remaining tags and collisions between these tags at the binary tree and query tree protocols hardly occur. In this case, adaptive

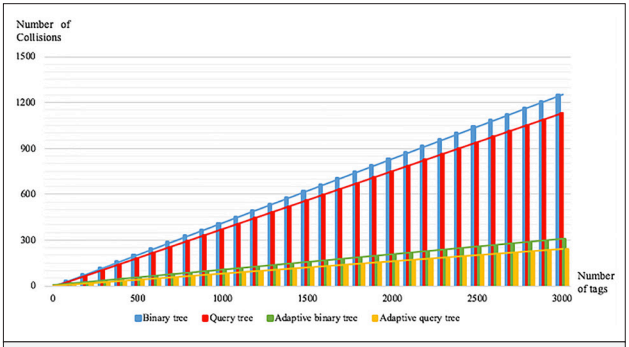

Figure 11. Collisions by the number of tags

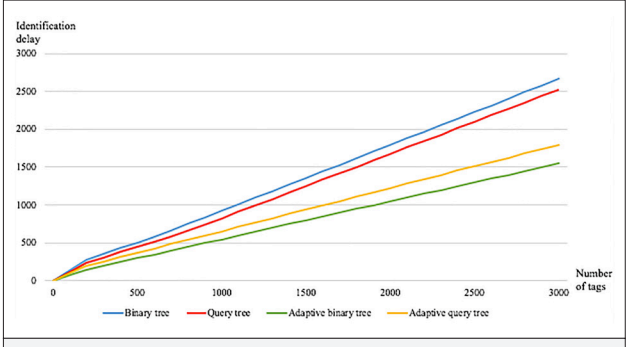

Figure 12. Identification delay by the number of tags

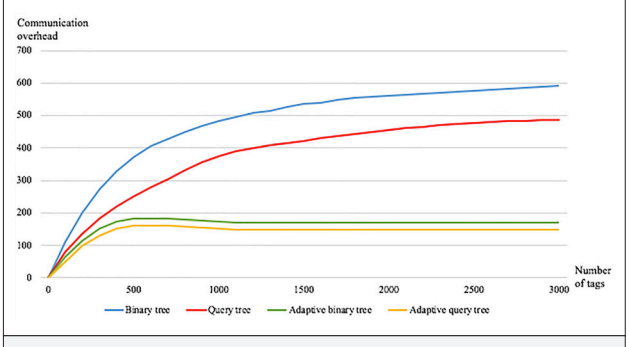

Figure 13. Communication overhead by the number of tags

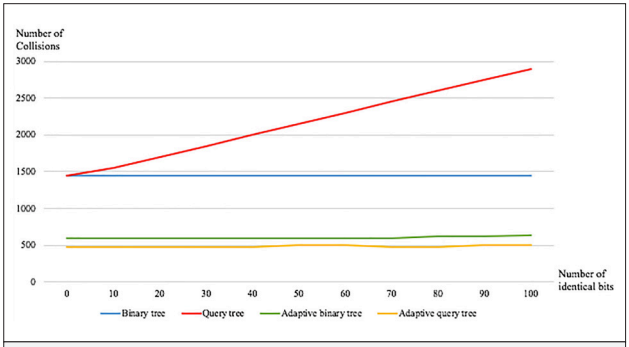

Figure 14. Impact of tag ID similarity

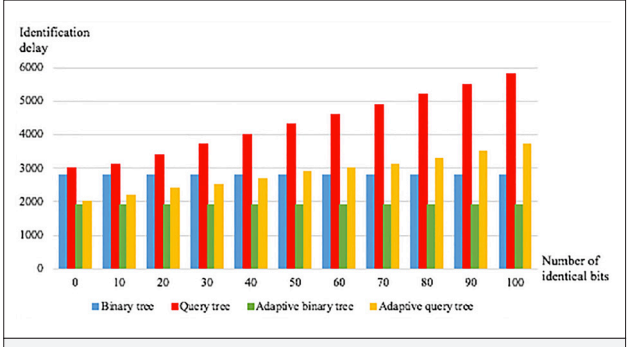

Figure 15. Identification delay by tag ID similarity

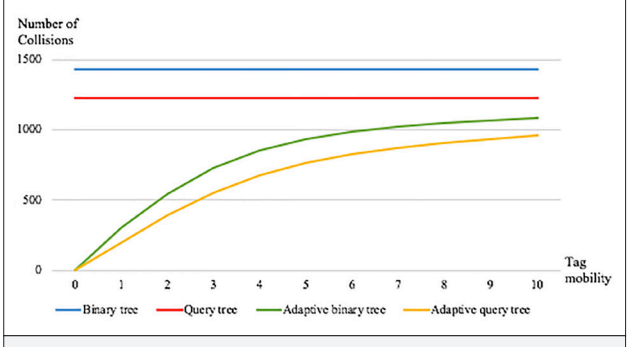

Figure 16. Impact of tag moving speed

tree protocols show performance similar to the binary tree and query tree [1, 10, 13].

Discussion

In today's rapidly changing competition environment, companies and organizations need to renew their services and communication techniques, change or revise their current business methods in order to benefit more from time and sources. In addition, automatic identification, object tracking and monitorig, data gathering and management technologies are always required for companies and organizations to develop applications and manage bussiness processes. Therefore, continuous innovations in data communication and information technology have lead to the development of new IoT systems using RFID [1].

In RFID system designs, it is aimed to build, collect, and manage dynamic information without any human contribution in real-time. Furthermore, it is required to employ more faster, more efficient, more secure, wide capacited communication technologies to instantly access dynamic object information in larger geographical areas without any limitations, to track and monitor objects, and to route the information associated with objects to the related systems. Therefore, the integration of RFID systems with IoT in the context of data gathering, management and analysis can lead to significant improvements in adaptability, sustainability, and efficiency for the industrial world including firms, manufacturers, retailers, customers, service providers, rule-makers, and end-users [1].

In RFID systems, data transmissions between readers and tags cause collisions because these devices use the same frequency band for mutual data communications. We can classify collisions into two categories: reader collision and tag collision. In a reader collision, when neighboring readers query a tag at the same time, reader signals collide and the tag cannot process any signal. In a tag collision, when multiple tags send their IDs to a reader simultaneously, tag signals collide and the reader cannot identify any tag. Since collisions lead to identification delay and communication overhead, they influence the RFID system's performance and stability [1, 10, 13].

Tag anti-collision protocols can be categorized into two groups: deterministic approaches (tree-based) and probabilistic approaches (ALOHA-based). ALOHA-based approaches reduce the occurrence probability of tag collisions since each tag attempts to send its ID at a randomly selected time. They have several problems that specific tags cannot be recognized for a long time. They cannot completely prevent the tag collisions and therefore cause the tag starvation problem. Tree-based approaches construct a tree conceptually for the tag identification process. They divide the tag set into two subsets and try to identify the subsets one by one. By dividing until each tag set has only one tag, the reader recognizes all tags in its interrogation zone. Tree-based approaches do not lead to the tag starvation problem. However, they have long tag identification delay as compared to ALOHA-based approaches [1, 10, 13].

Tag mobility is an important factor for RFID applications. We can classify the RFID applications into two groups: mobile and immobile. In immobile systems, deterministic and probabilistic anti-collision approaches can show similar features in terms of tag identification. In mobile systems, the time to recognize all tags in the reader interrogation area is an important factor for an anti-collision protocol's performance. For RFID applications that require continuous observation of tags, adaptive splitting protocols perform better than others, if the tag population has low speed.

Conclusion

In an RFID application, when a reader cannot recognize all tags in its own interrogation zone, data retransmission between the reader and tags is required for successful tag identification. In particular, since the neighboring tags cannot communicate with each other and make a decision on whether the channel is busy or not, tag collisions occur and consequently the collided tags retransmit their IDs to the reader. Tag collisions cause communication overhead, significant delays in data transmission, and critical faults that affect the system functionality and reliability. Therefore, an efficient and effective tag anti-collision protocol must be designed to enable the real-time execution and the fast identification process while minimizing collisions. Consequently, a tag anti-collision protocol used in an RFID application must have the following features:

- A reader must be able to promptly recognize all tags in its interrogation area. In mobile RFID applications such as real-time object tracking and monitoring, logistics and supply chain management, the tag identification process must keep pace with the moving speeds of objects. If the identification process is performed slower than the moving speeds of objects, the reader cannot identify the tags, and the tag starvation problem occurs, and thus the RFID system fails. Since the reader cannot precisely estimate the number of tags and their situations in its query area, the guarantee of identifying all tags should be considered in the development of tag anti-collision protocols.
- Tags must be identified while consuming less energy. In a passive RFID system, a tag's power is limited because its power is supplied by the reader signal. Furthermore, RFID tags have limited memory and low computational capability. Therefore, tag anti-collision protocols have to load the tags with less computational complexity and communication overhead.

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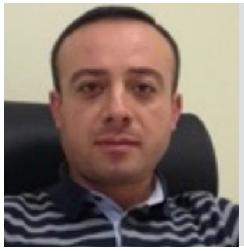

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