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Low-Voltage and Low-Power Analog Multiplier/Divider Using OTA Based on DTMOS Transistor

DTMOS Transistör Tabanlı OTA Kullanan Düşük-Gerilimli ve Düşük-Güçlü Analog Çarpıcı/Bölücü

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Abstract

A low-voltage and low-power current mode analog multiplier/divider design is presented in this paper. The multiplier/divider is based on operational transconductance amplifier (OTA) utilizing dynamic threshold MOS (DTMOS) structure and consists of only three OTAs. The circuit has the ability of consuming low power and requiring low voltage power supplies. 0.13µm IBM CMOS technology parameters are used to simulate the suggested multiplier/divider design and the simulation results are obtained using LTspice program. The current mode analog multiplier/divider architecture consumes only 12.07nW and requires ±0.2V of supply voltages thanks to employing DTMOS transistor. The simulation results agree well with the expected results.

Keywords: *Multiplier, Divider, DTMOS, OTA, Low Voltage, Low Power*

Öz

Bu çalışmada düşük gerilimli ve düşük güçlü akım modlu bir analog çarpıcı/bölücü tasarımı sunulmuştur. Çarpıcı/bölücü devresi dinamik eşik gerilimli MOS (DTMOS) yapısından yararlanan işlemsel geçiş iletkenliği kuvvetlendiricisi (OTA) tabanlıdır ve sadece üç tane OTA devresinden oluşmaktadır. Devre düşük güç tüketimi ve düşük gerilim kaynağına ihtiyaç duyma özelliklerine sahiptir. Önerilen çarpıcı/bölücü tasarımının benzetimlerini gerçekleştirmek için 0.13µm IBM CMOS teknoloji parametreleri kullanılmıştır ve simülasyon sonuçları LTspice programı kullanılarak elde edilmiştir. Akım modlu analog çarpıcı/bölücü mimarisi DTMOS transistör yapısı sayesinde yalnızca 12.07nW güç tüketmekte ve ±0.2V luk besleme gerilimine ihtiyaç duymaktadır. Beklenen teorik sonuçlarla uyumlu simülasyon sonuçları elde edilmiştir.

Anahtar Kelimeler: *Çarpıcı, Bölücü, DTMOS, OTA, Düşük Gerilim, Düşük Güç*

1. Introduction

Analog multipliers can be found in various analog systems with regard to analog modulators, artificial neural networks, peak detectors, analog signal processing, adaptive filters, frequency doublers, RMS-DC converters and so on. Fundamentally, an analog multiplier circuit generates a linear product of two input signals and yields z=A.x.y, where x and y are the inputs and A is a constant. The first analog multiplier design which consists bipolar junction transistor (BJT) has been proposed by Gilbert in

1968 [1]. In analog multiplier circuits, the properties of consuming low power and having low power supply voltages take an important place. Many methods in order to decrease the power dissipation of the circuit have been used by researchers [2–12]. One of the effective methods called DTMOS technique is utilized to reduce the power consumption and the required supply voltages [2, 4, 9, 11–15]. In this technique, bulk terminal is connected to gate terminal of MOS transistor so that the power dissipation becomes noteworthily less compared to the designs using traditional MOS transistors.

In literature, various analog multipliers have been suggested [2, 3, 5–8, 16–20]. In a study, a voltage-mode four-quadrant multiplier based on DTMOS technique is proposed by Babacan [2]. The multiplier consisting of 14 transistors includes the supply voltages of ±0.2V and the power dissipation is 18.4nW. Liu and Liu [3] have introduced a CMOS four-quadrant multiplier circuit operating in weak inversion region. The power dissipation of the multiplier is 6.7μW and it requires +1.5V supply voltage. Panigrahi and Paul [5] have introduced a voltage-mode multiplier circuit which is constituted in order to operate in weak inversion. The multiplication operation is carried out by driving the bulk terminals of the MOS transistors. The power dissipation and the single supply voltage are 714nW and +0.5V, respectively. Tanno et al. [6] have suggested a four-quadrant analog multiplier based on MOS weak-inversion-region with +1V single supply. The power dissipation of the design is 1.12μW. Wu and Xing [7] have proposed a current-mode four-quadrant analog multiplier. In the multiplier, two MOS translinear loops working in the subthreshold region are utilized. The power supply voltage and power dissipation are +3V and 60μW, respectively. In a study done by Mahmoudi et al. [8], a CMOS multiplier/divider working in the weak inversion mode has been proposed. The power dissipation is 9μW and the circuit requires +2V supply. Yildirim [16] has suggested a DTMOS transistor based multiplier structure using current squarer. The multiplier includes four current squarer circuits and a subtractor circuit. The power dissipation is 99.76nW and the supply voltage is +0.3V, respectively. In another study [17], a class-AB four-quadrant current multiplier circuit with the power dissipation of 12.4nW and a single +0.65V power supply has been proposed. The multiplier employs a class-AB current amplifier and a current splitter. Kasimis and Psychalinos [18] have suggested an improved version of the multiplier presented in [17]. Their current mode class-AB four quadrant multiplier provides a remarkable decrement in terms of power consumption compared to the corresponding one introduced in [17]. The power dissipation is 6.43nW and the supply voltage is +0.65V, respectively. Al-Absi and As-Sabban [19] have suggested a four-quadrant multiplier with the power dissipation of 700μW and a single +1.5V power supply voltage. The multiplier comprises of two rectifiers, two squaring circuits and one subtracting circuit. In a study done by Popa [20], two different analog multiplier/divider blocks whose power dissipations are 60μW and 75μW, respectively. The power supply of +1.2V is utilized in the circuit designs.

The motivation of doing this study is given as follows. A current-mode multiplier/divider having simple architecture is introduced in this work. The multiplier/divider circuit consists of only 3 OTAs which are based on DTMOS. Transistors are able to operate in subthreshold region thanks to using DTMOS technique. Therefore, the multiplier/divider circuit requires low power supply voltages and consumes low power which is in the order of nW with the help of DTMOS transistor.

2. Material and Method

In this part, material and method utilized in the study are given. Firstly, OTA structure based on DTMOS transistor is shown and then the proposed analog multiplier/divider architecture is presented.

2.1. OTA Structure Based on DTMOS Transistor

In the analog multiplier/divider block, OTA circuit which is based on DTMOS technique are used. Bulk terminal and gate terminal of MOS transistor are connected together to reduce the threshold voltage of MOS transistor in this technique. By doing this, the power consumption of circuit is significantly decreased because of MOS transistor operating in subthreshold region [2, 4, 9, 11–16, 21]. Figure 1 demonstrates the structure of DTMOS transistor and its symbol.

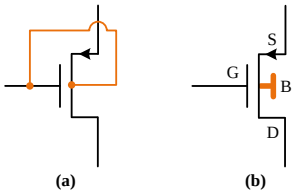

Figure 1. (a) DTMOS transistor structure and **(b)** its symbol

In the multiplier/divider topology, two-input one-output OTAs based on DTMOS given in Figure 2 is used. In Figure 2, a conventional OTA architecture has been modified by changing PMOS transistors to DTMOS transistors so that multiplier/divider circuit is able to consume power in the order of nW. The PMOS transistors (M_1-M_8) and NMOS (M_9-M_{14}) transistors aspect ratios are given by W/L=100µm/0.13µm and W/L=15µm/0.13µm, respectively. The biasing current and supply voltages are preferred as I_B=5nA and V_{DD}=-V_{SS}=0.2V, respectively.

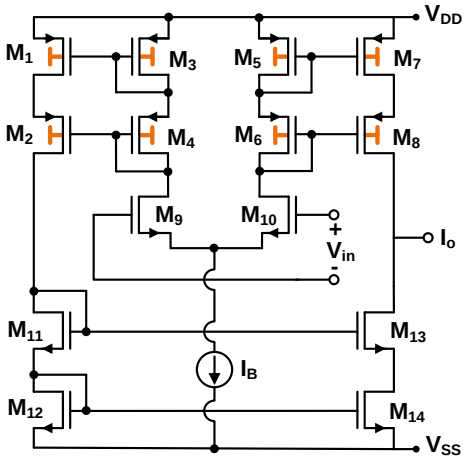

Figure 2. The circuit topology of DTMOS based OTA

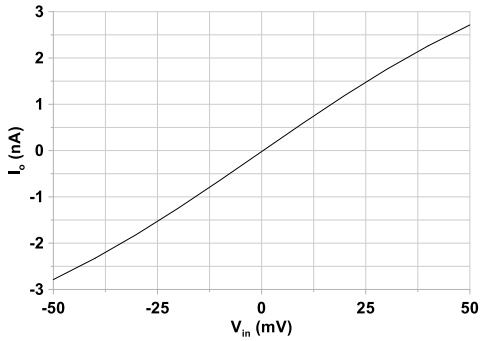

Figure 3. The DC transfer characteristic of DTMOS based OTA

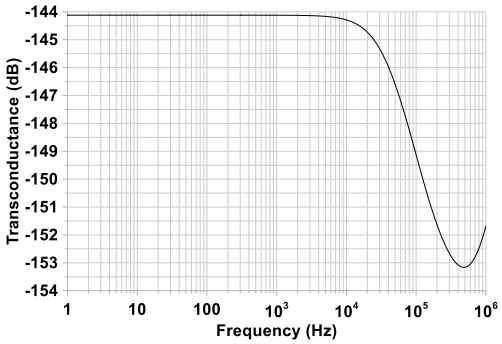

Figure 4. The transconductance of DTMOS based OTA

The DC transfer characteristic of the proposed OTA structure based on DTMOS is obtained by applying input voltage signal between -50mV and 50mV as given in Figure 3. Figure 4 demonstrates that -3 dB frequency for the OTA circuit is 58.7kHz. There is a trade-off between power consumption and bandwidth. High biasing current offers higher bandwidth. However, it occurs owing to consuming high power. In the proposed OTA which is based on DTMOS technique, the bandwidth is low in order to consume low power [15]. Both Figure 3 and Figure 4 reveal that transconductance gain value (g_m) of OTA is 62.2nΩ^{-1}.

2.2. Proposed Analog Multiplier/Divider Architecture

An analog multiplier/divider circuit based on OTA is proposed by Kaewdang [22]. In this study, we have modified the analog circuit by changing OTAs with DTMOS based OTAs to reduce the power dissipation of the circuit. The suggested analog multiplier/divider circuit diagram with DTMOS technique is presented in Figure 5.

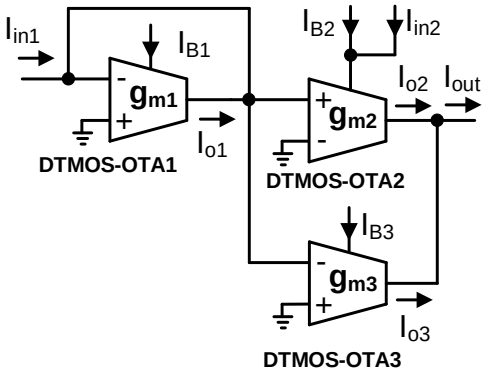

Figure 5. The circuit topology of DTMOS based multiplier/divider

The analog block consists of only 3 OTA structures which are based on DTMOS. The input current signal I_{in1} is applied to OTA_1 which is used as a current-controlled grounded resistor. The input voltage of OTA_1 is utilized as the input voltage for OTA_2 and OTA_3. The input current signal I_{in2} is added with the bias current I_{B2} belonging to OTA_2. By performing fundamental circuit analyses, the output current signals I_{o2} and I_{o3} of OTA_2 and OTA_3, respectively, are defined as

$$I_{o2} = \frac{g_{m2}}{g_{m1}} I_{in1} = \frac{I_{B2} + I_{in2}}{I_{B1}} I_{in1} \qquad (1)$$

$$I_{o3} = -\frac{g_{m3}}{g_{m1}} I_{in1} = -\frac{I_{B3}}{I_{B1}} I_{in1} \qquad (2)$$

In architecture, the transconductance gains of OTA_1, OTA_2 and OTA_3 are given as g_{m1}, g_{m2} and g_{m3}, respectively. The output current I_{out} is obtained by the summation of the currents I_{o2} and I_{o3}. When bias currents are set such that $I_{B2}=I_{B3}=I_B$, the output current I_{out} can be given in Eq. (3).

$$I_{out} = I_{o2} + I_{o3} = \frac{I_{in1} I_{in2}}{I_{B1}} \qquad (3)$$

Eq. (3) shows the current-mode multiplication and division function. When I_{in1} and I_{in2} are used as the input current signals, the analog block can perform multiplication operation. On the other hand, the analog block can perform division operation, when I_{in1} (or I_{in2}) and I_{B1} are used as the input current signals.

3. Results

The properties of the suggested low-voltage and low-power DTMOS based multiplier/divider in terms of DC transfer characteristic, operating as analog amplitude modulator, using as a divider, utilizing as a frequency doubler circuit, total harmonic distortion (THD) and power dissipation are examined. The analog block is simulated using 0.13µm IBM CMOS technology parameters. The power supply voltages of ±0.2V is used in the design. DTMOS technique is utilized and the bulk terminals are connected to gate terminals in PMOS transistors in order to decrease power dissipation of the analog block. In addition to this, the bulk terminals of NMOS transistors are connected to their source terminals.

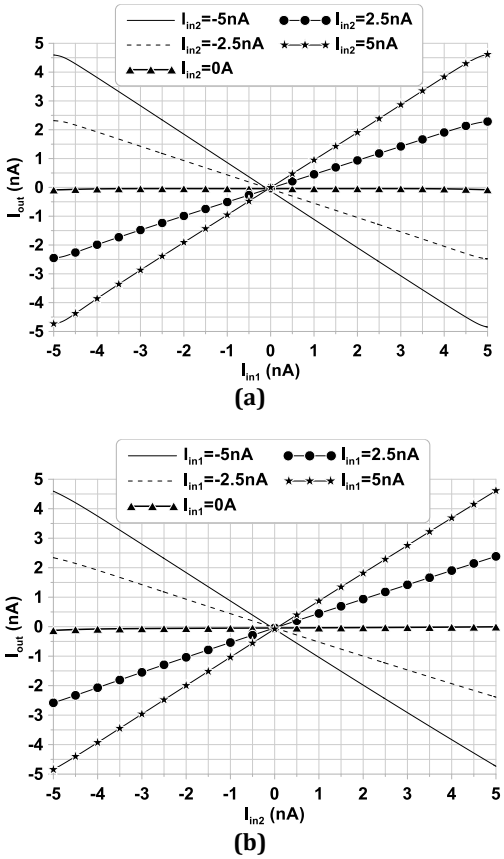

Figure 6. DC characteristic of multiplier/divider with regard to **(a)** I_{in1} **(b)** I_{in2}

Figure 6 (a) shows the DC transfer characteristics of DTMOS based multiplier/divider circuit for different I_{in2} currents from -5nA to 5nA with step of 2.5nA and I_{in1} current is applied from -5nA to 5nA and the bias currents are set to $I_{B1}=I_{B2}=I_{B3}=5nA$. Similarly, same processes are done to I_{in2} to obtain the DC transfer characteristics of multiplier/divider circuit with regard to I_{in2}.

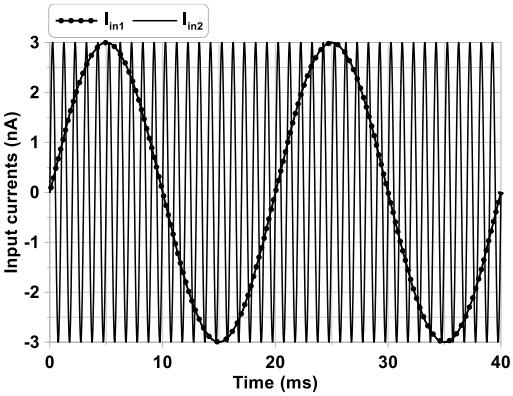

Figure 7. (a) Input current waveforms for $I_{in1}=3\sin(2\pi 50t)nA$ and $I_{in2}=3\sin(2\pi 1000t)nA$ **(b)** output current waveform of proposed multiplier

The time domain analyses given in Figure 7 for multiplier are done. The simulation results are presented in Figure 7 for $I_{in1}=3\sin(2\pi 50t)nA$, $I_{in2}=3\sin(2\pi 1000t)nA$ and $I_{B1}=5nA$ and reveal that the proposed multiplier/divider block can be utilized as an analog amplitude modulator. In addition, in Figure 8, we have performed time domain analyses for $I_{in1}=3\sin(2\pi 50t)nA$, $I_{B1}=5nA$ and I_{in2} current signals with different frequencies. Figure 8(a) and Figure 8(b) show the analyses results for $I_{in2}=3\sin(2\pi 500t)nA$ and $I_{in2}=3\sin(2\pi 2000t)nA$.

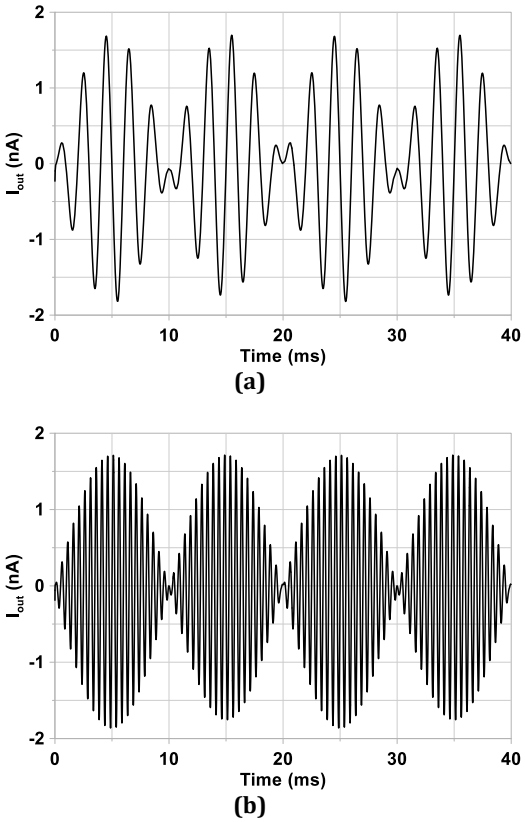

Figure 8. Output waveforms of multiplier for $I_{in1}=3\sin(2\pi 50t)nA$ and **(a)** $I_{in2}=3\sin(2\pi 500t)nA$ **(b)** $I_{in2}=3\sin(2\pi 2000t)nA$

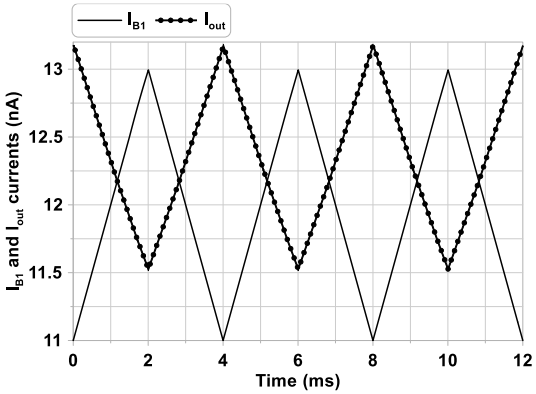

Figure 9. I_{B1} and output waveforms for divider structure

Our suggested analog circuit can also preform division operation and time domain simulation results for divider are given in Figure 9. The

simulation results obtained are given in Figure 9 for I_{in1}=10nA, I_{in2}=20nA and I_{B1} is a 250Hz triangular wave with amplitude of 1nA and with DC component of 12nA. In this case, the output current I_{out} is an inverting function of a triangular wave signal. Moreover, the proposed DTMOS based multiplier/divider analog block can be also used as a frequency doubler circuit. In order to show the property of frequency double of the introduced circuit, $I_{in1}=I_{in2}=3\sin(2\pi 100t)$nA and I_{B1}=5nA are applied to the analog block and the results are demonstrated in Figure 10.

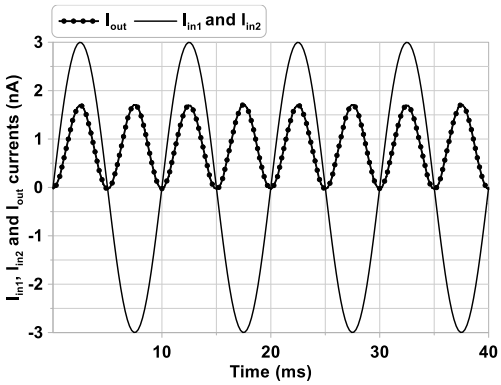

Figure 10. Input and output waveforms of multiplier/divider operated as a frequency doubler

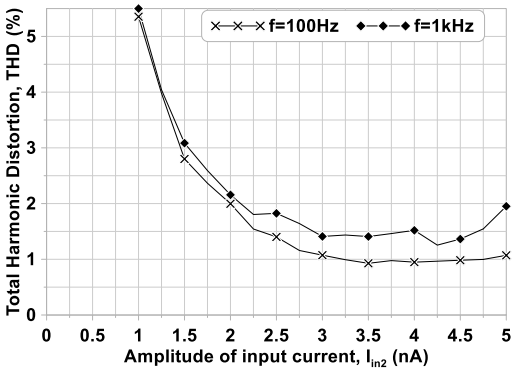

Figure 11. Total harmonic distortion of the proposed multiplier/divider

THD calculation is evaluated to underline the linearity of the proposed multiplier/divider circuit. The calculation of THD given in Figure 11 is carried out by setting the amplitudes of sinusoidal input signal current I_{in2} from 1nA to 5nA at two frequencies which are 100Hz and 1kHz and applying the input signal current I_{in1} as 3nA.

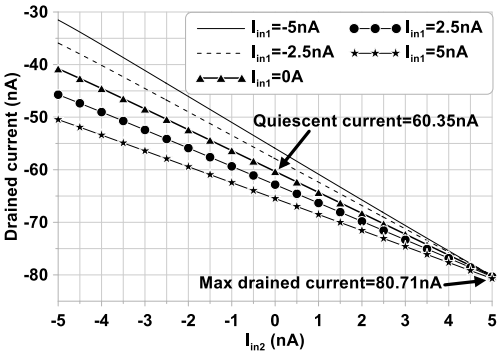

Figure 12. Drained currents from power supplies (V_{DD} and V_{SS})

Table 1. The comparison between our suggested multiplier/divider and previous multipliers

References	Number of transistors	Power dissipation (µW)	Supply voltage (V)	Technology (µm)
[2]	14	0.0184	±0.2	0.18
[3]	8[a]	6.7	+1.5	0.35
[5]	8[a]	0.714	+0.5	0.18
[6]	25[a,b]	1.12	+1	0.18
[7]	12	60	+3	0.5
[8]	17[a]	9	+2	0.35
[16]	12[a]	0.09976	+0.3	0.13
[17]	60	0.0124	+0.65	0.13
[18]	62	0.00643	+0.65	0.13
[19]	28	700	+1.5	0.18
[20]	17	60	+1.2	0.18
This study	**42[a]**	**0.01207**	**±0.2**	**0.13**

[a] Excluding biasing current source
[b] Excluding current subtractor

In Figure 12, the drained currents from power supplies V_{DD} and V_{SS} are presented to show the power efficiency of the introduced analog design. Figure 12 reveals that the maximum power consumption is calculated as 16.14nW since maximum drained current is equal to 80.71nA. On the other hand, the quiescent power

dissipation is 12.07nW as the minimum drained current from power supplies is 60.35nA.

The comparison of our proposed multiplier/divider with other multiplier circuit in literature is given in Table 1. According to Table 1, the suggested analog circuit has the advantage in terms of power consumption over all previous multipliers presented in Table 1 except the design in Ref [18]. Our suggested circuit has 42 transistors, whereas the design in Ref [18] has 60 transistors. In addition to these, the analog block has the ability of performing both multiplication and division operations.

4. Discussion and Conclusion

In this study, a low-voltage and low-power current-mode multiplier/divider circuit design is suggested. The two-input one-output analog circuit requires the power supply voltages of ±0.2V and comprises of only 3 OTAs. OTA structure employs 8 DTMOS transistors and 6 NMOS transistors excluding one biasing current source. The analog multiplier/divider block consists of 42 transistors in total since each OTA structure has 14 transistors. The quiescent power dissipation is 12.07nW as minimum drained current from the power supplies is 60.35nA thanks to utilizing DTMOS transistor. The analog amplitude modulator and frequency double circuit are demonstrated as application examples in order to express the performance of the multiplier/divider. The introduced analog design has the advantage in terms of power consumption and/or the number of required transistors over previous multipliers. In addition to these, the analog block has the ability of performing both multiplication and division operations. Simulation results obtained in this study agree well with the expected results.

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