Nested Miller Compensation Based Op-Amp Design for Piezoelectric Actuators

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***Abstract*—This study introduces the design of a practical three-stage operational amplifier (op-amp) using nested Miller compensation, particularly for piezoelectric actuators. Driving a piezoelectric actuator represents a challenge in amplifier design due to its large capacitive nature. A stable piezo driver needs to be free of oscillations and phase lag. Direct feedback compensation using a conventional Miller capacitor is an effective method as long as the capacitance of the load is considerably close to the value of the Miller capacitor. However, using a large capacitor causes a decrease in the slew rate and gain bandwidth. To avoid this, our design focused on the utilization of nested Miller compensation technique. A prototype of the design working at 100V peak to peak voltage (V_{pp}) is implemented using commercial off-the-shelf (COTS) components. The measurements show the successful driving capability and step-response of the op-amp design. In the design, Widlar current source is also utilized for thermal stability and short circuit protection. According to simulation results, the proposed op-amp has a slew rate of 0.5 V/µs, an open loop gain of 90dB with 3MHz Gain Bandwidth Product (GBP) and phase margin of 77°, and a common mode rejection ratio (CMRR) of 62dB.**

Index Terms—**Operational Amplifier, Stability, Piezoelectric, Actuator, Piezo Driver**

I. INTRODUCTION

THE WIDESPREAD use of piezoelectric actuators in diverse applications stimulate significant research efforts for the development of piezo drivers with high linearity and low-cost [1-3]. Due to their unique capability to make displacement in nanoscale, piezo materials are widely used in many scientific applications including atomic force microscopy (AFM), scanning tunneling microscopy (STM), nano- and micromanipulators, and optical microscopy stages [4-6]. In addition to its expanding use in scientific applications, piezoelectric materials have already been utilized in many consumer products, such as inkjet printers, lenses of the smartphones, lasers, fuel injectors, touch sensors, ultrasonic cleaners, etc [2,7-11]. Piezoelectric transducers are made up of dielectric materials with the ability to convert mechanical stress into electrical signals and vice versa. Typically, a standard piezoelectric crystal will expand at nanometer scale per a certain voltage applied. The piezoelectric materials inherently act as a capacitive element (typically 0.01 microfarad or more) and their drivers require considerably high voltage range that may not be easily handled by integrated systems. The piezoelectric materials exemplify a non-ideal type of load for conventional op-amp designs because of their large capacitance. Additionally, in piezoelectric materials, mechanical resonances appear at the frequency range varying from kHz to MHz [11]. This implies that the instability in op-amp operation can induce oscillations at high frequencies and this phenomenon may also trigger undesired mechanical resonance.

The aim of this study is to build an op-amp to drive large capacitive loadings at a wide range of frequency and voltage. Nested Miller compensation, short circuit protection, and overtemperature operation are exclusively considered in the design. Particularly, Miller and nested Miller compensation techniques are compared in detail. To demonstrate the validity of the techniques provided, the design is implemented using commercial off-the-shelf (COTS) circuit components. The circuit built by COTS components is powered by a peak to peak supply voltage (V_{pp}) of 100V, has a common mode rejection ratio (CMRR) of 62 dB, 0.5 V/µs slew rate, and open loop gain value of 90 dB with 3MHz bandwidth and 77° phase margin. Well-known transistor types (MMBTA42 and its complementary MMBTA92) are preferred in the prototype to show the feasibility of the system and to reduce the complexity of the implementation for scientists and engineers from diverse fields.

A typical op-amp involves a differential amplifier, voltage gain, level shifter, and power output stages. The three-stage design provided in this study has an additional differential amplifier stage to achieve higher gain. Combination of each stage is supposed to provide efficiency and linearity in

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Manuscript received July 02, 2019; accepted March 13, 2020.
DOI: 10.17694/bajece.585798

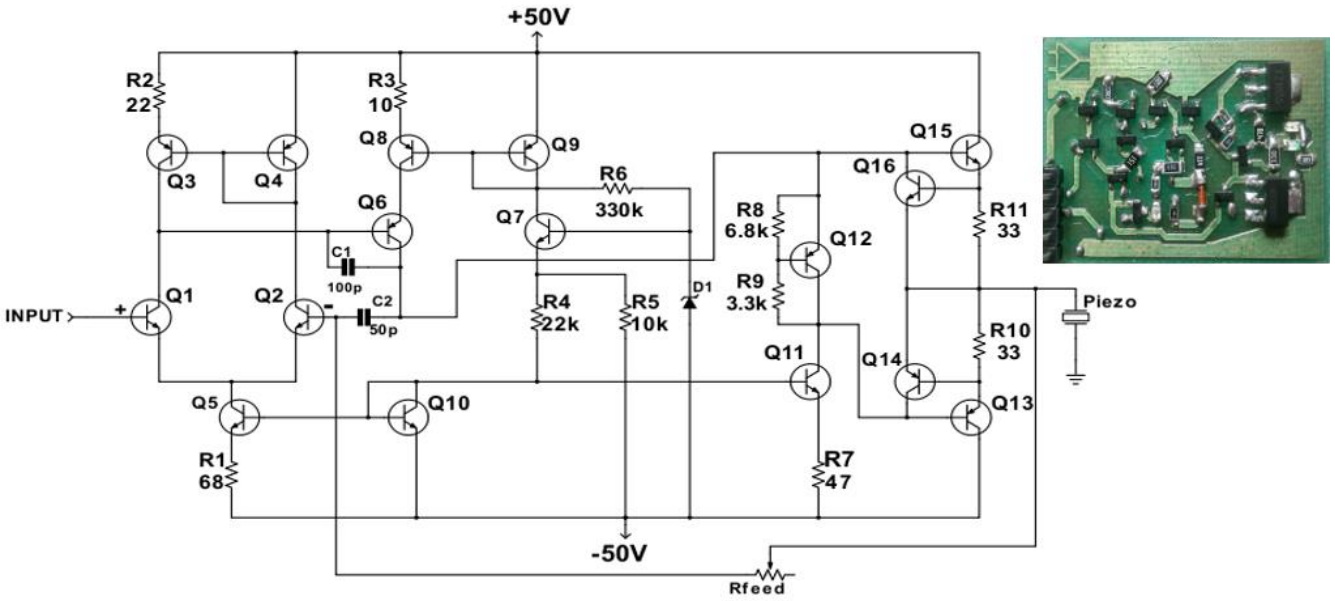

Fig. 1. *Op-amp Circuit Diagram. The inset shows the picture of the op-amp module*

amplification. The output stage has a Class AB amplifier configuration with two complementary transistors (FZT 855 and its complementary FZT955). The stability of the amplifier is directly associated with the compensation. Direct feedback compensation using a Miller capacitor is a well-studied concept, especially in CMOS based integrated circuits [12-14]. Miller compensation relies on the pole-splitting principle and no doubt, it efficiently solves the instability issues in many applications. Piezoelectric materials are of non-ideal loads for conventional op-amps. Their capacitance is large and subject to changes with varying voltage. Miller compensation technique using a single capacitor turns out to be not functional if the capacitance of the load is much greater than the value of the Miller capacitor. Increase in the Miller capacitor to improve the stability have adverse impacts on slew rate and gain bandwidth [15-18]. Considering the large capacitance of piezoelectric actuators as well as their varying capacitance under bias, the op-amp design given here utilizes nested Miller compensation technique. The major advantage of the nested Miller compensation is that stability can be improved with smaller capacitors and the speed of op-amp operation is considerably not affected by the compensation [15,16].

In a similar manner with many electronic devices working at high voltages, short circuit protection stands as an essential part of the op-amp design to ensure the reliability in extreme operating conditions. Widlar circuit with Class AB power amplifier configuration is utilized for short circuit protection and also ensures the overtemperature operation of the op-amp. The Widlar approach is important particularly in high-temperature applications to ensure the reliable operation of the instrument at non-standard thermal conditions [19].

II. Circuit Design and Prototyping

Fig. 1 shows the circuit schematic of the piezo driving op-amp with a picture of the prototype. The input stage of the op-amp circuit is a conventional n-type differential amplifier driven by a current source pair (Q3 and Q4). Inverting and noninverting inputs are respectively the bases of Q1 and Q2 with internal feedback capacitors (C1 and C2) and external feedback resistor (Rfeed). Rfeed is a zero-nulling resistor for nested Miller compensation. A current mirror consisting of Q5, Q10, and Q11 transistors yields to a bias current of 0.5mA. This part of the design is a Widlar current source, which is widely used to produce small current values using small resistors [19,20]. Widlar circuit is extensively utilized in integrated circuits because it effectively ensures the temperature stability and short circuit protection with small resistors. Q5 is the current sink for the differential pair and produces 0.25 mA bias current for both Q1 and Q2. Q8 and Q9 form another current mirror which provides 0.5 mA bias current for amplifier transistor Q6. 6.2V Zener is used for voltage regulation and also for sourcing the current. It eliminates the fluctuations at the voltage and prevents the system from abnormal changes at the current value. A stable current of 0.77mA can be observed from both Q10 and Q9 current mirror transistors. R6 sustains suitable current for Zener diode whereas R1, R4, and R5 provide 0.5 mA bias current for Q5 as sink current for the differential pair. R8 and R9 are the V_{BE} multiplier to eliminate crossover distortion for the output stage. Q13 and Q15 are the output power transistors with current limiter transistors Q14 and Q16. The output stage of the op-amp is a Class AB amplifier with temperature tolerable short circuit protection. R11- Q16 and R10 - Q14 pairs are the current limiters and constrain the output current

at about 15 mA. C1 is the Miller capacitor utilized for the direct compensation of the operational amplifier. C2 is the supporting compensation capacitor that shows derivative characteristics with the zero nulling-feedback resistor (Rfeed). Combination of C1 and C2 capacitors presents the nested Miller compensation circuitry. Well-known BJT transistors are utilized in the prototype for simplicity. Class AB amplifier consists of an FZT 855 (Q15) and its complementary FZT955(Q13), and the rest of the circuit have MMBTA42 and its complementary MMBTA92. While choosing the components, their costs, availability in the market, low voltage drop and functionality at high voltage were assessed.

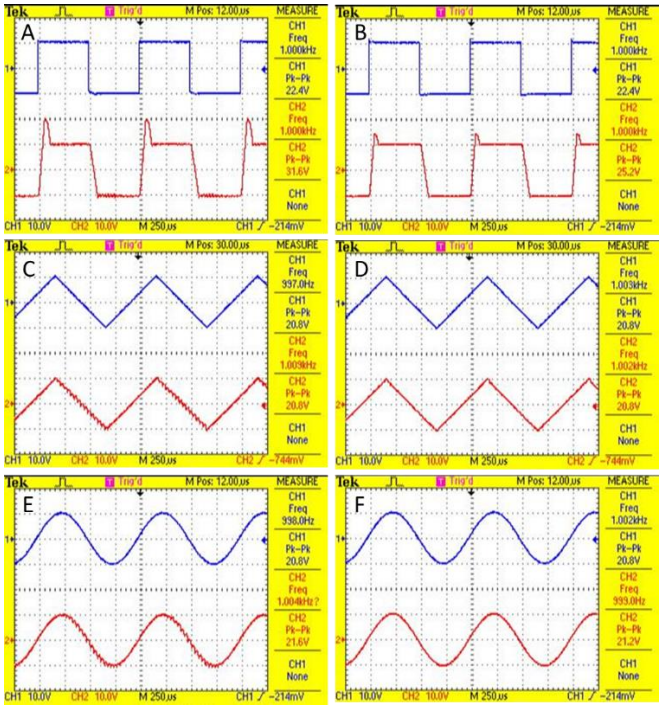

Fig. 2. *Output voltage characteristics of a 47nF piezoelectric load with a) Miller compensation for 1kHz square wave input at unity gain, b) nested Miller compensation for 1kHz square wave input at unity gain, c) Miller compensation for 1kHz triangular wave input at unity gain, d) nested Miller compensation for 1kHz square wave input at unity gain, e) Miller compensation for 1kHz sinusoidal wave input at unity gain, f) nested Miller compensation for 1kHz sinusoidal wave input at unity gain. (Blue lines are inputs, whereas red lines represent outputs)*

In a piezo driving amplifier, the output voltage is limited by the output impedance and instability might occur due to the large capacitance of the piezoelectric materials. The quality of the op-amp highly depends on the compensation. Direct compensation with Miller capacitor is the primary choice for many amplifier designs [12,14]. The capacitance of the load is very important while determining the value of the Miller capacitor. Principally, the capacitance of the load is not supposed to be much greater than the value of the Miller capacitor. The step-response degrades with the increase in the Miller capacitor. When nested Miller compensation technique is used, the value of the capacitor used for the compensation significantly decreases. This phenomenon is an advantage when the system speed and die size are considered [15-18]. Especially in CMOS design, smaller capacitor is preferred since it occupies less are in the layout. When the stability becomes an issue for commercial op-amps, several external compensation techniques can be considered. One of the common external compensation techniques is using an integrator at the output by utilization of an external capacitor and a resistor. This technique is not convenient when the size, cost, and speed is a concern. To our knowledge, the proposed circuit design introduces nested Miller compensation for piezo drivers for the first time in the literature. The circuit involves nested Miller compensation with C1 and C2 capacitors to improve the stability of the output signal. As shown in Fig. 1, Miller and supporting compensation capacitors are 100pF and 50pF, respectively. The novelty of this research is the use of small capacitors for compensation of a system that has a capacitive loading of 47nF. Nested Miller compensation allows the use of small capacitance to reduce the oscillations and overshoot. The op-amp design has 0.5 V/μs slew rate and 1 MHz Gain Bandwidth Product (GBP). By tuning C1 and C2 capacitors as well as zero nulling resistor (Rfeed) connected to the compensation circuitry, the op-amp can be modified to work for a variety of piezoelectric materials without significant degradation of the step-response.

Especially for large capacitive loads, control of oscillations at the output voltage becomes a crucial task to be examined for a universal piezo driver design. To determine the technical specifications and to understand the stability of the op-amp prototype, a number of measurements were conducted using Agilent 33220A Signal Generator, Tektronix TDS 2022B Oscilloscope, Agilent 34405A Multimeter, and Agilent E3648A DC Power Supply. R_{feed} value is maintained at 100kΩ during the measurements. Output voltage characteristics obtained from the prototype for various types of signals are shown in Fig. 2. Compensation at systems with multiple poles is frequently done by the domination of one of the poles [12]. Miller compensation determines a dominant pole via pole-zero cancellation [20]. When a capacitive load (47nF) is inserted into the output of the op-amp, oscillations are observed besides overshoots at the step response in the compensation configuration with a single Miller capacitor of 100pF (Fig. 2a, 2c, and 2e). Fig. 2b, 2d, and 2f show the results with nested Miller compensation. Nested Miller compensation with two capacitors brings additional zeros to the system. The output voltage characteristics show that Miller compensation using a single transistor may not be adequate to lower the oscillations. Instead of increasing the value of the Miller capacitor, we used nested Miller compensation capacitor (C2) not to affect step-response characteristics, and so the slew rate. In principle, the effect of the poles on the imaginary axis of the root locus must be eliminated by the zeros coming from the nested

compensation by the means of pole-zero cancellations. Basically, nested Miller compensation introduces complex zeros to the system. The roots causing undamped oscillation must be much greater than the roots causing underdamped oscillation. In an uncompensated system, the poles go into the right-hand plane (RHP) for higher gain and the system becomes unstable [15,20]. With the nested Miller compensation, purely imaginary poles do not affect the stability, and op-amp becomes stable at a high gain range. As also stated by Baker et al, the left-hand plane (LHP) zeros improve the speed of the op-amp [15].

III. Compensation and Zero Nulling Resistor

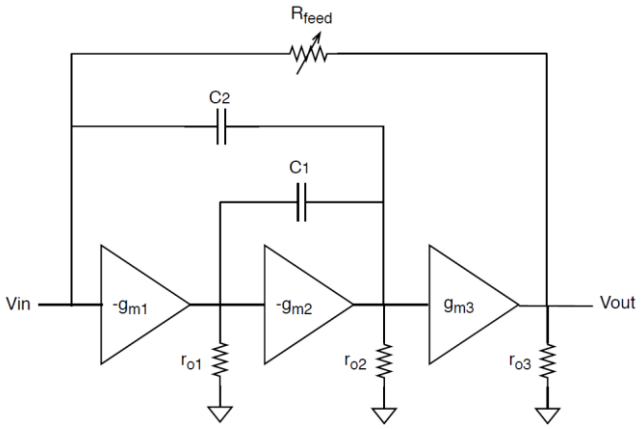

Fig. 3. *Block Diagram of the proposed three-stage opamp.*

Fig. 3 shows the symbolic block diagram of the proposed three-stage opamp. g_{m1}. g_{m2}, and g_{m3} refer to the transconductances of the stages, whereas corresponding output impedances are given by r_{o1}, r_{o2}, and r_{o3}. C1 and C2 forms the nested Miller compensation and Rfeed is the zero nulling resistor. Small-signal analysis of the system given in Fig. 1 provides a straightforward approach to find the transfer function of the proposed three-stage opamp [16,17].

The transfer function of the opamp with nested Miller compensation configuration is given in Eq.1.
where the voltage gain A_0 can be expressed by the following equation.

$$A_0 = g_{m1}g_{m2}g_{m3}r_{o1}r_{o2}r_{o3} \quad (2)$$

It is important to note that if the capacitive loading is taken into account in the transfer function, the expression in Eq. 1 will not change. Assuming two poles are widely separated, the denominator of Av(s) is used to find out the poles via the equation given in Eq.3.

$$D(s) = 1 + \frac{s}{\omega_{p1}} + \frac{s^2}{\omega_{p1}\omega_{p2}} \quad (3)$$

Thus, from the transfer function, the dominant pole, ω_{p1}, is simplified to

$$\omega_{p1} = \frac{1}{g_{m2}C_1r_{o1}r_{o2} + C_1r_{o1} + C_1r_{o2} + g_{m3}C_2r_{o2}r_{o3} + C_2R_{feed} + C_2r_{o3} + C_2r_{o2}} \quad (4)$$

and in a more simplified form:

$$\omega_{p1} \cong \frac{1}{g_{m2}C_1r_{o1}r_{o2} + g_{m3}C_2r_{o2}r_{o3}} \quad (5)$$

The numerator of Av(s) provides the function for the zero.

$$\omega_z = \left(C_2R_{feed} - \frac{C_1}{g_{m2}} - \frac{C_2}{g_{m3}}\right)^{-1} \quad (6)$$

RHP zero cancellation can be done via using R_{feed} resistor connected to both input and output.

$$R_{feed} = \frac{C_1}{C_2g_{m2}} + \frac{1}{g_{m3}} \quad (7)$$

When large capacitive loading is taken into account, zero becomes identical

$$\omega_z' = \left(C_LC_2R_{feed} - \frac{C_LC_1}{g_{m2}} - \frac{C_LC_2}{g_{m3}}\right)^{-1} \quad (8)$$

Thus, Rfeed value is independent of the loading but determined by C1 and C2 values as well as g_{m2} and g_{m3}. In a similar way with Mita et al., the relation between C1, C2 and CL is assumed as give below to achieve a reasonable phase margin.

$$C_2C_L > C_1^2 \quad (9)$$

$$Av(s) = A_0 \frac{1 + \left(C_2R_{feed} - \frac{C_1}{g_{m2}} - \frac{C_2}{g_{m3}}\right)s + \left(\frac{C_1C_2}{g_{m2}g_{m3}} - \frac{C_1C_2}{g_{m2}}\right)s^2}{\begin{aligned}1 &+ (g_{m2}C_1r_{o1}r_{o2} + C_1r_{o1} + C_1r_{o2} + g_{m3}C_2r_{o2}r_{o3} + C_2R_{feed} + C_2r_{o3} + C_2r_{o2})s \\ &+ (g_{m2}C_1C_2r_{o1}r_{o2}R_{feed} + g_{m2}C_1C_2R_{feed} + g_{m3}C_1C_2r_{o1}r_{o2}r_{o3} + C_1C_2r_{o2}R_{feed} + C_1C_2r_{o2}r_{o3} + C_1C_2r_{o1}R_{feed} \\ &+ C_1C_2r_{o1}r_{o3} + C_1C_2r_{o1}r_{o2})s^2\end{aligned}} \quad (1)$$

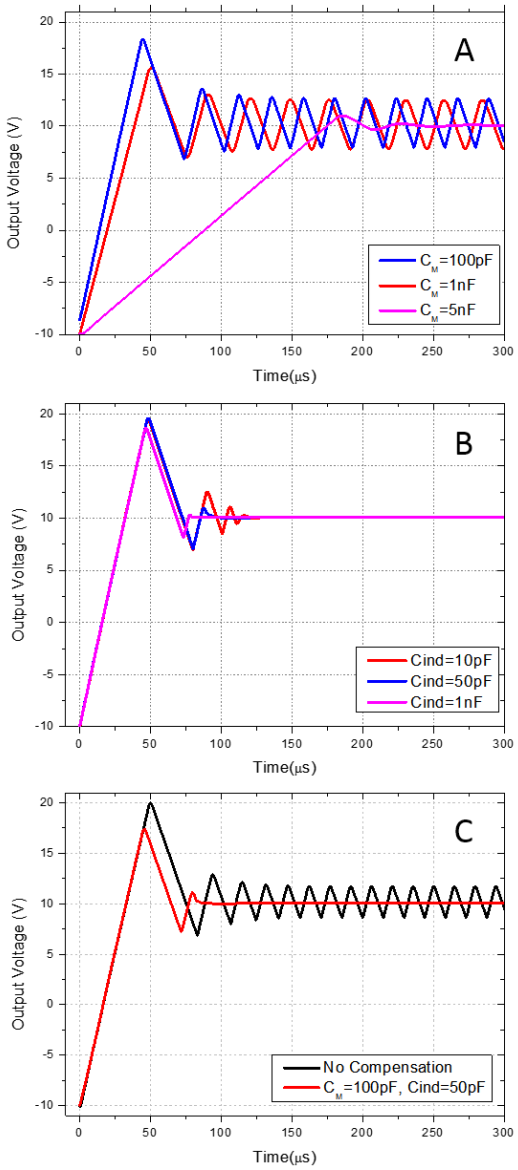

Fig. 4. *Step response simulations of the op-amp with (a) only Miller capacitor (C_M) and (b) additional capacitor to form nested Miller (C_{ind}). (c) Comparison of a non-compensated op-amp with the nested Miller compensated using the same capacitance values with the prototype.*

IV. Simulation Results

The measurements collected for various scenario is confirmed via the simulations done in LTSpice using the models of the components used in the prototype (i.e. MMBTA42, MMBTA92, FZT 855, FZT955). In simulations, a 47nF capacitor is used for mimicking the piezoelectric material loading and R_{feed} value is kept at 100kΩ. Direct compensation with Miller capacitance is a very convenient method, however, the stability of the system can be ensured at capacitances very close to the loading capacitance. When the loading has large a capacitance, like piezoelectric materials, an adverse impact of using a single Miller capacitor on the processing speed can be observed drastically, as shown in Fig.4a. Instability in the signal brings up mechanical vibrations associated with the resonance frequency.

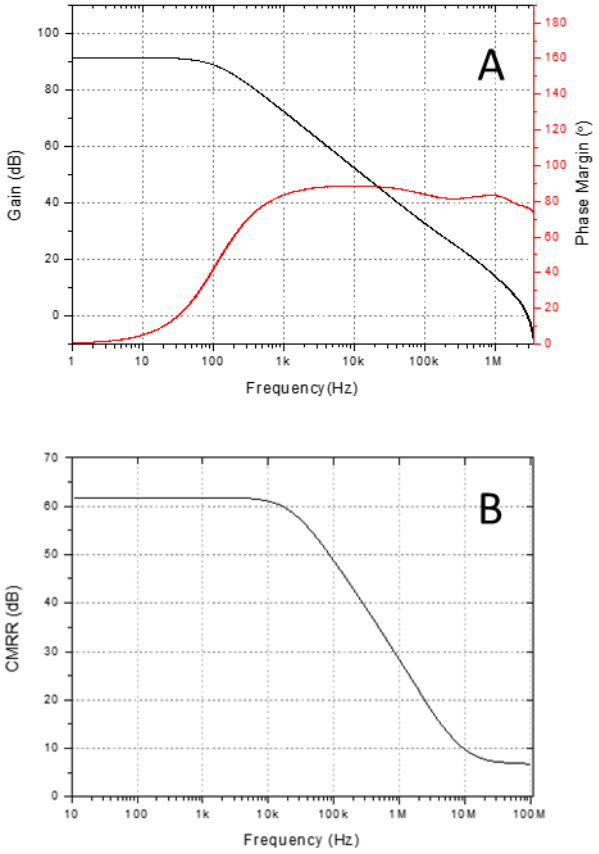

Fig. 5. *a) Open loop gain vs. frequency and phase margin plots b) Common mode rejection ratio (CMRR) vs. frequency*

Fig.4a illustrates step responses to exemplify the use of direct compensation with various values of Miller capacitors. With the increase at the value of Miller capacitors, overshoot settles down, however, the step response shows that the speed of the system decreases drastically and oscillations do not disappear with the use of small Miller capacitors. Fig. 4b shows the utilization of a supporting capacitor without the original Miller capacitor. Utilization of the supporting capacitor at the pF level effectively reduces the oscillations. As shown in Fig. 4b, insertion of an additional compensation capacitor eliminates a significant amount of oscillations, but increasing the value of the supporting capacitor from 50pF to 1nF does not make significant improvements in the overshoot. As compared with the Miller compensation, nested Miller compensation provides remarkable progress at the oscillation cancellation, but it does not remove the significant portion of the overshoot. Miller capacitor is very effective on the reduction of overshoot whereas nested Miller compensation is more advantageous for the step response. Consequently, combining two capacitors can be used to enhance the stability of the system, so step response and overshoot can be adequately compensated. Fig. 4c demonstrates how a non-compensated system is stabilized

using a single Miller capacitor and the configuration for the nested Miller compensation.

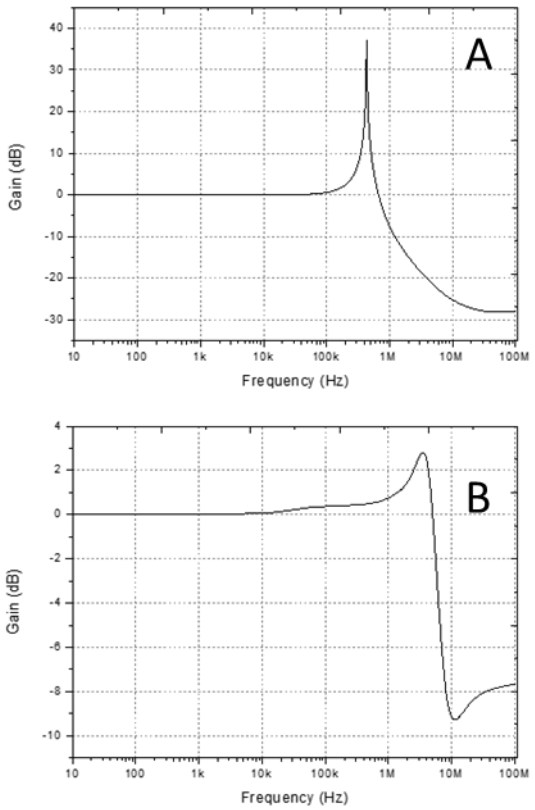

Fig. 6. *Frequency responses at unity close loop gain a) only with the presence of Miller Capacitor (C1=100pF, No C2, A_{VCL} = 1 V/V) b) with nested Miller compensation (C1=100pF, C2=50pF, A_{VCL} = 1V/V)*

V. Frequency Response Characteristics

Bode plot recorded at open loop gain is shown in Fig. 5a. Accordingly, open loop gain value of 90 dB with 3MHz bandwidth and 77° phase margin is achieved in the design. The common mode rejection ratio (CMRR) is one of the parameters defining the quality of the op-amp. CMRR is calculated by the ratio of differential voltage gain to common mode voltage gain. The op-amp design given here has CMRR of 62dB, as shown in Fig. 5b. The plotted CMRR expresses the capability of differential-mode amplification whereas the common-mode voltage is excluded.

Fig. 6a shows the frequency response of the amplifier in case only Miller compensation is used (C2 removed from the circuit in Fig. 1). The plot suggests that the amplifier gradually becomes unstable after 100 kHz and reaches resonance frequency at around 400 kHz. At the resonance frequency, oscillations can be observed at the output voltage characteristics and this induces an excessive gain in the system. Resonance in the signal causes mechanical vibrations which result in undesired motions in the piezoelectric positioners, stages, and actuators. In case only 100pF Miller capacitor is used, the recommended operating range of the op-amp would be limited to 100 kHz due to the resonance frequency. As the Miller capacitor is increased the stability of the system improves, but the capacitance value will be very large and it will have adverse impacts on the speed of the op-amp [15-18].

Impact of the nested compensation on resonance frequency is evaluated in detail. As shown in Fig. 6b, the resonance frequency is shifted to about 3.5 MHz when nested compensation is used. The excessive gain previously observed at 400kHz considerably decreases and becomes a tolerable value (~0.5dB) for stable operation. As compared to the system with regular Miller compensation, bandwidth and stability are improved at the higher frequencies with the addition of a 50pF supporting capacitor.

VI. Conclusion

Piezoelectric positioners with high precision movement ability are of emerging technologies in metrology and instrumentation. Accurate control of the positioners in micro and nanoscale without mechanical resonance is only possible with highly stable op-amps. The three-stage op-amp design provided in this context introduces a feasible technique to build a fundamental part of the piezoelectric_positioner controllers. Without the requirement of a dedicated semiconductor manufacturing line, the op-amp can be produced using COTS components. The challenge with piezoelectric materials is their large capacitance and resonance frequency. The conventional direct (Miller) compensation may not bring out ultimate solutions to oscillations when the capacitance of the load is greater than Miller capacitance integrated into the circuit. Experimental results showed that the stability of the op-amp is improved by nested Miller compensation. In the prototype design, regular Miller capacitor reduces the overshoot whereas nested compensation is more beneficial to eliminate the oscillations while maintaining the step-response. Additionally, features for short circuit protection and temperature stability enable the use of designed opamp in extreme conditions. In conclusion, the rail-to-rail op-amp design covered in this study can be modified for the diverse use of piezoelectric materials in scientific instrumentation.

VII. Acknowledgment

This work is financially supported by Hacettepe University BAP under FAY-2017-14008.

VIII. References

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