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THERMAL SPREADING PERFORMANCE OF GaN-ON-DIAMOND SUBSTRATE HEMTS WITH LOCALIZED JOULE HEATING

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Abstract: Diamond is the new substrate of choice for high power/frequency AlGaN/GaN high electron mobility transistors (HEMTs). Due to its high thermal conductivity, diamond presents improvements in removing concentrated heat from the electron channel, a necessity for reliable performance of these devices. Previous thermal performance comparison studies of GaN-on-SiC and GaN-on-diamond devices are limited to devices with often large and identical heat source regions due to modeling and experimental limitations. Analytical procedure presented in this study overcome these limitations and provide a more comprehensive thermal spreading performance analysis of GaN-on-SiC and GaN-on-diamond HEMTs with localized Joule heating. Important thermal spreading factors such as thermal boundary resistance, GaN buffer layer thickness, and multifinger arrangements are also investigated in this study.
Keywords: HEMTs, substrate effects, diamond, Joule heating.

YOĞUNLAŞMIŞ ISINMALI VE ELMAS ALTTAŞLI GAN HEMT'LERİN ISI DAĞITMA PERFORMANSI

Özet: Elmas yüksek güç ve frekans AlGaN/GaN yüksek elektron mobiliteli transistörler (HEMTs) için son zamanlarda tercih edilen alttaş malzemesidir. Yüksek ısıl iletkenliği ile elmas aygıt güvenirliği için gerekli olan elektron kanalındaki yoğunlaşmış ısının dışarı taşınmasında iyileştirmeler sunar. Önceki SiC ve elmas alttaşlara sahip GaN aygıtların ısıl karşılaştırma çalışmaları deneysel ve modelleme konusundaki sınırlamalar nedeniyle büyük ve tep tip ısı kaynağına sahip aygıtlarla sınırlandırılmıştır. Bu çalışmada sunulan analitik çalışma ile bu sınırlamaların üstesinden gelerek SiC ve elmas alttaşlı ve yoğunlaşmış ısınmalı GaN aygıtların ısıl karşılaştırmalarını daha detaylı bir şekilde gerçekleştrimeye olanak sağlar. Isı dağılımına etki eden katmanlar arası ısıl dirençlerin, GaN katman kalınlıklarının ve çok sayıda parmağa sahip aygıtlardaki parmak sayılarının etkileri bu çalışmada incelenmiştir.
Anahtar Kelimeler: HEMTler, alttaş etkileri, elmas, Joule ısınma.

NOMENCLATURE

k	Thermal conductivity [W/mK]
R	Thermal Resistance [k/W]
Q	Heat Generation [W]
T	Temperature [K]
a	Die width [μm]
b	Die Length[μm]
t	Layer Thickness [μm]
c	Heat source width [μm]
d	Heat source half length [μm]
x_c	Half finger spacing [μm]

INTRODUCTION

AlGaN/GaN high electron mobility transistors (HEMTs) are among the most investigated solid-state electronic devices in high power and frequency applications. They are the first replacement choice for the silicon laterally diffused metal oxide semiconductor (LDMOS) transistors and GaAs pseudomorphic HEMTs (pHEMT) in radio frequency and microwave applications because of their high electron mobility and breakdown fields (Lidow, 2013). Yet there are still serious concerns about the reliability and mean-time-to-failure (MTTF) of these devices. High temperatures in two-dimensional electron gas (2DEG) region are considered to be one of the major reasons for the limited device reliability. Localized heat source regions are the main reasons for such high temperatures.

Using a high thermal conductivity substrate, such as diamond, is among the most successful approaches that can be used to reduce the temperatures and increase the reliability of HEMTs. In the past, 25% to 50% reduction in channel temperature rise was observed for devices built with GaN-on-diamond substrates compared to conventional GaN-on-SiC technology (Felbinger et al., 2007; Hirama, Kasu and Taniyasu, 2012; Dumka et al., 2013; Pomeroy et al., 2014). Although past studies proved that the operating power and a combination of geometrical parameters such as;

finger number/spacing and material thicknesses are important for the thermal efficiency of GaN-on-Diamond HEMTs (Guo et al., 2017; Felbinger et al., 2007), little has been said about the impact of localized Joule heating on this thermal efficiency. Localized Joule heating occurs under the drain edge of the gate when device is biased at a relatively low gate voltage. In such cases, the size of the localized heat source region in a device can be as small as 50 nm (Venkatachalam et al., 2011) yet it may extend when higher gate and/or drain biases are applied (Pomeroy et al., 2015). When the heat source region is very small, thermal resistance of the device is dominated by the thermal spreading resistance which reduces the thermal advantages of diamond substrates over traditional SiC substrates. Thus to justify the usage areas of the new and expensive GaN-on-diamond technology as a substitute for conventional SiC technology with significantly lower fabrication costs, it is important to characterize its thermal spreading performance at all biasing conditions, including the ones which results in extremely localized Joule heating.

Thermal spreading performance of GaN-on-Diamond devices is strongly affected by the diamond's thermal conductivity (k) and the effective thermal boundary resistance (TBR). Although progress has been done in the area of single crystalline diamond substrates with extremely high thermal conductivity (Dussaigne et al., 2010), polycrystalline hot filament (HF), with k = 620 ± 50 W/(m.K) (Sun et al., 2015), and microwave (MW) chemical vapor deposited (CVD) diamond, with k = 1500 ± 300 W/(m.K) (Angadi et al., 2006; Dumka et al., 2013; Sun et al., 2015) are still preferred due to scalability and economic reasons (Jessen et al., 2006; Ejeckam et al., 2014; Sun et al., 2015). In all substrate-GaN integration processes, acoustic mismatch between the materials, formation of defects near the nucleation regions, and the presence of the nucleation/ bonding/ strain reliever layers (Cho et al., 2013) build a thermal barrier, known as thermal boundary resistance (TBR), between GaN and the substrate. Silicon Carbide, with a considerably lower thermal conductivity of k≈450 W/(m·K) (Dumka et al., 2013), may possess TBR as low as TBR=0.4 – $0.5 \cdot 10^{-8}$ m^2K/W (Cho et al., 2012) with the small lattice mismatch achieved through advanced technology. Yet in latest commercial devices this value is still as high as TBR ~ $2 \cdot 10^{-8}$ m^2K/W (Manoi et al., 2010; Killat et al., 2014). Due to their different crystallographic states, challenges exist in GaN and diamond integration causing higher TBR. For instance, GaN-on-MW diamond devices' strain relieving parts can be major source of thermal boundary resistance. Previously, TBR = $3 \cdot 10^{-8}$ m^2K/W (Cho, Li, et al., 2012; Anaya et al., 2016) is reported for GaN-on-diamond HEMTs. Lower TBR = $1.2 \cdot 10^{-8}$ m^2K/W is also reported when the nucleation layer thickness is reduced (Sun et al., 2015). In general, lower TBR is preferred to get the highest advantage from high conductivity substrates. Premature thermal spreading that results from using thinner GaN epilayers to decrease the distance between heat source regions and diamond substrates (Felbinger et al., 2007) can collide to this thermal barrier, which can result in further increase in the thermal resistance. Therefore, not only the TBR, but also the combination of the TBR and GaN thickness, typically in the range of 0.5-2 µm, is important in the thermal performance of devices.

To assess the advantage of diamond substrates when thermal spreading effects are dominant, devices with localized Joule heating with realistic thermal conductivity and TBR values are analyzed in this study. In addition to these variables effects of GaN epitaxial layer thickness and multifinger configuration to the thermal spreading performance of GaN-on-Diamond are studied. In order to analyze above listed numerous device parameters, an analytical approach developed in a former study is used (Azarifar and Donmezer, 2017).

METHOD

Since the highest temperatures and most of the thermal spreading occur in GaN and the substrate layer, this study will be limited to thermal characterization of the device and its substrate only. Fig. 1c is the illustration of the two-finger device configuration used for the thermal performance comparison study. Due to symmetry of the device and the boundary conditions (as shown in the Fig. 1a) only quarter of the device (shown in Fig. 1c) is modeled.

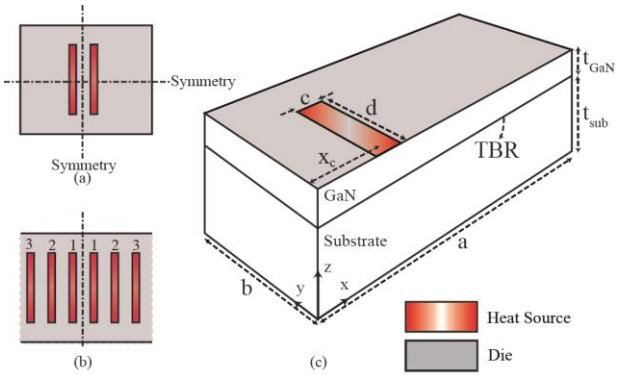

Figure 1. Top view of the (a) two finger and (b) multifinger devices analyzed in this study. (c) Quarter model of the two-finger device. Heat source region with the size of c × d is positioned at a distance xc from the center of the die in the quarter model. t_{GaN} and t_{sub} are the thickness of the GaN and substrate layer, respectfully. TBR is set between the GaN and substrate layers.

In the second part of the study a multifinger device represented in Fig. 1b is modeled to observe the effects of multiple fingers on thermal performance of devices. To conserve the symmetry of the device in quarter model approximation even number of fingers are modeled only.

Two-Finger Device

The rectangular regions shown on the surfaces of the structures in Fig. 1 represent the heat source regions due to localized Joule heating in devices. In thermal model surface heat flux is applied through these regions with

Table 1. Properties used in different studies

	Heat Source		Finger Spacing		Epitaxial Properties	
	c	d	x_c	Finger	t_{GaN}	TBR
Study	nm	µm	µm	Number	µm	$m^2K/Wx10^8$
1	50-1000	50-100	30	2	1	2
2	50	50	30	2	0.5-2	0-5
3	50	50	10-200	2	1	2
4	50	50	10-60	2-20	1	2

dimensions of c x d placed at a distance x_c from the left symmetry plane. Total thermal resistance, R=ΔT/Q [K/W], where ΔT is the temperature rise [K] at the heat source region and q [W] is the total power dissipated from this region is used in this study to compare thermal performances of devices independent of the amount of total power dissipated. Heat spreading from these small heat source regions to a realistic 800 µm square (a x b = 400 µm x 400 µm in the quarter model) is defined with the spreading thermal resistance (R_s). After spreading heat is conducted to the bottom of the substrate through the GaN and substrate layers with thicknesses of t_{GaN} and t_{sub} respectively, which is described by the one-dimensional thermal resistance (R_{1D}). While the thickness of the substrate is kept constant t_{sub} = 100 µm based on reference (Dumka et al., 2013) the GaN layer thickness will be varied to investigate the effect of GaN thinning on the device thermal performance. This one-dimensional resistance also includes the effective thermal boundary resistance (TBR) between the GaN and the substrate layers. As shown in Eq. (1) the total thermal resistance, R can be found by adding these resistances.

$$R_s + R_{1D} = R \tag{1}$$

In which R_{1D} and R_s can be evaluated using the geometrical parameters in Fig. 1 by Eq. (2) and Eq. (3) respectively (Muzychka et al., 2013):

$$R_{1D} = \frac{t_{GaN}}{k_{GaN}ab} + \frac{t_{sub}}{k_{sub}ab} + \frac{TBR}{ab} \tag{2}$$

$$\begin{aligned} R_s = {} & 2\sum_{m=1}^{\infty} A_m \frac{\cos(\lambda_m x_c)\sin(cd/4)}{\lambda_m c} \\ & + 2\sum_{n=1}^{\infty} A_n \frac{\cos(\delta_n d/2)\sin(\delta_n d/2)}{\delta_n d} \\ & + 4\sum_{m=1}^{\infty}\sum_{n=1}^{\infty} A_{mn} \frac{\cos(\lambda_m x_c)\sin(\lambda_m c/2)\cos(\delta_n d/2)\sin(\delta_n d/2)}{\lambda_m c \delta_n d} \end{aligned} \tag{3}$$

In Eq. (2) k_{sub} is the thermal conductivity of the substrate layer; k_{SiC}, k_{HF}, or k_{MW}, which are 450, 620, or 1500 W/(m·K) respectively and TBR is the thermal boundary resistance between the GaN and the substrate. Finally, $\delta_n = n\pi/b$ and $\lambda_m = m\pi/a$ are the eigenvalues and A_m, A_n, and A_{mn} are calculated as (Muzychka et al., 2013):

$$A_m = \frac{4\cos(\lambda_m x_c)\sin(\lambda_m c/2)}{abck_{GaN}\lambda_m^2\phi(\lambda_m)} \tag{4}$$

$$A_n = \frac{4\cos(\delta_n d/2)\sin(\delta_n c/2)}{abdk_{GaN}\delta_n^2\phi(\delta_n)} \tag{5}$$

$$A_{mn} = \frac{16\cos(\lambda_m x_c)\sin(\lambda_m c/2)\cos(\delta_n d/2)\sin(\lambda_m d/2)}{abcdk_{GaN}\lambda_m\delta_n\beta_{mn}\phi(\beta_{mn})} \tag{6}$$

In Eq. (6) k_{GaN} is thermal conductivity of GaN, $\beta_{mn} = (\delta_n^2 + \lambda_m^2)^{0.5}$ is the eigenvalue and $\phi(\xi)$ is the spreading function specific to the perfect heat sink consideration (Muzychka et al., 2013):

$$\phi(\xi) = \frac{1 + TBR\cdot\xi k_{GaN}\cdot\tanh(\xi t_{GaN}) + \frac{k_{GaN}}{k_{Sub}}\tanh(\xi t_{GaN})\tanh(\xi t_{Sub})}{TBR\cdot\xi k_{GaN} + \frac{k_{GaN}}{k_{Sub}}\tanh(\xi t_{Sub}) + \tanh(\xi t_{GaN})} \tag{7}$$

Assuming constant substrate base temperature (T_{base}), average temperature of the die surface, ($\overline{T}_{S,die}$) can be evaluated using the calculated values of R_{1D} and heat generation (Q ~ Power/Number of Fingers) as in Eq. (8). On the other hand, R therefore R_S is required to obtain the average temperature of the heat source region ($\overline{T}_{source}$) using Eq. (9).

$$Q\cdot R_{1D} = \overline{T}_{s,die} - T_{base} \tag{8}$$

$$Q\cdot R = \overline{T}_{source} - T_{base} \tag{9}$$

The validity of the codes based on the above presented analytical method is verified using a finite element analysis program COMSOL Multiphysics in a previous study (Azarifar and Donmezer, 2017).

Multifinger Device

To analyze the thermal spreading performance of GaN-on-Diamond technology on multifinger devices with localized Joule heating, above methodology presented for the thermal resistance calculation of a two-finger device can be used with some variations. To evaluate the thermal resistance of the innermost fingers (fingers with index 1 in Fig. 1b) with highest temperature in

multifinger configuration, thermal effects of neighboring fingers should also be considered. Using the influence coefficient method introduced in (Muzychka, 2006), thermal resistance effect of each neighboring finger (shown in Fig. 1b with different index numbers) on the innermost finger can be evaluated and added to the thermal resistance of the innermost finger calculated using Eq. (1), (2), and (3) in which effects of neighboring fingers are not present. After obtaining the total thermal resistance for the innermost fingers temperatures can still be obtained using Eq. (8) and (9). This method can be used to estimate the total thermal resistance and temperature of not only the innermost device fingers but also all device fingers if needed. The validity of the codes based on the above methodology are verified using a finite element analysis program COMSOL Multiphysics in a previous study for multifinger devices (Azarifar and Donmezer, 2017).

Table 1 summarizes the studies performed to compare the thermal spreading performance of GaN-on-SiC and GaN-on-diamond devices with various configurations. These studies, divided into four major groups, will be explained next.

Study 1: Gate Width (d)

In this study, effects of changing gate width on the thermal performances of GaN-on-SiC, HF diamond, and MW diamond devices with localized Joule heating are investigated. For this study two-finger device configuration is used and die size is chosen as 800 µm to represent a realistic die. Although higher thermal resistances are observed for smaller dies, thermal resistance do not change significantly once the square die size reaches 800 µm. Thus the study presented here will be applicable to most devices with die sizes exceeding 800 µm.

Two gate widths (2 × d) of 100 and 200 µm are modeled and to simulate the heating effect of a real device under various operating conditions including the low gate voltage biasing two different heat source lengths c=50 nm and 1 µm are chosen. Under low gate voltage Joule heating characteristic of an amplifier cell is expected to be more localized, to represent this heat source, length of c = 50 nm is chosen. Inversely, during an open gate operating condition channel is fully open and heating is less localized thus heat source length is chosen as c = 1 µm. Since finger spacing ($2 \times x_c$) of 60 µm is a common value in GaN HEMT fabrication, its value along with the values of GaN and substrate thicknesses and TBR is kept constant throughout this first study. Values of the parameters used in this study are summarized in 1.

Study 2: Epitaxial Properties (t_{GaN} and TBR)

In this second study, the effects of GaN thickness and TBR on the thermal spreading performances of GaN-on-SiC, HF diamond, and MW diamond devices are investigated. Here all device dimensions are kept constant, and the study is performed for a device with smallest reported heat source region (c=50 nm) to compare the thermal performances of diamond substrates in devices with localized Joule heating. Values of the parameters used in this study are summarized in Table 1.

Study 3: Finger Spacing (x_c)

The effects of finger spacing on the thermal spreading performances of GaN-on-SiC, HF diamond, and MW diamond two-finger devices are investigated in the third study. Various finger spacing values from $2x_c$ = 20 µm-400 µm are modeled to investigate the effects of finger spacing. In this study all device dimensions are kept constant and study is performed for a device with smallest reported heat source region (c=50 nm) to compare the thermal performances for devices with localized Joule heating. The results are later compared with the results of multifinger devices. Important properties used in this study are presented in Table 1.

Study 4: Multifinger spacing

In this last study, effects of a multifinger (20 finger) configuration and finger spacing on the thermal spreading performances of GaN-on-SiC, HF diamond, and MW diamond devices are investigated. Thermal resistance on the innermost fingers is calculated in order to compare the results with the ones from the study of a device with only two fingers. The finger spacing is varied between $2x_c$ = 10 µm – 60 µm. Important properties used in this study are presented in Table 1. By conducting a comparative study with the four study sets explained above, a comprehensive thermal spreading performance comparison of GaN-on-SiC and GaN-on-diamond devices with localized Joule heating is performed.

Table 2. Total thermal resistance values of GaN-on-SiC, GaN-on-HF, and GaN-on-MW devices and thermal resistance reductions achieved with HF and MW diamond substrates for devices with varying gate widths (d).

Heat Source		Total Thermal Resistance [K/W]			Resistance Reduction	
d [µm]	c [nm]	SiC	HF Diamond	MW Diamond	HF Diamond	MW Diamond
100	50	80.9	77.4	71.8	4.3%	11.2%
200		41.6	39.5	36.3	4.9%	12.6%
100	1000	49.1	45.6	40.0	7.2%	18.5%
200		25.7	23.6	20.4	7.9%	20.4%

RESULTS AND DISCUSSIONS

Gate Width (d)

In Table 2 total thermal resistances ($R = R_{1D}+R_s$) of GaN-on-SiC, HF diamond, and MW diamond devices with varying gate widths are summarized. When analyzed separately Rs is found to be as high as 200 times greater than the R_{1D}, for certain configurations, proving the importance of thermal spreading effects. The difference between R_{1D} and R_s decreases when the die size is reduced to the size of heat source region. However; in realistic cases, heat source region is much smaller compared to die size, thus; spreading thermal resistance becomes effective and total thermal resistance increases accordingly.

According to Table 2, smaller heat sources, with short gate length (d) and small c (due to localized Joule heating), lead to higher R_s in devices that cause significantly higher R of the device. Thus, although thermal resistance reduction as high as 20%, similar to literature (Felbinger *et al.*, 2007), can be achieved for a device with large gate width (d = 200 µm) operated with fully open channel conditions (c = 1 µm) with MW diamond substrates, its thermal reduction efficiency is almost halved for devices with shorter gate widths and localized heating. For same power density devices operating with low frequency (C-band, wireless), where longer gate widths are preferred, using diamond substrates will be less effective in reducing thermal resistance than for the devices operated in millimeter-wave where smaller gate widths are used to reduce phase lag (Francis *et al.*, 2010).

To sum up, the total thermal resistances of GaN-on-HF and GaN-on-MW devices is calculated to be up to 7.9% and 20.4% lower respectively as compared to GaN-on-SiC devices. The main reason behind this reduction is the decrease in R_{1D} and R_s (more dominantly R_{1D}) with the higher thermal conductivities of HF and MW diamond. Although higher thermal resistance reduction of around 40%, similar to the findings of (Sun *et al.*, 2015), can be achieved for diamond substrates by only comparing the R_{1D} values, this effect will only reflect the improvement of the average temperature of the die surface. It will not reflect the channel and/or maximum temperature improvement of the device, which is especially important for certain device degradation mechanisms. Therefore, to get the full advantage of diamond substrates for lowering the channel temperatures, devices with longer gate widths should be operated at biasing conditions that eliminate localized Joule heating as in the case of fully open channel conditions. When localized Joule heating cannot be eliminated, it is more suitable to use MW diamond substrate instead of HF diamond to obtain a reasonable reduction in channel temperatures.

Epitaxial Properties

In the second study, effects of some epitaxial properties such as TBR and GaN thickness (t_{GaN}) on the total thermal resistance of devices are studied. Figure 2 shows the variation of R with respect to t_{GaN}=0.5 µm-2.0 µm when different TBR values are used for devices grown on different substrates.

In Fig. 2, the thermal performance of the current state-of-the-art GaN-on-SiC technology with t_{GaN} = 2 µm and TBR = 2 m^2K/W is marked. Since the motivation to move towards substrates with high thermal conductivity is to reduce the total thermal resistance below this value epitaxial properties resulting with higher thermal resistances (underperform region highlighted in Fig. 2) will be undesired. It can be seen that both GaN-on-HF with TBR > $3\cdot10^{-8}$ m^2K/W and GaN-on-MW with TBR > $5\cdot10^{-8}$ m^2K/W underperform for almost every GaN thickness. Thus, TBR between the GaN and diamond layers should be below these values to make expensive diamond substrates a viable solution for thermal problems in HEMT devices with localized Joule heating.

To further reduce the thermal resistances, thin GaN layers are recommended with diamond substrates in literature (Felbinger et al., 2007). The idea behind this is to decrease the R_{1D} and position the high thermal conductivity diamond substrates as close to heat source regions as possible to facilitate heat spreading. Although this is true for devices with no and very small TBR, as can be seen in Fig. 2, t_{GaN} < 1 µm causes significant increase in the total thermal resistance of devices with TBR > $2\cdot10^{-8}$ m^2K/W. When no TBR is present thermal resistances can be decreased up to 25% with MW diamond substrates and 12% with SiC by just changing the GaN substrate thickness from 2 µm to 1 µm. However, for devices where TBR is present for all these configurations heat cannot spread effectively from where it is generated due to thinning of GaN layer, referred as premature thermal spreading, R_s and thus R increase. The thickness can be reduced further for devices with more distributed heating as in the case of fully open channel operating conditions. However, even in this scenario spreading effects will be present and therefore, it is recommended to optimize the GaN thickness without taking TBR and R_s into account.

Finger Spacing

With increasing finger spacing, area required for heat spreading also increases. This phenomenon leads to a lower thermal resistance in the devices due to decreased R_s. However, no significant change in the total thermal resistance can be observed after a particular finger spacing value. Figure 3 shows the effect of finger spacing, $2x_c$ = 20 µm – 400 µm, on the total thermal resistance of two-finger devices.

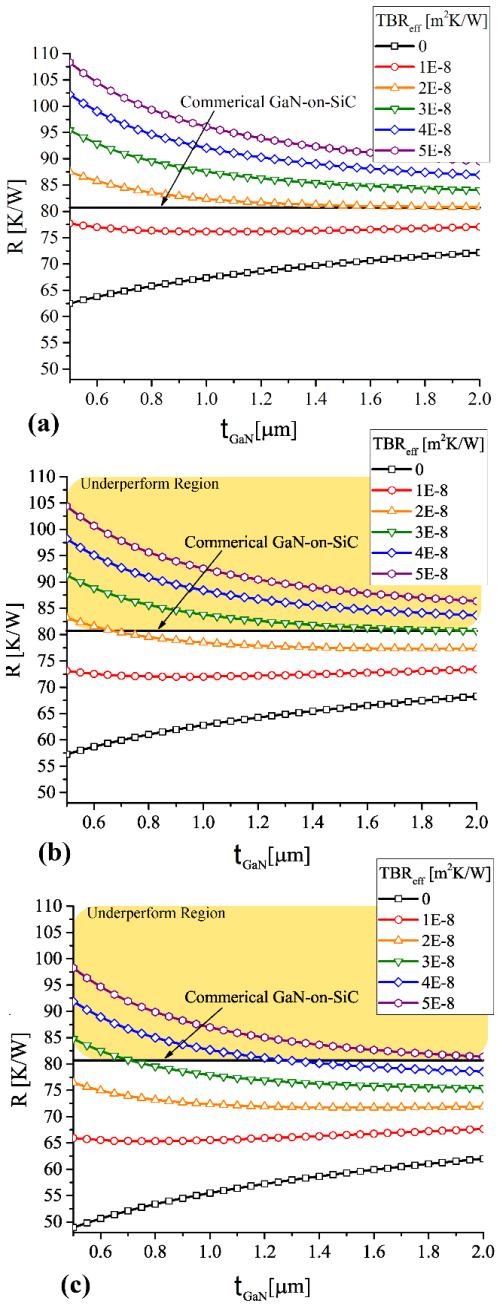

Figure 2. Total thermal resistance values of a) GaN-on-SiC, b) GaN-on-HF diamond, and c) GaN-on-MW diamond when the GaN thickness and effective thermal boundary resistances are varied

For $2x_c$ = 20 μm – 80 μm, total thermal resistance drops abruptly with increasing finger spacing. When the finger spacing is further increased from 80 μm, the total thermal resistance change is not as significant. For typical finger spacing values, $2x_c$ = 20 μm - 60 μm, thermal resistance values of GaN-on-SiC and GaN-on-HF are comparable. For example, the thermal resistance reduction obtained by using expensive HF diamond technology can simply be achieved by changing the finger spacing from 20 μm to 75 μm with GaN-on-SiC devices. However; GaN-on-MW proves its significant advantage over other technologies and should be especially preferred when denser devices with reduced finger spacing are desired.

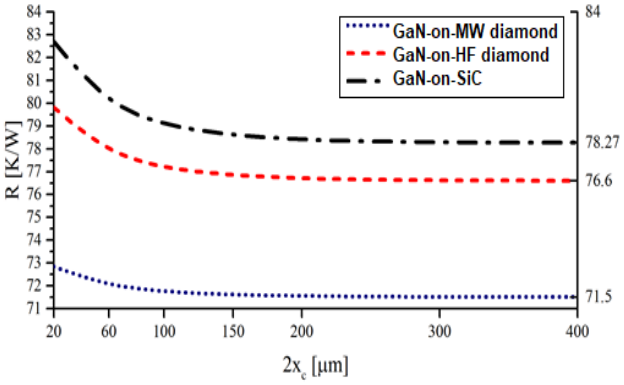

Figure 3. Thermal resistance effect of finger spacing on thermal resistance of a 2-finger device

Multifinger Spacing

Based on the device operation conditions the size and the amount of heat generated in each finger changes. Moreover, each finger thermally affects the innermost, hottest fingers of the devices (labeled as 1 in Fig. 1b). Thermal cross talk between fingers is strongly affected by the relative locations of fingers with respect to each other (finger spacing), Generally, the nearest neighbors have the highest effect that decreases with the increased finger spacing. The thermal effects from neighboring fingers can be accounted for by adding additional thermal resistance terms each associated with one neighboring finger. Thus by adding all the thermal resistances from the neighboring fingers on the innermost finger with its own thermal resistance, one can identify the total thermal resistance on the innermost fingers and obtain the temperature rise of the innermost finger. Fig. 4 illustrates the thermal resistance effect by neighboring fingers on the innermost fingers of a 20 finger device for three different finger spacing values: $2x_c$ = 20, 40, and 60 μm for a GaN-on-SiC device. As shown in Fig. 4, finger 2 has the greatest thermal resistance effect on the innermost fingers and with increasing finger spacing thermal effects of neighboring fingers decreases.

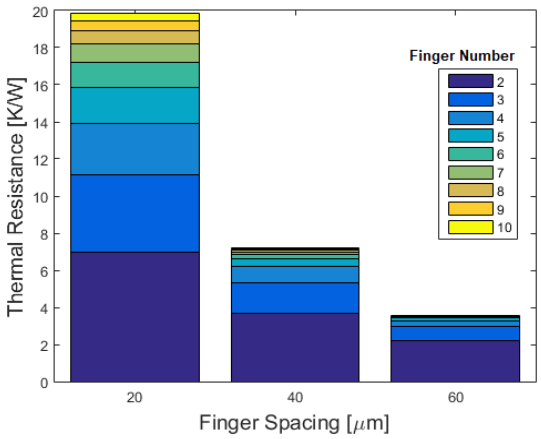

Figure 4. Additional thermal resistance created by the neighboring fingers (# 2 -10) on the innermost finger (# 1) for GaN-on-SiC device.

Table 3. Thermal resistance comparison between GaN-on-SiC and GaN-on-diamond devices for different finger numbers and finger spacing ($2x_c$) values.

	Finger Spacing					
	20 [µm]		40 [µm]		60 [µm]	
Finger	Thermal Resistance Reduction Compared to GaN-on-SiC					
Number	HF Diamond	MW Diamond	HF Diamond	MW Diamond	HF Diamond	MW Diamond
2	5.3%	13.5%	4.7%	12.2%	4.5%	11.6%
20	9.5%	24.3%	12.2%	16.9%	5.5%	14.0%

When compared with GaN-on-MW and HF diamond, effects of neighboring fingers on thermal resistance is much larger for GaN-on-SiC. Thus a reduction in total thermal resistance can be achieved by using HF or MW diamond substrates for multifinger devices. Table 3 shows this reduction that can be achieved by high thermal conductivity MW and HF diamond substrates for two and multifinger devices with varying finger spacing. For both two and multifinger devices, GaN-on-MW is the best choice independent from finger spacing. Thus, while there is not a significant difference between the thermal performance of 2-finger GaN-on-SiC and GaN-on-diamond devices, high thermal conductivity diamond substrates prove their advantage in multifinger configuration as shown in Table 3. Thermal advantages of GaN-on-MW devices are the highest for multifinger devices with small finger spacing. For a moderate power density of 5W/mm, for which temperature rise above 100K is expected (Sun et al., 2015), 25% decrease in thermal resistance achieved for a multifinger device with GaN-on-MW diamond technology will reduce the temperature rise above 25 K.

CONCLUSIONS

Thermal performance of diamond substrate technology is explored in this paper considering various parameters and compared with the mature GaN-on-SiC technology. The thermal performance of diamond substrates has proven its strength for high power applications in the past. In this study, the effects of localized Joule heating, integration related high TBR, and dense - multi finger configurations on thermal benefits of diamond substrates are investigated.

It is shown that localized Joule heating and short gate widths are responsible for high thermal spreading resistance GaN layer. Diamond substrate cannot effectively reduce this dominant thermal resistance in the device. Thus actual thermal advantages of using GaN-on-diamond substrates can be as low as 11% compared to 40% thermal advantage when MW diamond is used when thermal spreading effects are present.

When epitaxial properties are investigated, TBR, often neglected in thermal models, is found to be the most important one. Integration process of GaN and diamond can impose unexpected thermal resistance which can obstruct the benefit of the high thermal conductivity of diamond. While GaN thinning is not a good thermal solution when TBR>$2\cdot10^{-8}$ m^2K/W between the GaN and the substrate due to premature thermal spreading, 25% and 12% thermal resistance reduction can be achieved with MW and HF diamond substrates respectively compared to SiC by just thinning the GaN from 2 µm to 1 µm

When device compactness is not important, thermal performance of the device can be improved by increasing the finger spacing in both two and multifinger devices and SiC substrates thermal performance reaches HF diamond technology when the finger spacing is tripled for two finger devices. MW diamond exhibits its highest benefit in compact multifinger devices and SiC substrate technology is significantly lower for all finger spacings.

Considering the price, integration complexity, and fabrication quality GaN-on-diamond HEMTs should only be preferred where their thermal benefits far exceed current GaN-on-SiC technology. This study shows that both HF and MW diamond substrates with moderate TBR values can be used with multifinger devices with small finger spacing to improve thermal performances of devices. For other applications, while it cannot outperform GaN-on-MW diamond technology, GaN-on-SiC technology can still provide thermal benefits when certain improvements such as TBR reduction, finger spacing reduction, and/or heat source size increase by the modification of biasing conditions. In this study comparisons are based on thermal resistance values. To analyze the temperature benefits of using these technologies power densities should be known. Highest temperature reductions will be obtained for high power applications.

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