Research Article GU J Sci 35(2): 586-604 (2022) DOI: 10.35378/gujs.797571

Gazi University

Journal of Science

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Quantum dot Cellular Automata based Fault Tolerant Fingerprint Authentication Systems using Reversible Logic Gates

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Highlights

- Fault tolerance analysis of various XOR gates against single cell addition and missing defects.
- Highly fault tolerant XOR is used to design four Fingerprint Authentication Systems in QCA.
- Energy dissipation analysis of all four FAS designs is presented at different kink energy levels.
- The proposed FAS designs are highly area and cost efficient.

Article Info

Received: 20 Sep 2020
Accepted: 15 Apr 2021

Keywords

QCA
Fault tolerant design
Reversible logic
Nanoelectronics
Biometric system

Abstract

The limits and difficulties looked by CMOS innovation in the nano system has prompted the exploration of other potential advancements which can work with same functionalities anyway with lower power scattering and higher speed. One such technology is Quantum dot Cellular Automata (QCA). In this paper, QCA is explored to design the authentication system. This paper first presents the basic operating principle of a Fingerprint Authentication System (FAS) followed by fault tolerance analysis of four efficient XOR gate designs in the literature. The XOR gate is then used in the proposed four fault tolerant designs of reversible FAS in QCA, which are based on different reversible gates. Based on the evaluation of different performance parameters, it is seen that the proposed FAS designs are cost efficient and achieve improvement up to 59.46% in terms of number of cells, 67.16% improvement in cell area, 67.14% improvement in total area, 66.67% improvement in latency and 90.51% improvement in terms of circuit cost from the existing design Furthermore, the energy dissipation examination of the proposed designs is also additionally introduced. Subsequently, the proposed designs can be effectively used in biometric applications demanding ultra-low power consumption, higher operating speed and minimal area utilization.

1. INTRODUCTION

The fundamental nanometer-scale physical constraints of complementary metal oxide semiconductor (CMOS) technology are nearing. It causes a slew of short-channel effects and contributes to the deterioration of field-effect transistor characteristics [1-3]. Alternative nanotechnologies, such as the nanowire transistor, quantum-dot cellular automata (QCA), carbon nanotube field-effect transistor, and others, have already been offered solutions to these problems. QCA, first proposed by C. S. Lent in [1], has been identified as the most recent powerless technology capable of replacing nanoscale-based transistor-based semiconductor technology. It offers intriguing benefits such as increased device density and greater working switching frequencies (in the range of a few THz) at the nanoscale. Because the energy dissipation during state transition and propagation in QCA is negligible [4-6], there is significantly minimal energy dissipation when compared to CMOS technology. QCA is thoroughly investigated, and many logics are being proposed for diverse purposes, including reversible logic [6-9], arithmetic circuits [4, 5, 10-16], code converters [17-21], sequential circuits [17, 22-25], memories [26-29], and so on.

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1.1. QCA Preliminaries

- *QCA Cell:* It comprises four quantum wells, two of which have two electrons in diagonally opposing locations to achieve the lowest electronic repulsion, resulting in two binary states with information [30-32]. As seen in Figure 1, one of the electron locations describes '1' while the other describes '0.' Figure 2 shows the cells forming a QCA wire in tandem [3, 33].

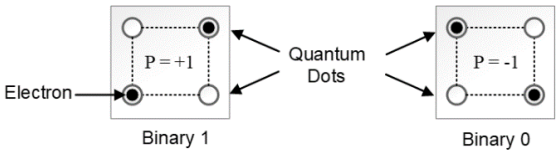


Figure 1. *QCA cell and its polarizations*

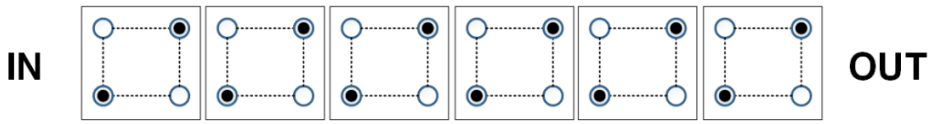
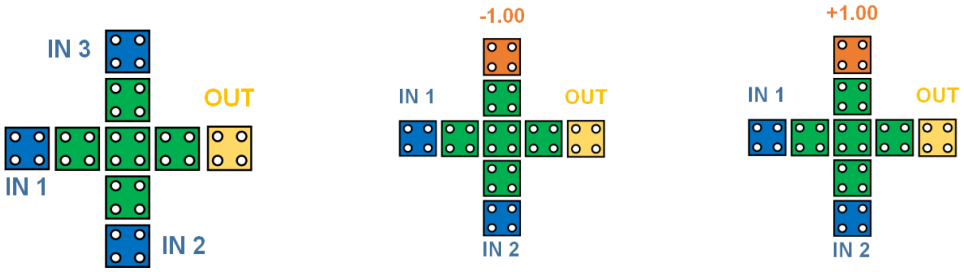


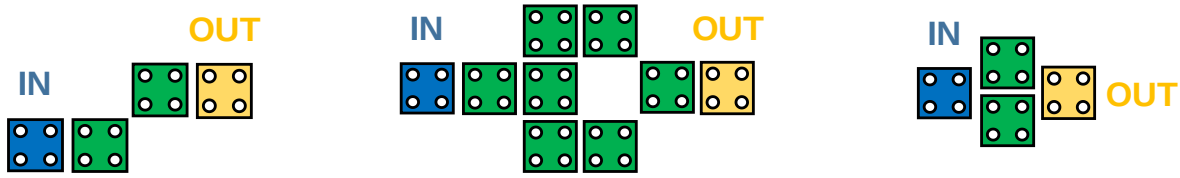
Figure 2. *QCA Binary wire*

- *QCA Logic Gates:* As shown in Figure 3(a), the basic logic gate in QCA is a three-input majority voter gate [3, 9]. The M(A,B,C) = AB + BC + CA mathematical operation is used to operate the gate. Figure 3(b) and Figure 3(c) illustrate the output of an OR gate when one of the inputs is set to ‘1' and the output of an AND gate when one of the inputs is set to ‘0'. (c). Inverter, besides being the basic building block of the Majority Voter, is used to invert the input logic. Figure 4 [3, 9] shows various inverter setups in QCA.



(a) *(b)* *(c)*

Figure 3. *Design of (a) 3-Input majority voter gate (b) Majority voter based AND gate and (c) Majority voter based OR gate in QCA [3, 9]*



(a) *(b)* *(c)*

Figure 4. *Various configurations of QCA Inverters (a) Half-cell displaced, (b) Large robust and (c) Rotated cell [3, 9]*

- *Clocking in QCA:* A four-phase clock is used in QCA circuits [34], as shown in Figure 5 [11]. The QCA cells are unpolarized at first, resulting in a low potential. During the switch phase, the polarization of a QCA cell is mainly controlled by the polarization of nearby cells, and the potential of the electrons begins to climb. Furthermore, once the electron reaches its maximum potential

vitality at the end of the switching period, no state transition happens. In the hold phase, the cell maintains its initial state and maintains a high level of potential vitality. The potential liveliness of the electrons begins to decrease during the release and relax phase, eventually returning to null polarization [3, 12, 33].

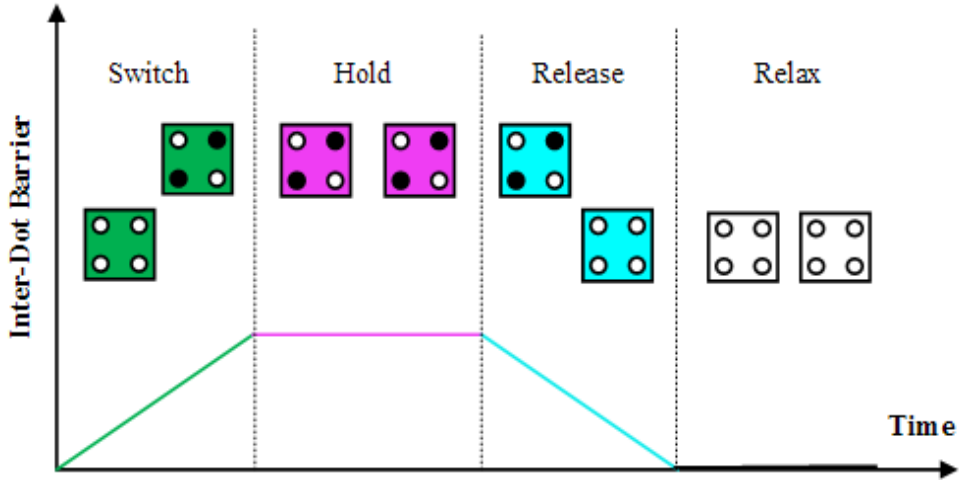


Figure 5. *Illustration of clocking in QCA*

The organization of the remaining paper is as follows: the brief description of the Fingerprint Authentication System (FAS) and its basic operation along with the review on existing design of FAS in QCA is given in Section 2. Various XOR gates and their fault tolerance analysis against single cell addition and missing defects is presented in section 3 along with their performance comparison followed by four proposed QCA designs of FAS in section 4. The energy dissipation analysis of all proposed FAS designs is presented in section 5. The comparison of various performance metrics is given in section 6 followed by concluding remarks in section 7.

2. FINGERPRINT AUTHENTICATION SYSTEM

The fingerprint authentication systems (FAS), based on digital logic and represented in in Figure 6, is utilized to coordinate with the information unique mark picture with existing pictures accessible in the data set [35]. On the off chance that match exists, the client is verified. All bits of the info picture (input) are checked consecutively with the pictures in the data set and when the match occurs, the comparing yield bit is set to rationale '1'. On the off chance that toward the finish of coordinating, every one of the pieces of yield are '1' then the match between these two images exists [35]. This mechanism can be perceived from Table 1.

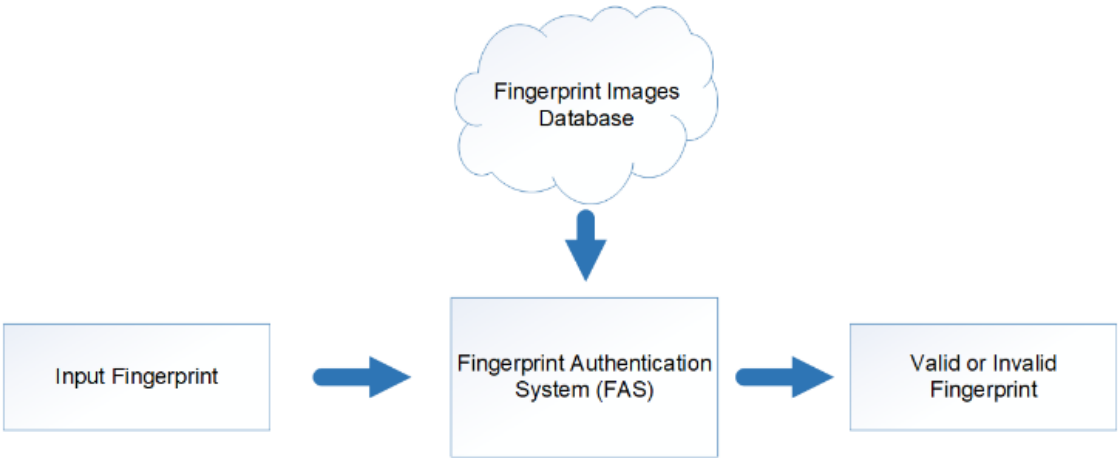


Figure 6. *FAS conceptual block diagram [35]*

Table 1. *Operating Conditions of FAS*

A	B	Output
" -1 " or " Logic 0 "	" -1 " or " Logic 0 "	" +1 " or " Logic 1 "
" -1 " or " Logic 0 "	" +1 " or " Logic 1 "	" -1 " or " Logic 0 "
" +1 " or " Logic 1 "	" -1 " or " Logic 0 "	" -1 " or " Logic 0 "
" +1 " or " Logic 1 "	" +1 " or " Logic 1 "	" +1 " or " Logic 1 "

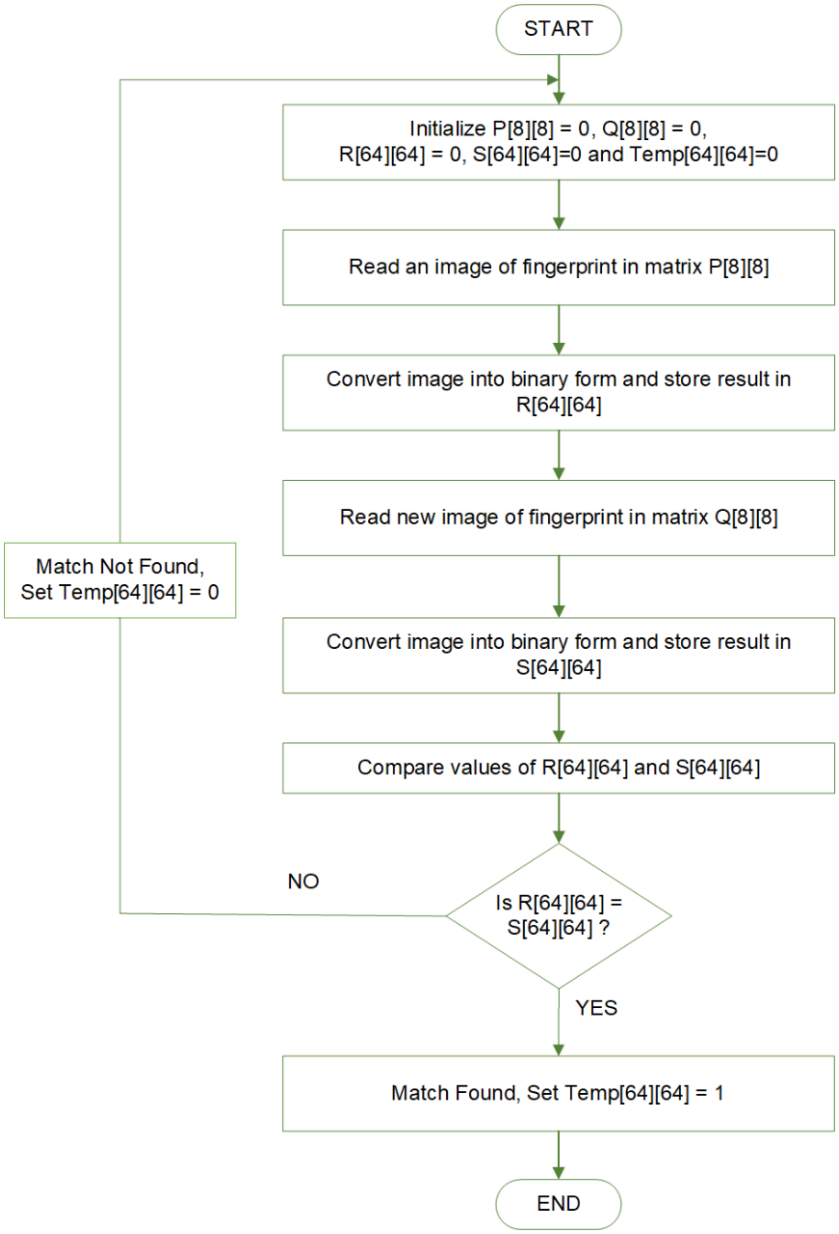


Figure 7. *Operating steps of FAS [35]*

It is seen from Table 1 that FAS operation is similar to that of an XNOR gate, hence the equations of FAS can be written as:

$$Y = \bar{A}\bar{B} + AB. \quad (1)$$

This operation can be visualized using the operating mechanism depicted in Figure 7. One such fingerprint authenticator (FPA) has been presented in [36], using a 2×2 Feynman Gate (shown in Figure 8).

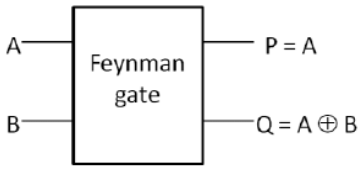


Figure 8. *Feynman Gate*

Debnath et al. in [36] presented an FPA by modifying the input A (written as X) to A' (written as X') of the Feynman gate as depicted in Figure 9.

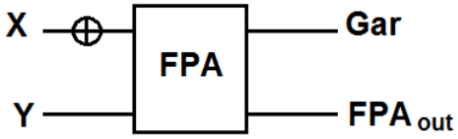


Figure 9. *FPA proposed in [36]*

The QCA implementation of this FPA, shown in Figure 10, by Debnath et al. in [36] was done using the equations based on the majority voter concept

$$GAR = \bar{X} \quad (2)$$

$$FPA_{out} = M(M(\bar{X}, \bar{Y}, 0), M(X, Y, 0), 1). \quad (3)$$

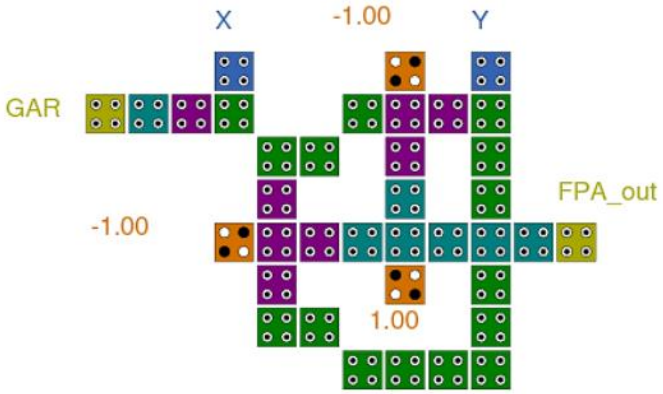


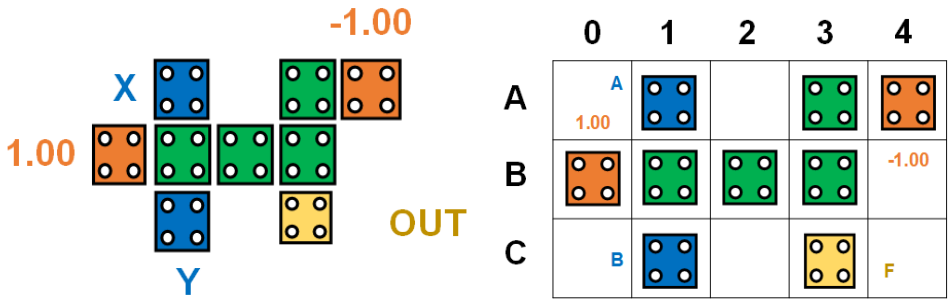
Figure 10. *QCA based FPA proposed in [36]*

3. XOR GATES IN QCA

The basic operating principle of a Fingerprint Authentication System (FAS) is identical to the operation of XNOR gate and XNOR gate can be directly designed from XOR gate. Hence, in this section, various efficient XOR gates proposed in the literature have been presented. In addition to this, since the application in concern requires accuracy, so a fault tolerant design is of prime importance. To achieve this, fault tolerance analysis of these XOR gates has also been presented in order to select the most efficient and fault tolerant design of XOR gate for the proposed FAS.

3.1. Design - 1

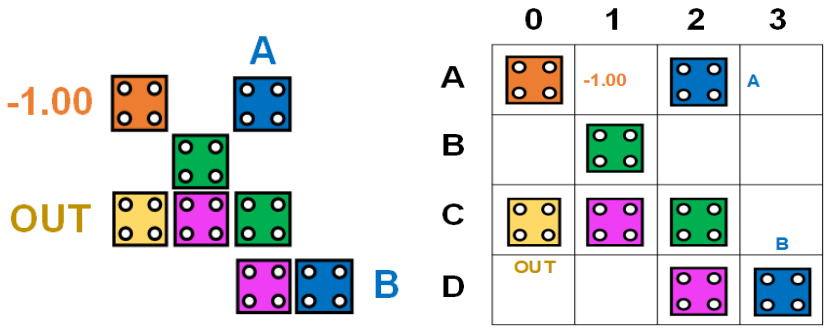
The first design considered in this paper is of Majeed et al. in [37] who proposed an XOR gate shown in Figure 11(a). It consists of 9 cells having 0.25 clock cycle latency and cell area 0.003 μm^2. The total area occupied by this design is 0.01 μm^2. The gird diagram used for analyzing the fault tolerance of this gate is shown in Figure 11(b).



(a) *(b)*

Figure 11. *(a) XOR gate proposed in [37] (b) Grid diagram of XOR gate*

3.2. Design - 2

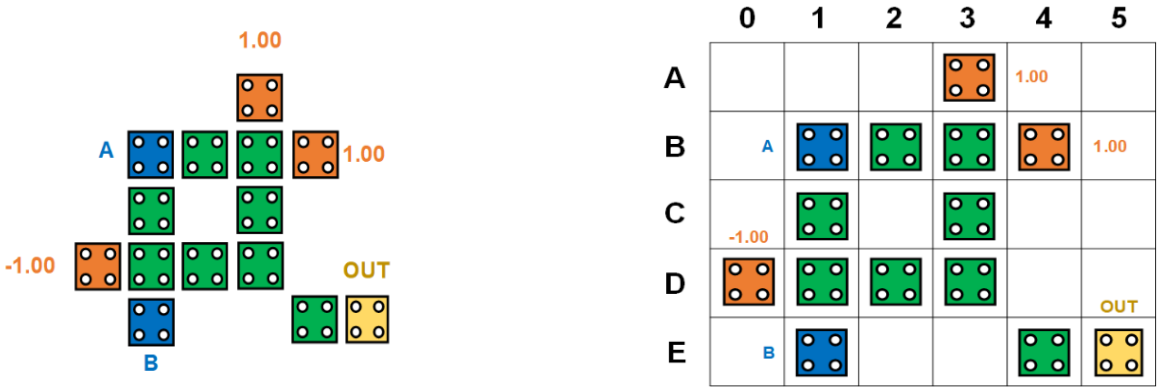


(a) *(b)*

Figure 12. *(a) XOR gate used in [12] and (b) Grid diagram of XOR gate*

Another XOR gate considered in this paper is shown in Figure 12(a). This design occupies cell area of 0.0026 μm^2 and is designed with 8 cells having 0.5 clock cycle latency. The total area occupied by this design is 0.0061 μm^2. The gird diagram used for analyzing the fault tolerance of this gate is shown in Figure 12(b). There are two cases available here viz. Case 1 and Case 2. In Case 1, the clocking of additional cell D1 is in clock zone 1 whereas in Case2, the clocking of D1 is in clock zone 2.

3.3. Design – 3

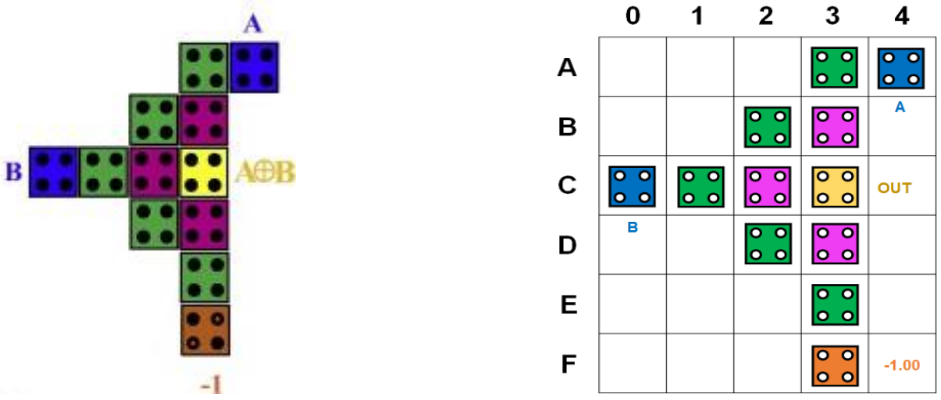


(a) *(b)*

Figure 13. *(a) XOR gate proposed in [38] and (b) Grid diagram of XOR gate*

The third XOR gate considered in this paper is shown in Figure 13(a). This design occupies cell area of 0.0045 μm^2 and is designed with 14 cells having 0.25 clock cycle latency. The total area occupied by this design is 0.0116 μm^2. The gird diagram used for analyzing the fault tolerance of this gate is shown in Figure 13(b).

3.4. Design - 4



(a) *(b)*

Figure 14. *(a) XOR gate proposed in [39] and (b) Grid diagram of XOR gate*

The fourth XOR gate considered in this paper is shown in Figure 14(a). This design occupies cell area of 0.0039 μm^2 and is designed with 12 cells having 0.5 clock cycle latency. The total area occupied by this design is 0.0116 μm^2. The gird diagram used for analyzing the fault tolerance of this gate is shown in Figure 14(b).

3.5. Performance Comparison of Fault Tolerance of XOR Gates

Table 2. *Fault tolerance performance comparison*

XOR Design No.		Fault Tolerance against Single Cell Addition Defect	Fault Tolerance against Single Missing Cell Defect	Overall Fault Tolerance
1		70.83%	43.75%	60%
2	*Case 1*	69.44%	50%	63.46%
	Case 2	63.89%		59.62%
3		84.375%	62.5%	77.08%
4		82.14%	53.125%	71.59%

The fault tolerance analysis of these designs against single cell addition and missing defects was performed using the mechanism presented in [40]. All these designs have been designed using QCADesginer tool [41]. Based on the fault tolerance comparison of various XOR designs presented in Table 2, it is observed that Design-3 has highest overall fault tolerance against single cell addition and omission defects and hence this design will be used for designing the Fingerprint Authentication System.

4. PROPOSED FINGERPRINT AUTHENTICATION SYSTEMS (FAS) IN QCA

In this section four different designs of Fingerprint Authentication System (FAS) are proposed using different reversible logic gates.

4.1. Design – 1 (Using Feynman Gate)

Feynman gate [42] is a 2 × 2 reversible gate having the following output equations:

$$P = A \quad (4)$$

$$Q = A \oplus B. \quad (5)$$

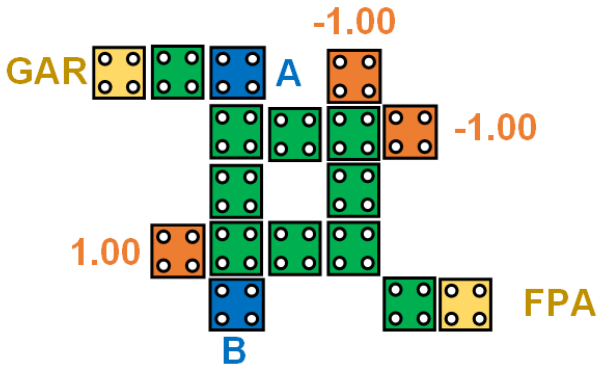


Figure 15. *Proposed Design-1 of FAS using Feynman Gate*

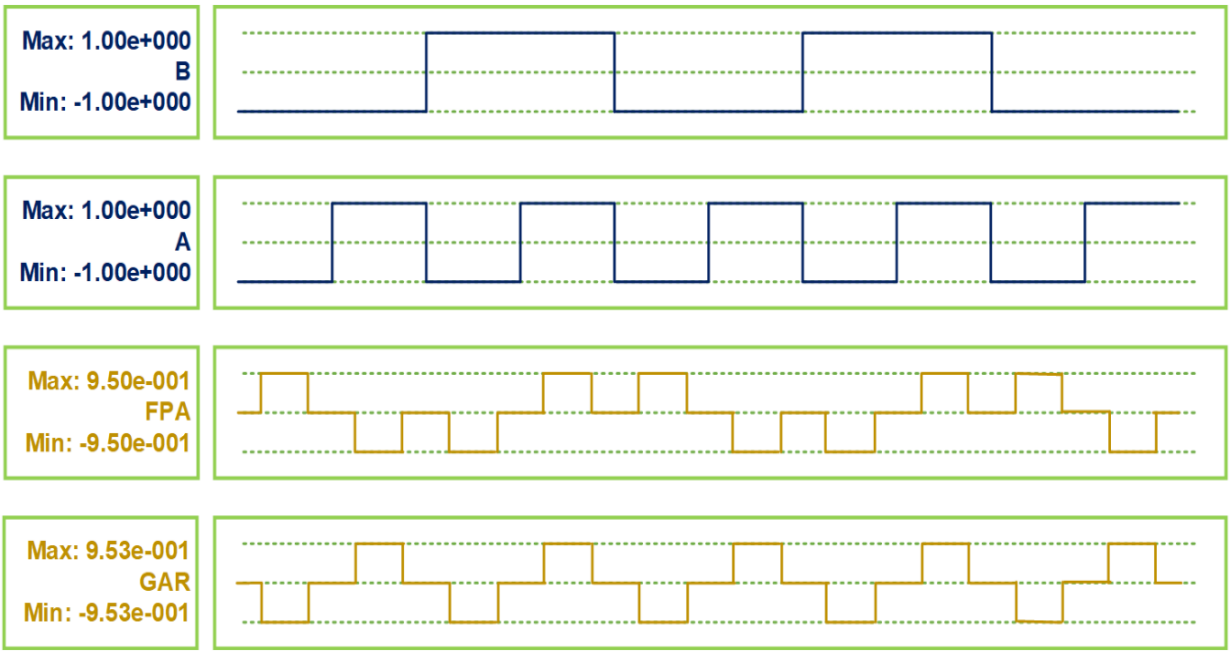


Figure 16. *Input and output waveforms of proposed QCA design-1 of FPA*

The above equations have been implemented using fault tolerant XOR gate (Design-3) and an inverter has been applied at the output Q to obtain the desired FPA output. The proposed implementation in QCA is shown in Figure 15. This design occupies cell area of 0.00486 μm^2 and is designed with 15 cells having 0.25 clock cycle latency. The total area occupied by this design is 0.011564 μm^2. The design can be validated from the simulation input and output waveforms shown in Figure 16 obtained from QCADesigner tool [41].

4.2. Design – 2 (Using BJN Gate)

BJN gate [43] is a 3x3 reversible gate having the following output equations:

$$P = A \quad (6)$$

$$Q = B \quad (7)$$

$$R = (A + B) \oplus C. \quad (8)$$

If either input B or input A is set to '0' and an inverter is applied at the output R, we can obtain the desired FPA output. The proposed implementation in QCA using fault tolerant XOR gate, when input B is set to '0', is shown in Figure 17. This design occupies cell area of 0.007776 μm^2 and is designed with 24 cells having 0.5 clock cycle latency. The total area occupied by this design is 0.031284 μm^2. The design can be

validated from the simulation input and output waveforms shown in Figure 18 obtained from QCADesigner tool [41].

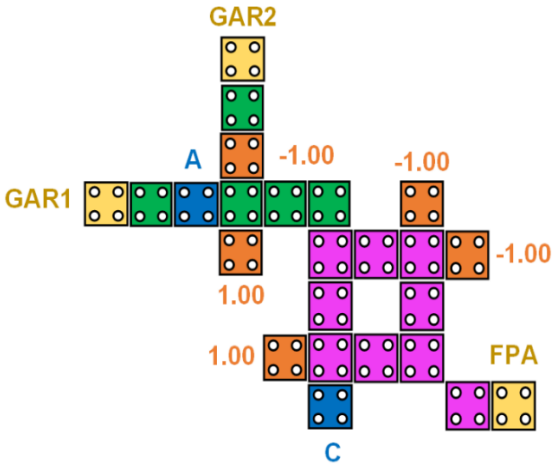


Figure 17. *Proposed Design-2 of FAS using BJN Gate*

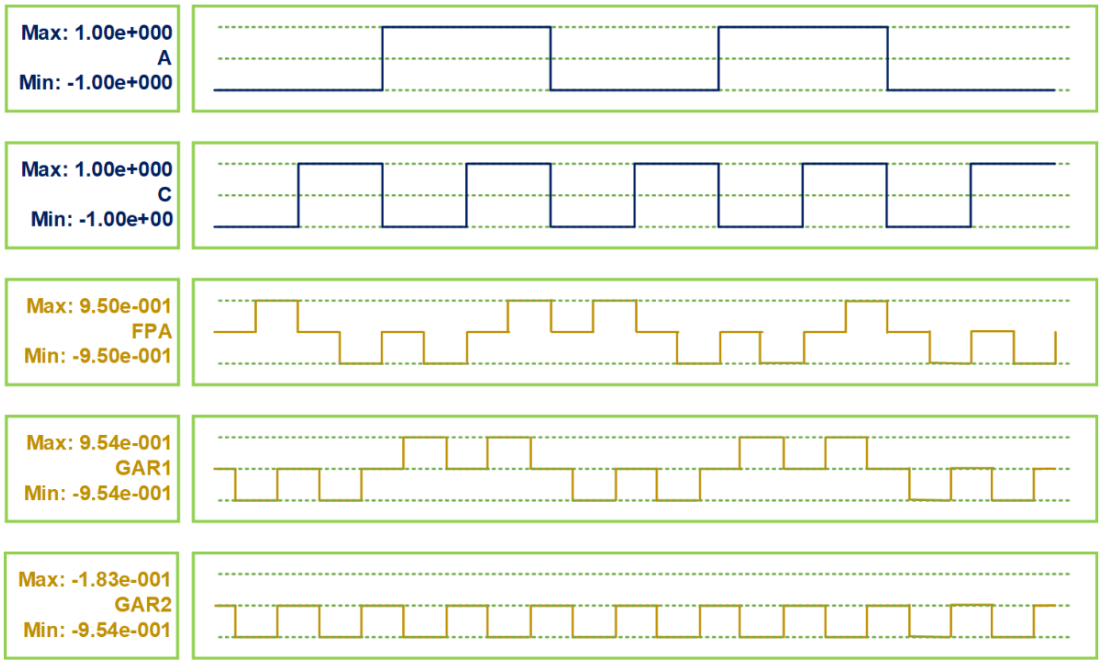


Figure 18. *Input and output waveforms of proposed QCA design-2 of FAS*

4.3. Design – 3 (Using Toffoli Gate)

Toffoli gate [44] is a 3x3 reversible gate having the following output equations:

$$P = A \tag{9}$$
$$Q = B \tag{10}$$
$$R = AB \oplus C. \tag{11}$$

If either input A or input B is set to '1' and an inverter is applied at the output R, we can obtain the desired FPA output. The proposed implementation in QCA using fault tolerant XOR gate, when input B is set to '1', is shown in Figure 19. This design occupies cell area of 0.008748 μm^2 and is designed with 27 cells having 0.5 clock cycle latency. The total area occupied by this design is 0.024564 μm^2. The design can be

validated from the simulation input and output waveforms shown in Figure 20 obtained from QCADesigner tool [41].

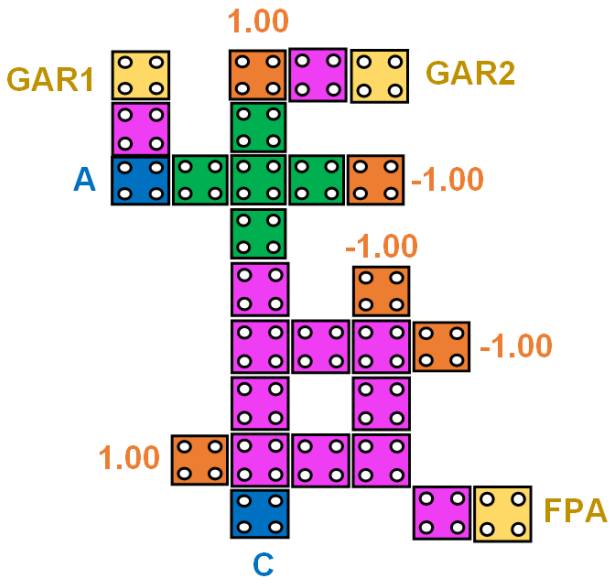


Figure 19. *Proposed Design-3 of FAS using Toffoli Gate*

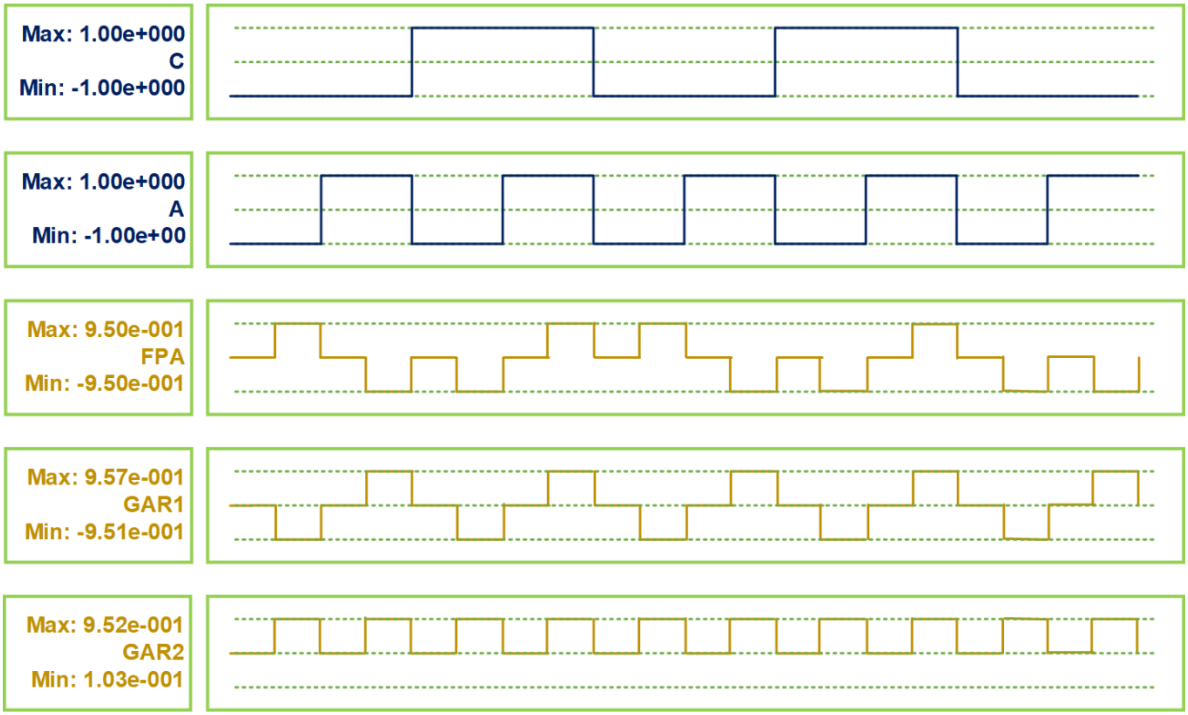


Figure 20. *Input and output waveforms of proposed QCA design-3 of FAS*

4.4. Design – 4 (Using Double Feynman Gate)

Double Feynman gate [45] is a 3x3 reversible gate having the following output equations:

$$P = A \tag{12}$$
$$Q = A \oplus B \tag{13}$$
$$R = A \oplus C. \tag{14}$$

As is evident from the equations, if an inverter is applied at outputs Q and R, we can get two XNOR gates from a single gate. This will lead to an additional functionality of FAS as the proposed system will be able to detect two different fingerprints simultaneously. The proposed implementation in QCA, using fault tolerant XOR gate, is shown in Figure 21. This design occupies cell area of 0.010368 μm^2 and is designed with 32 cells having 0.25 clock cycle latency. The total area occupied by this design is 0.030084 μm^2. The design can be validated from the simulation input and output waveforms shown in Figure 22 obtained from QCADesigner tool [41].

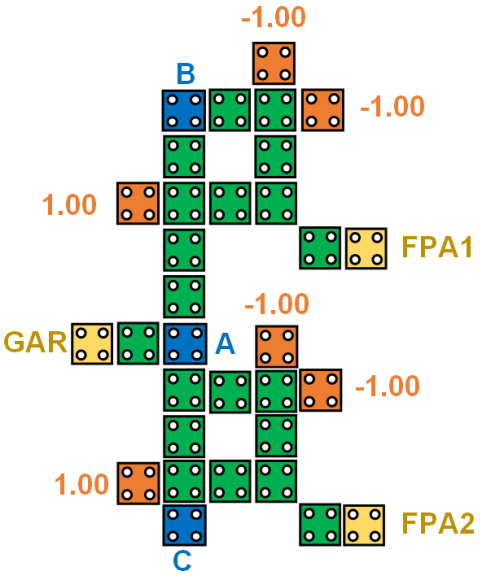


Figure 21. *Proposed Design-4 of FAS using Double Feynman Gate*

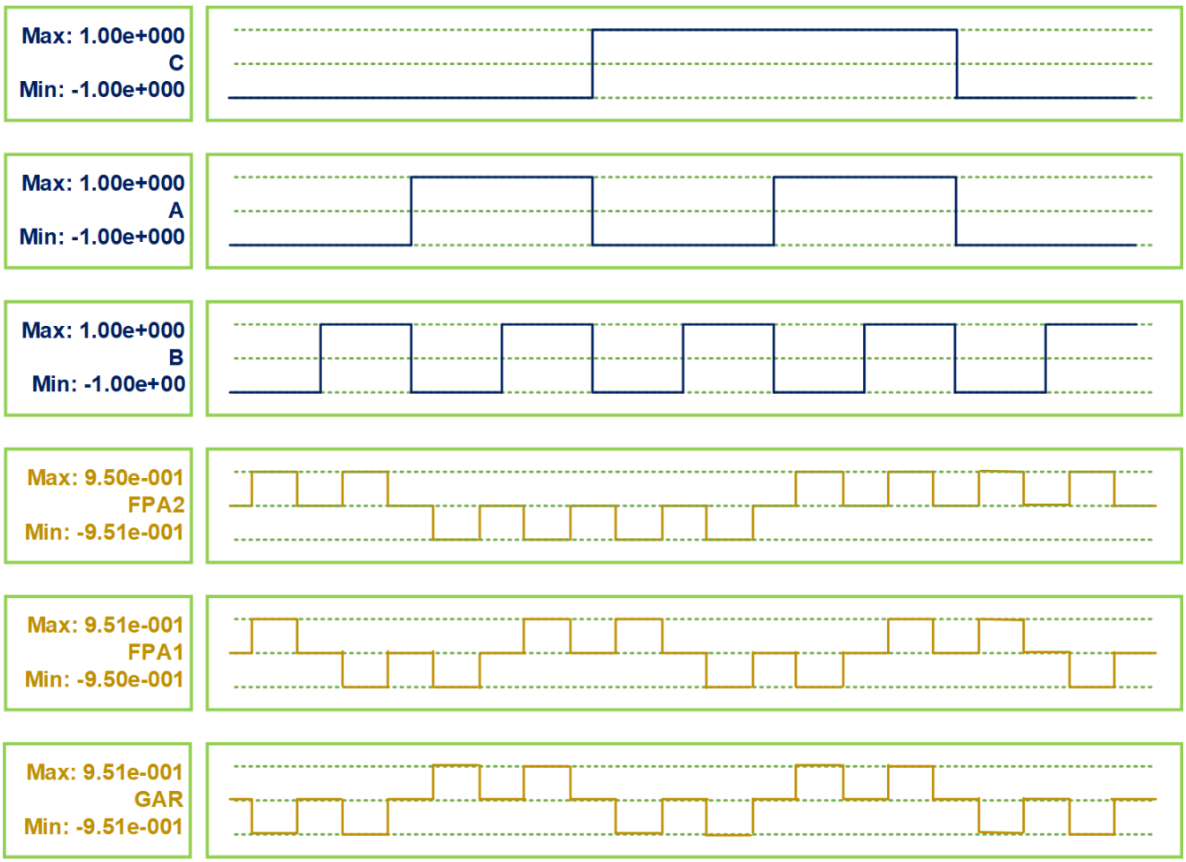


Figure 22. *Input and output waveforms of proposed QCA design-4 of FAS*

5. ENERGY DISSIPATION ANALYSIS

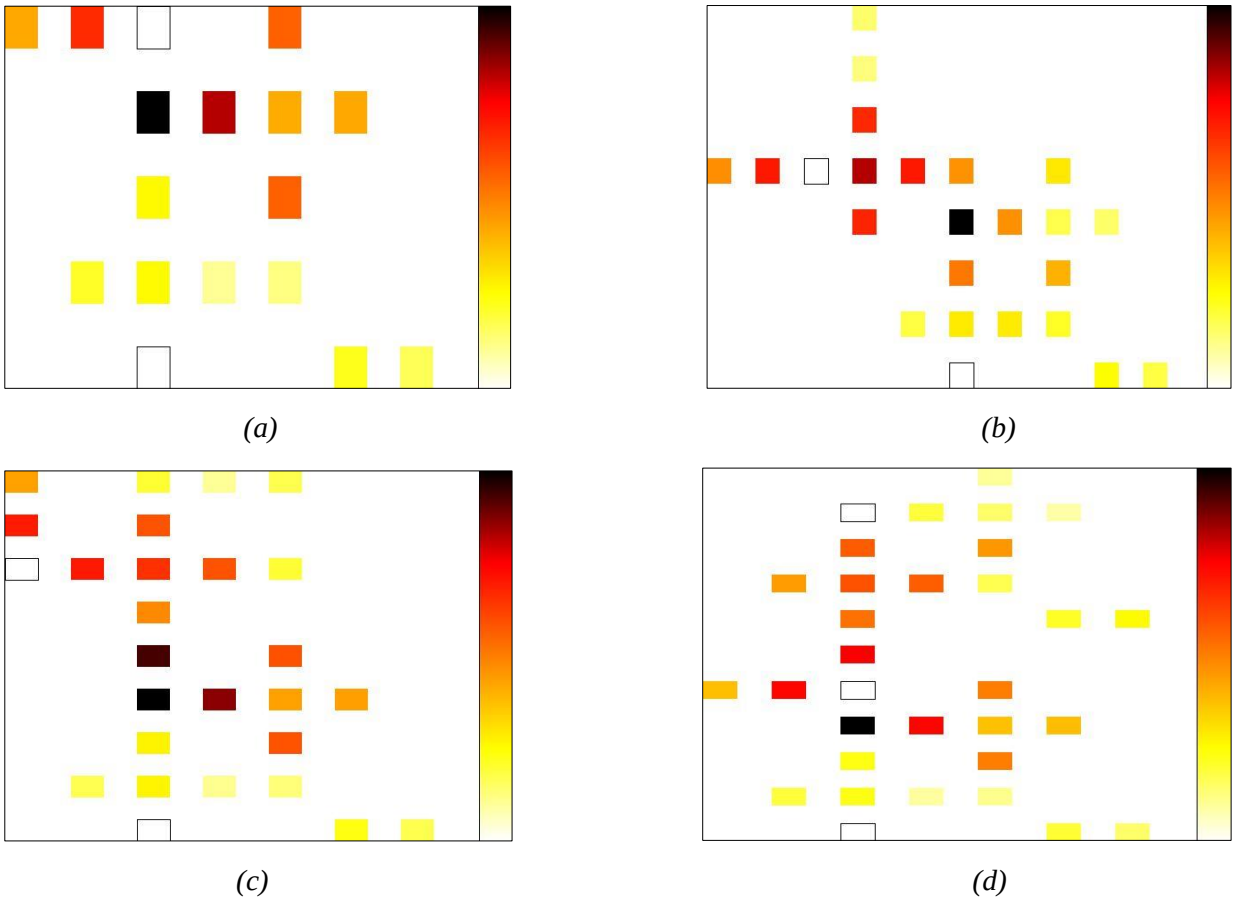
The energy dissipation evaluation of the FAS designs proposed in this paper has been performed using QCAPro tool [46]. This tool calculates the Hamiltonian, given in Equation (15), for energy calculations by using Hatree-Fork [47, 48] method. It is a probabilistic approximation method for energy calculation.

$$H = \begin{bmatrix} \frac{-E_k}{2}\sum_i C_i f_{i,j} & -\gamma \\ -\gamma & \frac{E_k}{2}\sum_i C_i f_{i,j} \end{bmatrix} = \begin{bmatrix} \frac{-E_k}{2}\left(C_{j-1} + C_{j+1}\right) & -\gamma \\ -\gamma & \frac{E_k}{2}\left(C_{j-1} + C_{j+1}\right) \end{bmatrix}. \quad (15)$$

The per clock cycle (T_{cc}) energy dissipated per clock cycle is then calculated using the Hamiltonian, evaluated in Equation (15) along with Coherence vector as given in Equation (16)

$$E_{diss} = \frac{\hbar}{2}\int_{-L}^{L} \vec{\Gamma}.\ \frac{d\vec{\lambda}}{dt}dt\ = \frac{\hbar}{2}\left(\left[\vec{\Gamma}.\vec{\lambda}\right]\frac{L}{-L} - \int_{-L}^{L}\vec{\lambda}.\ \frac{d\vec{\Gamma}}{dt}dt\right). \quad (16)$$

The QCAPro tool uses these equations to provide different energies dissipated by the QCA circuits at three different tunneling energy levels which are 0.5Ek, 1.0Ek and 1.5Ek. This tool also provides with graphical representation of energy dissipated by each cell in the design in the form of energy dissipation maps. Figure 23 shows the energy dissipation map for all designs at 0.5 Ek level. The default temperature and other settings have been selected in the QCAPro tool to obtain these maps. The dark/black cells in these maps depicts the cells dissipating maximum energy in the circuit whereas the white cells are input cells which dissipate no energy. It is observed from the energy maps that only few cells in proposed designs are dark and hence the proposed FAS designs can be considered as energy efficient in nature.



(a) *(b)* *(c)* *(d)*

Figure 23. *Energy dissipation map at 0.5 Ek energy level of proposed FAS (a) design - 1, (b) design – 2, (c) design-3 and (d) design - 4 at 2K temp*

6. DISCUSSION

The efficiency of the proposed designs is evaluated by drawing a number of comparison tables. The comparison table showing the efficiency of the proposed design of FAS as compared to the existing design is given in Table 3.

Table 3. *Comparison between previous and the proposed designs of FAS*

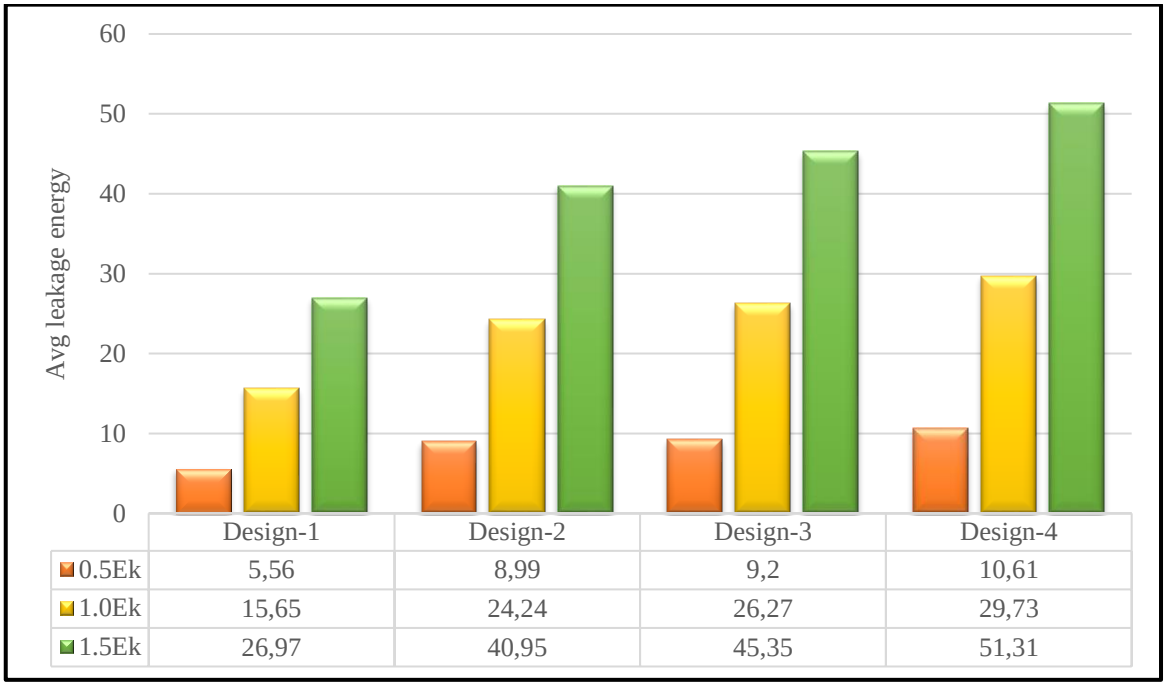
Structure	Cell count	Cell Area (μm^2)	Total Area (μm^2)	Latency	QCA Cost
[36]	37	0.0148	0.0352	0.75	0.0198
Proposed Design-1	15	0.00486	0.011564	0.25	0.00723
Proposed Design-2	24	0.007776	0.031284	0.5	0.00782
Proposed Design-3	27	0.008748	0.024564	0.5	0.00614
Proposed Design-4	32	0.010368	0.030084	0.25	0.00188

Here QCA cost is the product of total area and square of latency. In addition to this, parameter by parameter wise percentage improvement compared to existing design [36] is presented in Table 4. It is seen that the proposed FAS designs show an improvement ranging from 13.51% to 59.46% in terms of number of cells, 29.94% to 67.16% improvement in cell area, 11.12% to 67.14% improvement in total area, 33.33% to 66.67% improvement in latency and 60.51% to 90.51% improvement in terms of QCA circuit cost. It is also worth stating here that the proposed 3 × 3 Double Feynman Gate based Design-4 of FAS has the ability to match two different fingerprints simultaneously and despite this additional feature, it achieves an improvement of 90.51% in terms of QCA circuit cost compared to the design proposed by [36] which uses 2 × 2 Feynman gate for its FAS design.

Table 4. *Percentage improvement in proposed designs compared to design [36]*

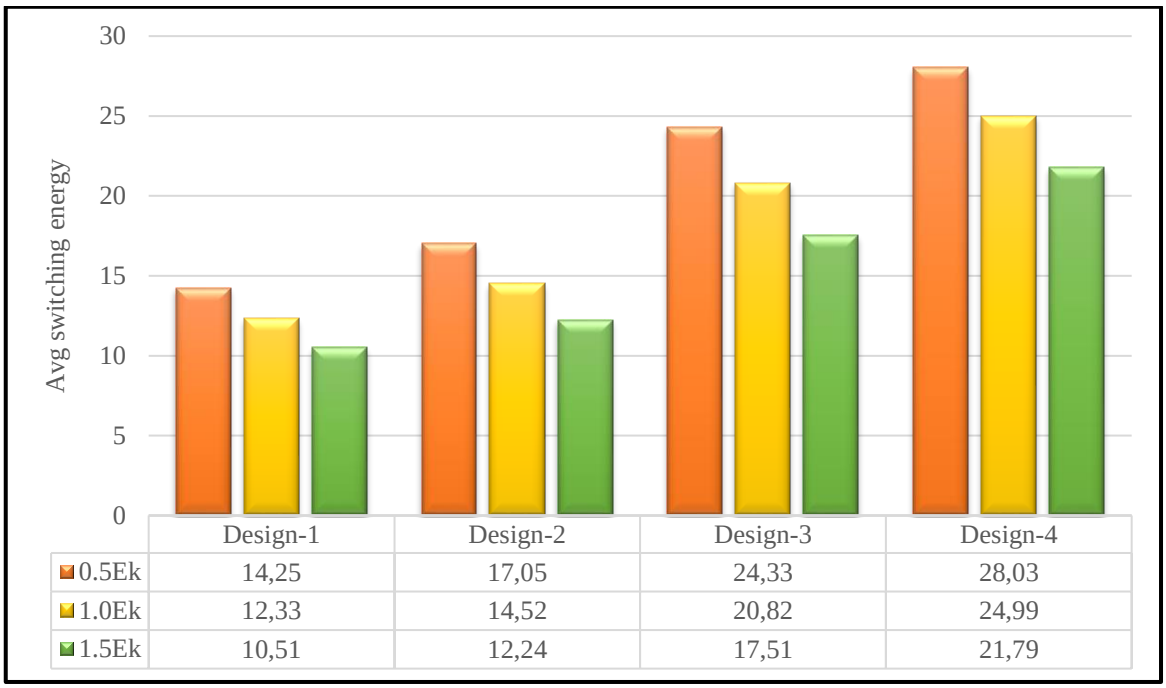
Parameter	Design-1	Design-2	Design-3	Design-4
Cell count	59.46%	35.14%	27.03%	13.51%
Cell Area (μm^2)	67.16%	47.46%	40.89%	29.94%
Total Area (μm^2)	67.14%	11.12%	30.22%	14.53%
Latency	66.67%	33.33%	33.33%	66.67%
QCA cost	63.48%	60.51%	68.99%	90.51%

A graphical correlation showing the energy effectiveness of the proposed FAS designs are shown in Figure 24. It is evident from the graphical comparison of energy dissipated by proposed designs that Design-4 dissipates the highest energy which is evident due to higher number of cells utilized in its design whereas, Design-1 dissipates the least energy. Depending upon the requirement of the user, any of the four proposed designs of Fingerprint Authentication Systems can used for secure nano-computing applications.



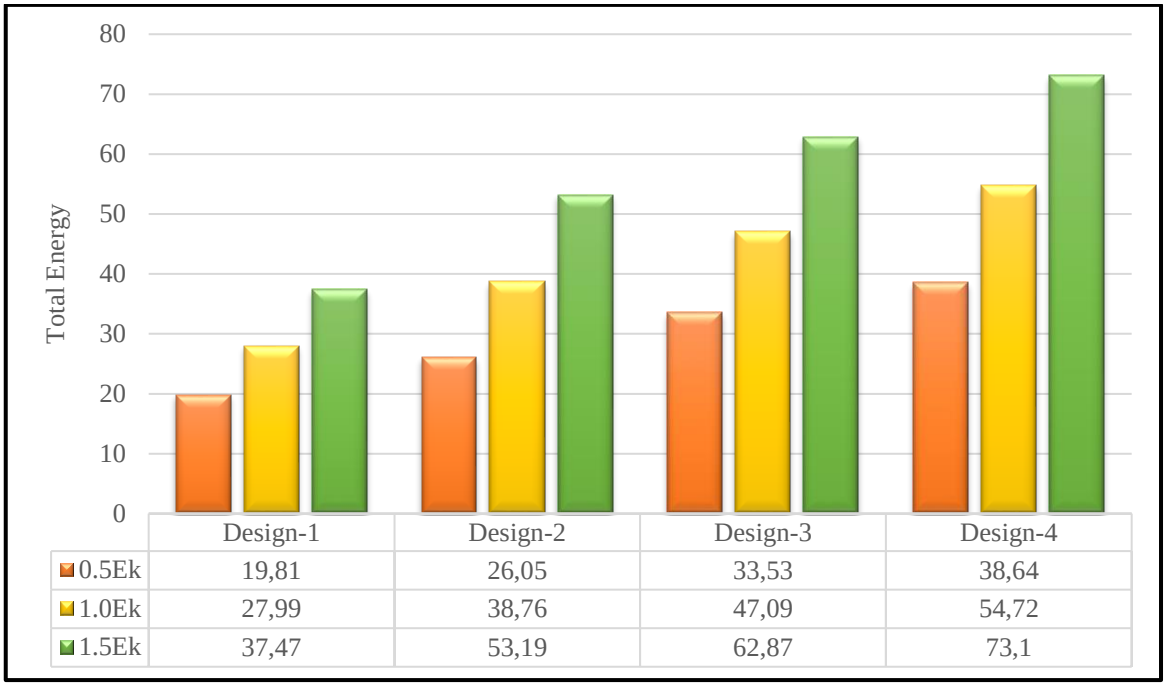
	Design-1	Design-2	Design-3	Design-4
0.5Ek	5,56	8,99	9,2	10,61
1.0Ek	15,65	24,24	26,27	29,73
1.5Ek	26,97	40,95	45,35	51,31

(a)



	Design-1	Design-2	Design-3	Design-4
0.5Ek	14,25	17,05	24,33	28,03
1.0Ek	12,33	14,52	20,82	24,99
1.5Ek	10,51	12,24	17,51	21,79

(b)



	Design-1	Design-2	Design-3	Design-4
0.5Ek	19,81	26,05	33,53	38,64
1.0Ek	27,99	38,76	47,09	54,72
1.5Ek	37,47	53,19	62,87	73,1

(c)

Figure 24. *Comparison of (a) avg. leakage (b) avg. switching and (c) total energy (meV) dissipation of proposed FAS designs*

7. CONCLUSION

This paper first presents the basic operating principle of a Fingerprint Authentication System (FAS). Its operation follows that of an XNOR gate which can be directly designed from an XOR gate. Hence, given the application and accuracy of the results required, a first of its kind fault tolerance analysis of five efficient XOR gate designs in the literature is presented. Based on the performance evaluation one of the design is selected and four fault tolerant designs of FAS are proposed which are based on different reversible gates. The simulation results are acquired utilizing the QCADesigner tool and the energy dissipation of proposed FAS designs is determined using the QCAPro tool. It is seen that the proposed designs are cost efficient and achieve improvements up to 59.46% in terms of number of cells, 67.16% improvement in cell area, 67.14% improvement in total area, 66.67% improvement in latency and 90.51% improvement in terms of circuit cost compared to the design. Additionally, based on the energy dissipation analysis for different kink energy levels, it is seen that the presented FAS designs dissipate very low energy which make them suitable for application in different ultra-low power nano-computing applications.

CONFLICTS OF INTEREST

No conflict of interest was declared by the authors.

FUNDING INFORMATION

The authors would like to thank National Project Implementation Unit (NPIU), a unit of Ministry of Education, Government of India and The World Bank, for providing financial assistance to carry out this research under TEQIP-III Collaborative Research Scheme (CRS) with sanction number: 1-5736612144.

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