Design and Analysis of Transformerless Grid-Tie Buck-Boost Photovoltaic Inverter with Immittance Conversion Topology

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Abstract- This article introduces the design and analysis of a single-phase single-stage transformer-less grid-tie buck-boost photovoltaic inverter topology for domestic purposes. Functionally, this new inverter can adjust to a wide range of photovoltaic dc variations, higher or lower dc voltages compared to utility line voltage, and in the meantime track the maximum amount of solar energy all in one single power stage. For switching of inverter power circuit, a combination of sinusoidal pulse width modulation (SPWM) and square wave signal under grid synchronization condition are used. Moreover, to control SPWM duty cycle and to regulate the inverter's instantaneous ac output voltage, a closed-loop SPWM control technique is used to stabilize the output as fast as possible. Besides, we also employed immittance conversion circuit topology in the inverter output terminal instead of conventional LC filter. The design and analysis of working principles of the inverter control circuit and grid synchronization methods are described in details. This paper mainly focuses on the analysis of working principles, computer simulation of the operation and design consideration of the inverter for grid-connected applications. The effectiveness of the proposed system is clarified through the following mathematical modeling and simulations.

Keywords—Single-stage, SPWM, Square wave, Buck-boost converter, Power electronics, THD; Grid-tie Inverter (GTI)

1. Introduction

The worldwide development in sustainable energy sources replaces the traditional energy sources. However, renewable energy such as solar energy play a vital role due to is pollution free nature. Solar energy is not directly interfaced with the utility grid because of its economic reasons [1]. Hence power electronics interfaces such as an inverter offer the necessary means to convert the constant-voltage output of the photovoltaic panels into a useable sinusoidal ac power in grid-connected photovoltaic system [2], [3]. Traditional, the grid-connected inverters are classified as single-stage & two-stage configuration.

According to [4]-[6], multiple stage or two-stage configuration of four-switch buck-boost GTI is usually used in photovoltaic application. Such inverter systems have dc-dc or dc-ac-dc converters enhanced to achieve a higher dc voltage before inversion. Though a two-stage buck-boost inverter can reach a reasonably high power capacity, the extra power stage necessitates further power components, which condenses circuit complexity as well as shoots up the cost.

Numerous alternatives architectures for grid connected PV system configurations exist, such as centralized module, AC module and modular configuration where the last topology perfectly fits with an intelligent PV module concept [7]. A few possible configurations of grid connected PV systems are shown in Fig.1. A centralized inverter configuration is shown in Fig. 1(a) that interfaced vast amount of PV modules. Nevertheless, there are some severe limitations in the design of centralized inverters, such as power loss for using a central MPPT, PV modules with

mismatch losses due to the high voltage dc cabling connecting the PV modules with the inverter, string diode loss etc. Fig. 1(b) shows the AC module configuration, which is an abridged version of the centralized inverter topology. Now a single string of PV module is coupled with an inverter. Each string can be applied with a distinct MPPT, as there is no loss attributed to string diodes. In contrast to the centralized inverter the overall efficiency is improved. Fig. 1(c) shows the modular arrangement [8].

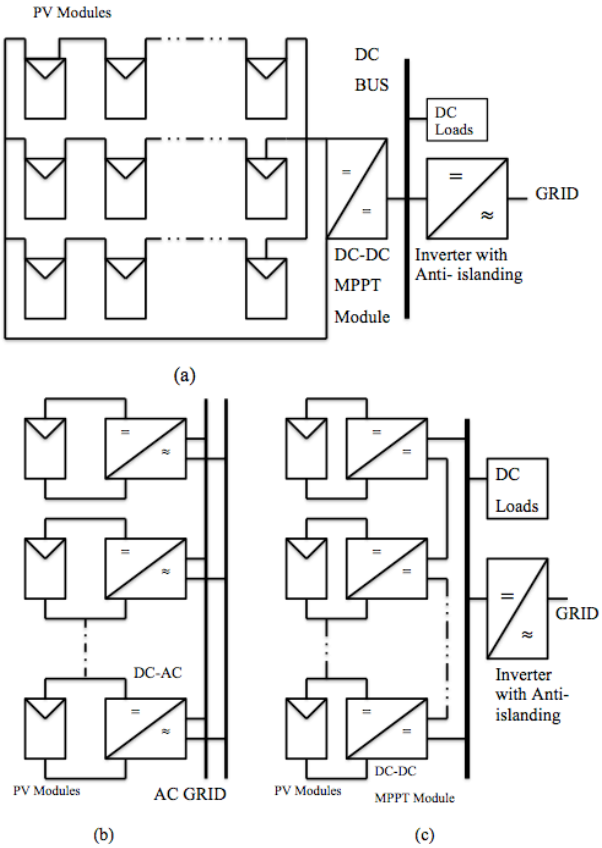


Fig. 1. Block diagram of proposed single-stage buck-boost PV inverter

A common inverter is merged with multiple Strings connected to separate DC-DC converter. The advantage of this modular configuration over centralized system is that each string can be controlled individually and confirm less cabling loss thereby heightening the overall system efficiency.

Normally a single-stage inverter is an inverter with only one stage of conversion for both stepping-up and stepping-down the dc voltage from PV sources and modulating the sinusoidal output voltage or current [9]-[12]. The inverter involves two sets of Buck-Boost type chopper circuit, and the number of switching devices which are used in the system is less than that in the conventional system. A transformer and an inductor that links to a utility grid line are not essential for the system. In the system, there is no earth-leakage current at all in the- theoretical base. And also the main circuit of this system is rather simple and it is expected the higher efficiency will be realized. The output power capacity of proposed inverter is under 700W.

The inverter switching control circuit and grid synchronization schemes are exemplified in detail in this paper [13], [14]. The inverter's parameters are designed mathematically, and the designed inverter is simulated via PSIM software to verify the inverter's output performances. Therefore, a closed-loop SPWM control structure is engaged in the system to adjust the instantaneous ac output current of the inverter. Fig. 2 displays the block diagram of the proposed PV power system. The flexibility of PV generation system is thus much improved. Furthermore, the AC module concept effectively decreases the manufacturing costs as a result of mass production efficiency. In this paper, first we show the buck-boost inverter power circuit, its equivalent circuit and basic differential equations. Next, from these results the basic characteristics such as the ripple current of the solar array, input impedance, output voltage and output power of the inverter are introduced. Finally, the power flow characteristics are elucidated when the proposed inverter is interconnected with the utility lines.

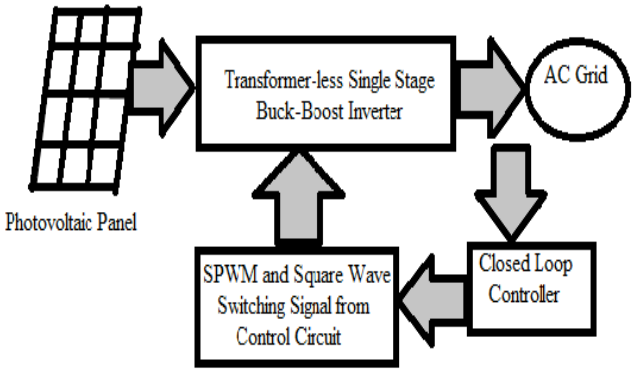


Fig. 2. Block diagram of proposed transformer-less GTI

As associated to the established single stage buck-boost inverters, buck inverters and other two-stage buck-boost inverters [9] with line-frequency transformers, both the component consider, bulk and cost of the proposed buck-boost GTI is diminished, thus exhibiting a more reliable and cost-effective design with overall high efficiency for domestic photovoltaic systems.

2. Requirements of Grid-Synchronization

The GTI design varies a bit from conventional stand-alone inverter. The output voltage from GTI is necessary to meet certain conditions for the inverter to be connected to the grid [1].

1) Voltage magnitude and phase of inverter must be same as grid.
2) The GTI output frequency must match with the grid frequency (50 Hz in Bangladesh).

To fulfill the above conditions, the grid voltage is sampled and then kept as a reference for the design of

switching signal. This require for the GTI has to force power produced from the PV panels into the grid. The real and reactive power flow of the GTI into grid are shown by [2],

$$\text{Real Power, } P = \frac{|V_{inv}||V_{grid}|}{z_t}\sin\varphi. \quad (1)$$

$$\text{Reactive Power, } Q = \frac{|V^2_{inv}|}{z_t} - \frac{|V_{inv}||V_{grid}|}{z_t}\cos\varphi. \quad (2)$$

Where, z_t = Linking line impedance
V_{inv} = Output voltage of inverter
V_{grid} = grid power voltage
ϕ = angle different between V_{inv} and V_{grid}

From equation (1), it is apparent that to send back maximum real power to the grid the phase angle ϕ must be 90^0. Practically for stability reasons the phase angle should be kept less than 90^0. From equation (1), the value of sinφ both have negative and positive value. In positive value, inverter output voltage leading the grid voltage. Then real power will flow from GTI into the grid line. However, the real power will flow from opposite direction if the value is negative.

3. Design of Proposed Buck-Boost GTI

3.1 Power Circuit Design and Operation of GTI

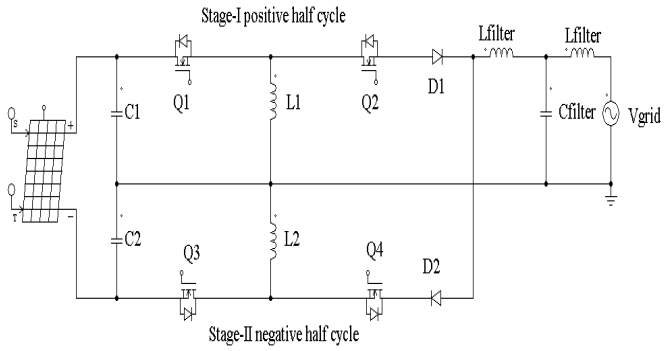


Fig. 3. Power circuit of proposed buck-boost GTI

Fig. 3 shows the power circuit of a transformer-less grid-tie buck-boost photovoltaic inverter with immittance converter topology. The power stage is constructed by PV array, with two series capacitors parallel with the PV array, four power MOSFETs switches Q_1, Q_2, Q_3, Q_4 with two diodes D_1, D_2, two resonant inductors L_1, L_2 with an output filter formed by T-LCL parallel with load. The four power switches are uni-directional in nature. The operation sequence begins when MOSFET Q_1 and MOSFET Q_2 are in on-state and all of the other MOSFETs are in off-state and formed positive half-period of the desired output voltage V_o. On that stage, the PV array energy is transferred to the inductor L_1 and the stored energy is discharged to the utility grid line and giving positive polarity. The stage II is defined as the duration that MOSFET Q_3 and MOSFET Q_4 are in on-state and the rest are off-state, on that stage the PV array energy is transferred to the inductor L_2 and the stored energy is discharged to the utility grid line and formed negative half-period of the desired output voltage V_o. Table 1 illustrates the operation of stage of the proposed inverter and each state of MOSFET is listed in Table 2. The switch in each branch is operated alternatively so that they are not in same mode (ON /OFF) simultaneously and both choppers are operated at the fixed frequency in Discontinuous Current Mode (DCM) [12]-[14]. In practice they are both in OFF for short period of time called blanking time, to prevent short circuiting failure in inverter. These bridges legs are switched such that the output voltage V_o is shifted from one to another and hence the change in polarity occurs in voltage waveform. If the shift angle is zero, the output voltage V_o is also zero and maximal when shift angle is 180^0.

Table 1. Equivalent circuit of inverter in Stage-I & Stage-II

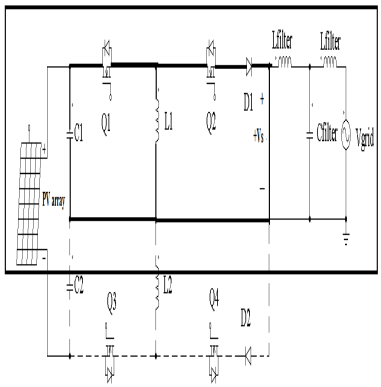
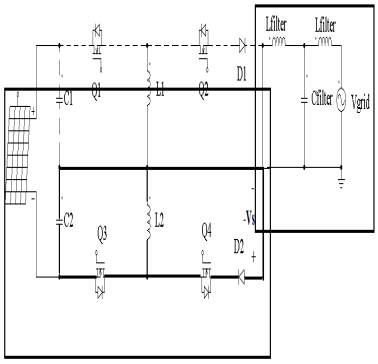
Stage	***True Circuit***	***Cycle Name***
I		Equivalent circuit of positive half cycle
Stage	***True Circuit***	***Cycle Name***
II		Equivalent circuit of negative half cycle

Table 2. State of MOSFETs

Stage	*Q1*	*Q2*	*Q3*	*Q4*	V_{out}
Stage-I	ON	ON	OFF	OFF	+Vs
Stage-II	OFF	OFF	ON	ON	-Vs

3.2 Input Capacitor Selection:

The average differential equation for input capacitor C_1 and C_2 is specified below:

$$C\frac{dv_c}{dt} = (1-D)i_L - \frac{V_{out}}{R} \quad (3)$$

The duty cycle of the inverter circuit is 75% and by solving the equation (3) the capacitor can be selected as $C=C_1=C_2=100\mu F$ where cutoff frequency f_c is 50 Hz. Thus, the input capacitor is responsible for desire ripple voltage, ripple current and loop stability.

3.3 Design of Circuit Parameters

In this section, mathematical calculations involved in the Transformer-less grid-connected buck-boost photovoltaic inverter is presented. Here assume that 24V four PV panels are connected in series hence desire input voltage is 96V. Table 3, illustrates the design specifications of proposed 700W grid-connected buck-boost photovoltaic inverter.

Table 3. Design specification of proposed buck-boost GTI

Symbol	*Actual Meaning*	*Value*
V_{ac}	Desire RMs Output Voltage	220V
V_{dc}	PV Array Voltage	96V
f_s	Output frequency	50Hz
I_{pk}	Estimated Inductor current in simulation	10.5A
N	Number of the switching times	200sec

3.4 Mathematical Analysis of Inverter

The port current I_1 and I_2 can be avergerd over the switching cycle according to Discontinuous Current Mode (DCM) operation [12]. In steps I and II equivalent resistance are assumed to be R_1 and R_2, therefore the equations are stated as following:

$$L\frac{dI_1(S)}{dt} + R_1 I_1(S) = V_{dc} \quad (4)$$

$$-L\frac{dI_2(S)}{dt} - R_2 I_2(S) = \sqrt{2}V_{ac} \quad (5)$$

Here L is the inductance of L_1 and L_2, the switching cycle of the inverter is S, V_{dc} is the PV array voltage and V_{ac} is output voltage of the inverter. Substituting $I_1(S)=I_2(S-1)$ in equation (4) and $I_2(S)=I_1(S)$ on equation (5) at time t=0, the above equations are resolved as follows-

$$I_1(S) = \frac{V_{dc}}{R_1} + [\{I_2(S-1) - \frac{V_{dc}}{R_1}\}e^{\{(-\frac{R_1}{L})T_{on}(S)\}}] \quad (6)$$

$$I_2(S) = \frac{-\sqrt{2}V_{ac}}{R_2} + [\{I_1(S) + \frac{V_{ac}}{R_2}\}e^{\{(-\frac{R_2}{L})T_{off}(S)\}} \quad (7)$$

As inverter is operated in DCM the above equations are simply expressed as follows:

$$I_1(S) = \frac{Vdc}{L} \times T_{on}(S) \quad (8)$$

$$I_2(S) = -\frac{\sqrt{2}Vac}{L} \times T_{off}(S) \quad (9)$$

$$T_{on} + T_{off} = \frac{1}{2Nf} \quad (10)$$

Where f is the utility grid frequency and $N=1/f$ is the number of switching times.

3.5 Inductor selection

A MOSFET switch in the input side is used to build the inductor current. The current waveform of the inductor is illustrated in Fig. 4(a). In the proposed inverter, the inductor current is operated in discontinuous current mode (DCM) [16]. In Fig. 4(a) T_t is the total time period of the switching cycle, T_{on} is the on time in one switching cycle, In Fig. 4(b), D is the duty cycle of the inverter and d.Tt is the fall time of inductor current.

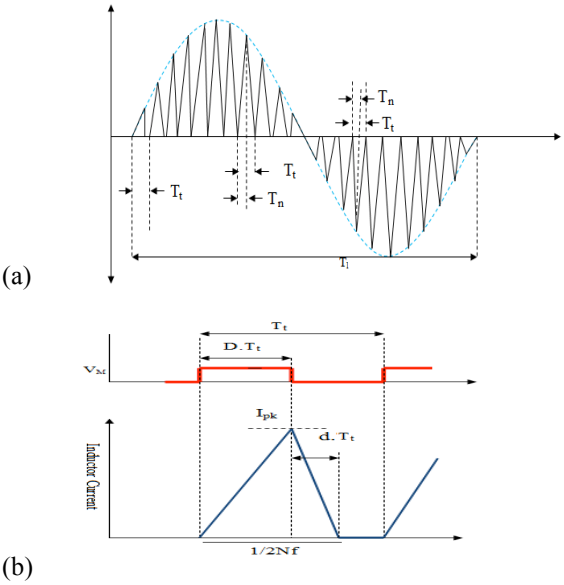


Fig. 4. Inductor current waveform (a) Input inductor current over one full cycle (b) Inductor current over one switching cycle

The peak value of the inductor current I_{pk} for general switching can be demonstrated as follow:

$$I_{PK} = \frac{Vdc \times DT_t}{L} = \frac{\sqrt{2}Vac}{L} T_{off} \quad (11)$$

Fig. 4(b) shows the waveform of inductor current in the Sth term.

$$T_{on} = \frac{LI_{pk}}{V_{dc}} \quad (12)$$

$$T_{off} = \frac{L \times I_{Pk}}{\sqrt{2}V_{ac}} \quad (13)$$

By substituting equation(12) and equation(13) in equation(9) the following equation is obtained–

$$I_{PK} = \frac{\sqrt{2}VacVdc}{2NfL(Vdc + \sqrt{2}Vac)} \quad (14)$$

By substituting equation (14) in equation (11), the design value of L_1=L_2 is obtained as:

$$L = \frac{\sqrt{2}Vac\,Vdc}{2NfI_{PK}(Vdc + \sqrt{2}Vac)} = 0.35mH \quad (15)$$

3.6 Control Circuit Design

In conventional inverter design, only one type switching method is used. But, in this proposed design instate of using one type of switching signal to switch the inverter, a combination of square wave and SPWM is employed. With this kind of combination switching, the switching loss across the switches of the inverter will be significantly reduced due to minimize the switching frequency. Block diagram of the proposed switching control circuit is shown in Fig. 5. In order to simplify the synchronizing process, the sine wave of proposed design will be sampled from power grid by using the voltage transformer to step down peak 312 V (RMS 220V) grid voltage into peak 7.07V (RMS 5V).

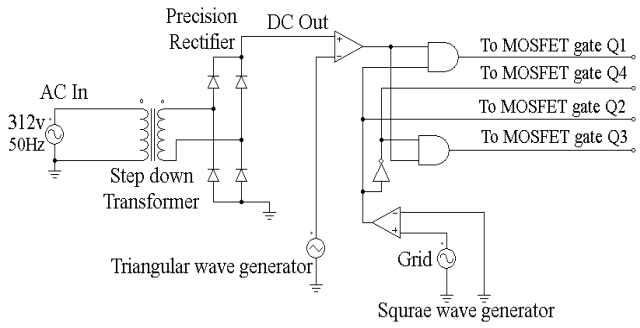


Fig. 5. Control circuit of proposed grid-connected inverter

With the sampled sine wave from the grid and used to generate SPWM signal. Thus the frequency of the output from the GTI will be having the same frequency as the grid voltage and current where this is one of the most significant requirement for the GTI.

After sampling, the sine wave is rectified with a precision rectifier. In addition, a high frequency triangle wave of 20 KHz frequency is used. Then the two signals are passed through a comparator to generate the uni-polar SPWM signal [15]-[16]. This unipolar signal only has positive values, which changes from +5V to 0V and again back to +5V. A square wave signal is used as the line frequency (50Hz for Bangladesh) and is in phase with the SPWM signal. Then the square wave signals is transmitted through a NOT gate to produce a signal that is 180^0 out of phase of the original signal. The inverter requires four switching signals since it has used four MOSFET switches. In order to generate four switching signals, two AND operation is performed between square wave and the SPWM signals. The switching signals can be categorized in four groups. The first group contains MOSFETs Q_1, the second group contains MOSFETs Q_2, while third group contains MOSFET Q_3, and the fourth group contains MOSFETs Q_4.

3.7 Closed-loop Control

In this proposed GTI design, we used a closed-loop controller scheme where the output current is measured and compared with an ac reference current signal [17] and provided fast dynamic response, strength and insensitivities to dc and ac as well as parametric uncertainties. Fig. 6. shows the block diagram of real-time waveform feedback closed-loop SPWM control method.

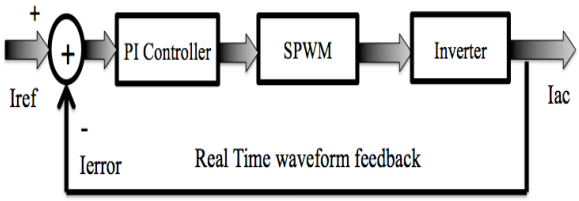


Fig. 6. Closed-loop control block diagram

The error in between the measured output current and the reference current is compensate by a Proportional Integral (PI) controller and is used to generate the desired SPWM switching gate signals for MOSFET Q_1, Q_2, and Q_3. In this closed-loop operation initially we calculate the peak modulation index M_a for 50 Hz grid voltage cycle by using of equation (4) and then this peak value is used to produce sinusoidal modulation index. A normalized sine table is used to get the modulation index in each switching cycle, from the peak modulation index. However, this modulation index is corrected via calculating new modulation index from the error between the measured ac current and reference current.

3.8 Grid Synchronization

This proposed grid-connected inverter design operation involves a grid synchronization part. During synchronization, the inverter produces output in phase with grid. The sine wave from grid is sampled and phase shift is set to zero. The un-shifted sine wave is rectified and compared with high frequency triangular wave to generate SPWM signal. SPWM signal is then undergoes an AND operation with square wave and generates three sets of switching signals. With this kind of switching and zero phase shifts, the output voltage and current of GTI controlled with the same phase with the grid. Whenever, the inverter and grid in phase once zero crossing of both voltages are detected the contactor is activated and the inverter is fed into grid. Fig. 7 is showing zero crossing result of GTI.

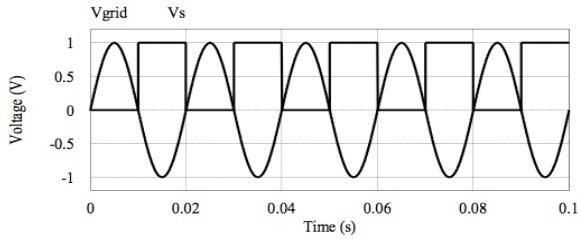


Fig. 7. Zero-crossing output result of GTI

Where the grid signal and square wave show the zero point at falling and rising edges. After both voltages are tied, the inverter begins to inject power into the grid. To avoid the grid to having power from the inverter when the grid is down and create undesirable accident, the free wheeling diode is employed between the grid and the inverter MOSFET power circuit that will block the reverse power flow from grid. This isolation process is to avoid the grid to become live part on the time when it should not be.

3.9 Filter circuit design

To eliminate harmonics from the inverter output, filter circuit is employed. In conventional inverter, LC filter is used but this article is employed a T-LCL immitance converter. The filter circuit consists of two inductors L_1 and L_2, and a capacitor C, in a T shape. From the derivation of the equation the output current of the filter, I_0 is found as [18]-[21]:

$$V_i = Z_0\left[1+\frac{1}{Q}\frac{Z_L}{Z_o}\right] \tag{16}$$

$$I_0 \cong \frac{V_i}{Z_0}\left[1-\frac{1}{Q}\frac{Z_L}{Z_o}\right] \tag{17}$$

Where V_i is the input voltage, Z_L is the load impedance, Q is the quality factor

$$Q = \frac{\omega L}{r} \tag{18}$$

With $\omega = 2\pi f$ is the angular frequency, r is the internal resistance of the inductor and Z_0 is the characteristic impedance determined by the filter component L and C:

$$Z_0 = \sqrt{\frac{L}{C}} \tag{19}$$

When the internal resistance of the inductor is negligible or zero, the quality factor becomes infinity. Under this condition, the second term becomes zero, giving the ideal condition:

$$I_0 \cong \frac{V_1}{Z_0} \tag{20}$$

From equation (20) it is observed that the output of T-LCL filter is independent of load. Therefore, in the proposed inverter, a T-type LCL immittance converter is applied as a filter circuit because it is not only capable in reduction of harmonic but also helpful to maintain constant current at the load.

The value of C and L of T-LCL filter (considering Butterworth type) is calculated using the condition of cut-off frequency of low pass filter,

$$Z_0 = X_C = \frac{1}{2\pi f_C C} \tag{21}$$

Where Z_0 is the characteristic impedance given by equation (19). In the proposed design, the cutoff frequency, f_C =50Hz and characteristic impedance is assumed as 20Ω. Therefore, the value of C and L is calculated using equations (21) and (19) as,

$$C = \frac{1}{2\times\pi\times f_C\times Z_0} = \frac{1}{2\times\pi\times 50\times 20} \approx 0.159mF$$

$$L = CZ_0^2 = 0.159\times10^{-3}\times(20)^2 \approx 63.60mH$$

4. Simulation Result and Discussion

The proposed GTI design will undergo a computer simulation using powersim (PSIM) software. To confirm the mathematical modeling analysis in the previous section, 700W of the proposed buck boost GTI is simulated. The complete simulated schematic diagram of the proposed buck-boost GTI is shown in Fig. 8. Fig. 9 shows the simulated output voltage waveform, which is non-sinusoidal and distorted, and contains excessive harmonics. A low-pass T-LCL filter is used at the output terminal of the inverter to reduce the harmonics thereby producing a pure sinusoidal output voltage.

After filtering, 220V (RMS), 50Hz pure sine wave output voltage is obtained and shown in Fig. 10. It is observed that the output voltage of proposed inverter becomes stable after couple of cycles.

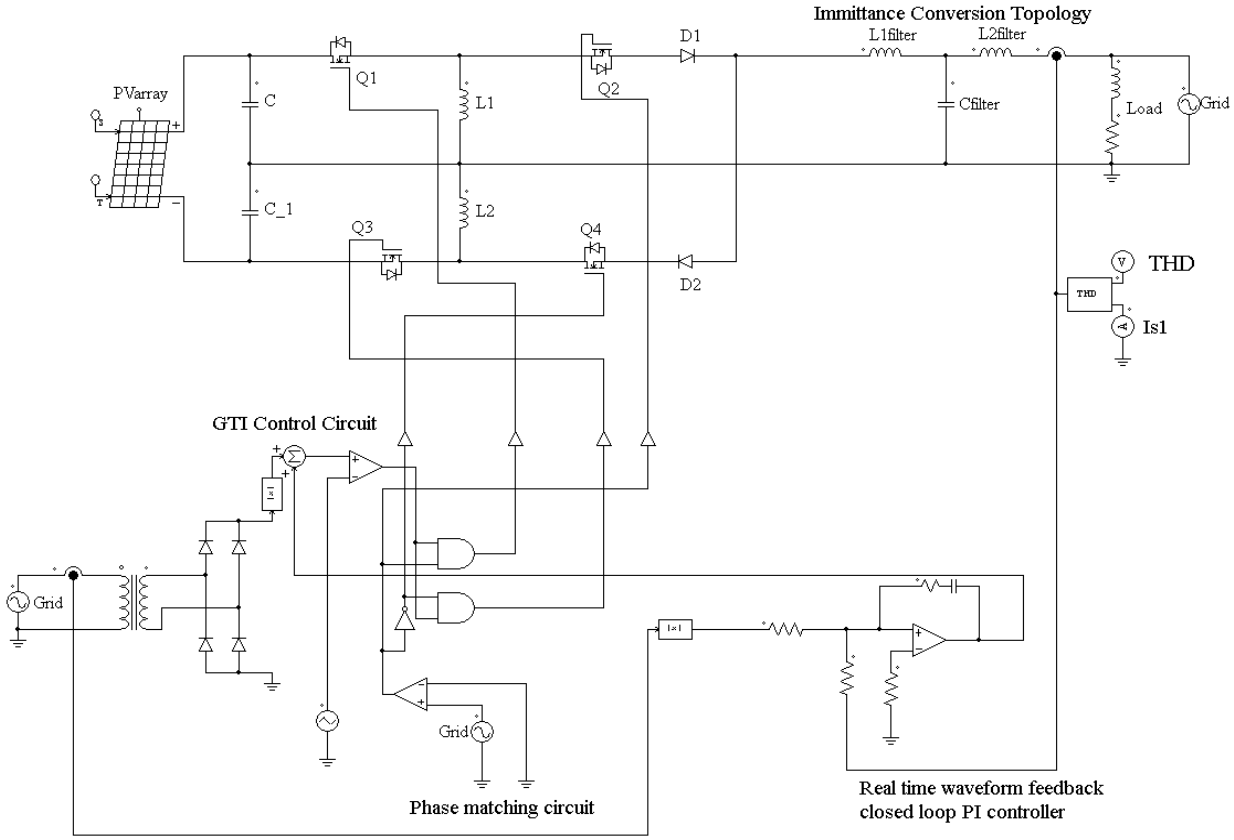


Fig. 8. Complete schematic diagram of three-switch buck-boost GTI in PSIM

Therefore this is affirmed that voltage, frequency and phase of the inverter output are exactly matched with the grid voltage, frequency and phase.

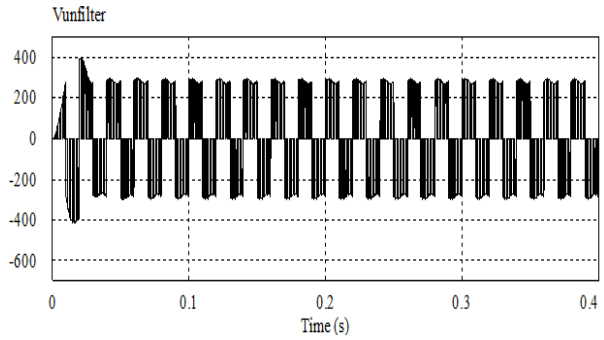


Fig. 9. Output voltage waveform without filtering in PSIM

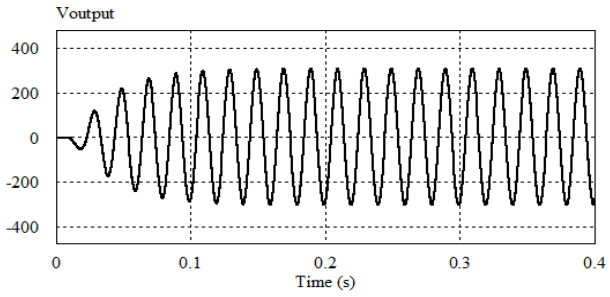


Fig. 10. Output voltages after filtering in PSIM

The peak value of the inverters output current is an important factor in designing the inverter stack size. The inverter current rating is normally determined by the filter impedance and the rated load impedance in a steady state. The output current should be maintained constantly. Fig. 11 illustrates the inverter output current which becomes stable within a couple of cycles. And Fig. 12 shows the simulation results, where the Total Harmonic Distortion (THD) of output current is about 0.9%.

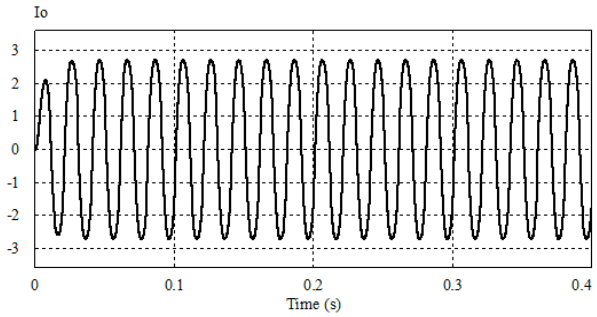


Fig. 11. Output current waveform in PSIM

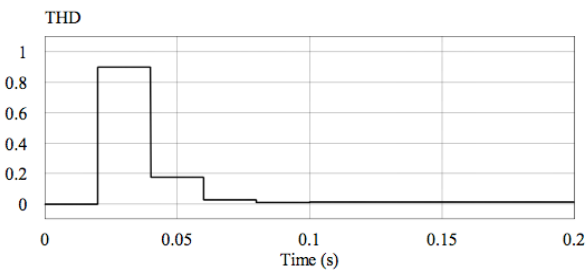


Fig. 12. Output current THD of GTI

Fig. 13 presents the FFT analysis of output voltage in unfiltered and filtered condition. The Fast Fourier transform ensures that unfiltered inverter output has harmonics with mentioned value but filtered output has only fundamental harmonics which lies with in 50Hz and rest of harmonics are negligible. After filtering the output has very low level of THD less than 1% because the proposed circuit is totally transformer less.

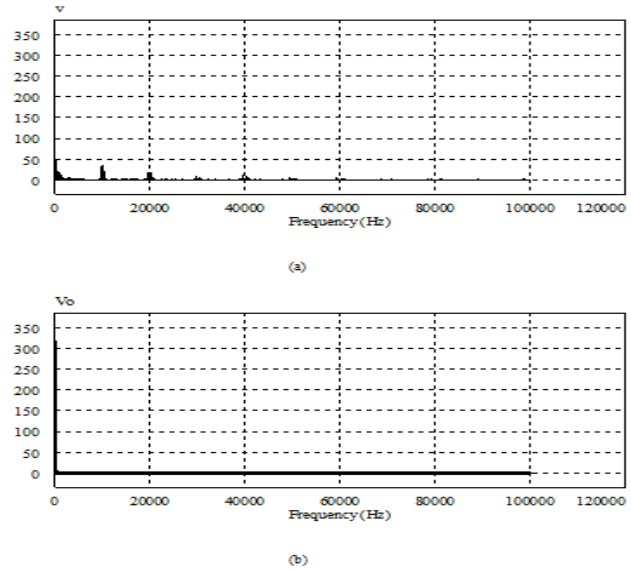


Fig. 13. Output Voltage's FFT (a) before filtering (b) after filtering

The load impedance was changed to verify the output current of the GTI. Fig. 14 shows output load current versus load impedance of the GTI. The load impedance was varied from 5Ω to 100Ω considering characteristic impedance of the circuit Zo=20Ω, and applying without any filter at the output. The same procedure was applied for LC and T-LCL filter. It is observed that output current is remained constant in case of LC and T-LCL filter whereas output current varies greatly in the absence of any filter with the change of load impedance. Moreover output current variation in T-LCL filter is less than LC filtering.

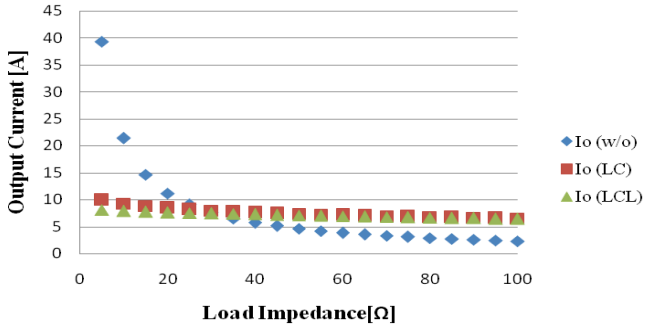


Fig. 14. Output current vs. load impedance

The inverter's efficiency is calculated using the following formula:

$$\eta = \frac{p_{out}}{p_{in}} \times 100\% \qquad (22)$$

Where P_{in} and P_{out} are the input and output power of the inverter. By varying resistive load, the efficiency of the inverter was monitored with LC and T-LCL filter as illustrated in Fig. 15. It is observed that the efficiency of T-LCL filter is slightly higher than that of the conventional LC filter due to its constant current characteristic.

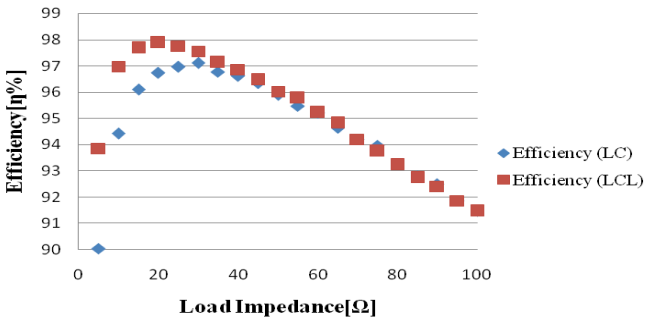


Fig. 15. Efficiency vs. Load impedance

Table 4 reviews the output current and voltage performances. Thus it is observed from table analysis and as compared to the [8]-[12], that inverter output is optimum when modulation index is 0.90.

Table 4. Summary of transformer-less inverter simulation result in PSIM

Modulation Index	Voltage THD *(before filtering)*	Voltage THD *(after filtering)*	RMS Output Voltage *Vo(V)*	Power Factor	Power P_o *(Watt)*
0.3	1.79	0.01	100.25	0.99	115
0.6	1.45	0.007	125.50	0.99	455
0.8	0.94	0.008	165	0.99	560
0.9	0.89	0.009	220.05	0.99	700
1.5	0.87	0.013	250	0.99	890
2.0	0.91	0.014	310	0.99	1145
2.5	0.90	0.016	380	0.99	1445
3.0	0.91	0.016	410	0.99	1870

5. Conclusion

This paper presents a novel transformer-less photovoltaic grid-tie inverter power circuit. The proposed PV system employs a high step-up ZVT-interleaved boost converter with winding-coupled inductors and active-clamp circuits as the first power processing stage, and high voltage gain is obtained and verified by the simulation results. A 700W simulation circuit is designed and the simulation results confirm the validity and applicability of the proposed photovoltaic system. Therefore the results verified the viability of the proposed transformer-less GTI for photovoltaic applications and confirmed the capability of the inverter to feed a sinusoidal voltage to the utility grid.

In future, hardware of the proposed transformer-less GTI will be constructed with the help of a microcontroller.

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