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Technological Advances in A-Si: H/c-Si Heterojunction Solar Cells

Kamlesh Patel*‡, Pawan K. Tyagi**

* Department of Electronic Science, Univ. of Delhi South campus, New Delhi -110021, India

** Department of Applied Physics, Delhi Technological University, Delhi -110042, India

(kpatel@south.du.ac.in, pawan.phy@dce.edu)

‡Corresponding Author; Kamlesh Patel, Department of Electronic Science, University of Delhi South campus, Benito Juarez Road, New Delhi -110021, India, Tel: +91 11 24110440,kpatel@south.du.ac.in

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Abstract- Cost effective silicon-based thin-film solar cells have attained a sustainable age with stable in comparison to the crystalline silicon solar cells. The heterojunction solar cells based on amorphous silicon/crystalline silicon heterostructures are producing efficiency more than 22%. The research activities have led to such high efficiency through a number of technological developments. To make the surface passivation better at the top of c-Si substrate, a thin intrinsic a-Si: H layer is deposited in between the a-Si:H layer and c-Si substrate and such configuration has famous as Heterojunction with Intrinsic Thin-layer (HIT) solar cells. Various research methodologies used for the efficiency improvement in HIT cells have been developed in ages and now the HIT cells with efficiency better than 24% are being manufactured. The simultaneous developments of characterization methods well supported the improvements in fabrication technologies to analyze their self-governing effects on the deposited amorphous films, c-Si substrates and device performances. A number of characterization facilities have been established, which are based on the evaluation of effective carrier lifetime, density of interface states, recombination rate, cell efficiency, band offset, current density-voltage characteristics, charge carrier concentration, photoluminescence, activation energy etc. The present paper reviews the fabrication technologies for the development of these reported solar cells and their characterizations as well at the material and device levels.

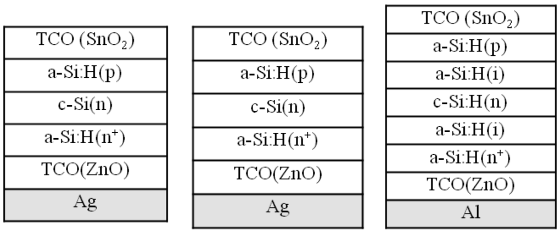
Keywords- Cell efficiency; heterojunction; HIT cell; PECVD; Thin film silicon.

1. Introduction

In the last two decades, the interest in the photovoltaic field has expanded with the awareness of the need for searching the alternative and green sources of energy due to the limited conventional and dangerous power sources, i.e. Coal (Thermal), Nuclear power, etc. The p-n junction based crystalline silicon (c-Si) solar cells dominates 80% of the photovoltaic industry as such cells received equal support from the microelectronics research and development. Thin-film based hydrogenated amorphous silicon (a-Si: H) and hydrogenated microcrystalline silicon (μc-Si: H) semiconductor materials are commonly used in making p-i-n thin-film structures.

Other heterostructures are combination of materials of different bandgaps or work functions, like a-Si: H/c-Si, CdS/CdTe and Cds/CIGS solar cells. The silicon based heterojunction solar cells are an appealing technology as the combinations of crystalline silicon wafer technology (high performance) and thin silicon film technology (low material consumption and low temperature process). Such heterostructure allowed the combination of the best suitable properties of different solids, passivation of c-Si wafers and realization of low temperature processing for solar cells. In other words, the wafer PV technology has a limitation due to high raw-material costs, whereas thin-film technologies allow for an important reduction in semiconductor thickness due to its capacity to absorb most of the incident sunlight within a few microns of thickness compared to the several hundred microns in the wafer technology. In addition, the thin-film technology has an enormous prospect of cost reduction, based on the flexibility to make strong, large-area monolithic modules with a fully automatic fabrication procedure.

Silicon heterojunction cells are made up of a crystalline silicon absorber onto which one or more thin-film silicon layers are deposited and are now reporting efficiency ~22%, which is near to the theoretical values of ~23% for c-Si cells. These cells have a great demand in the commercial sector at many places and now are being used in household for power generation. Conceptually, improving the passivation of c-Si surface led to the development of another configuration known as HIT (Heterojunction with Intrinsic Thin-layer) cell, which has now reached ~25%. Fig. 1 represents the typical configurations of heterojunction and HIT solar cells, which are configured as TCO(SnO2)/a-Si:H(p)/c-Si(n)/a-Si:H(n+)/TCO(ZnO)/Ag,TCO/ a-Si:H(p)/a-Si:H(i)/c-Si(n)/a-Si:H(i)/a-Si:H(n+)/TCO/Al and bifacial HIT solar cell, i.e., the TCO/a-Si:H(p)/a-Si:H(i)/c-Si(n)/a-Si:H(i)/a-Si:H(n+)/TCO/Al.



(a) Heterojunction (b) HIT cell (c) Bifacial HIT

Fig.1. Various forms of heterojunction cells.

In the development of such kind of highly efficient cells, several fabrication techniques are being used. Some of them are plasma-enhanced chemical vapour deposition (PECVD), very high frequency (VHF PECVD) and hot-wire CVD (HWCVD), plasma-spray silicon growth (PSSG), liquid-phase epitaxy (LPE) molecular- beam epitaxy (MBE) etc. Among these techniques, PECVD process is widely used and investigated for high growth rate and low hydrogen contents [1]. The RF PECVD (13.56 MHz) has the advantages of high power density, high pressure depletion, pulse-modulation of RF power and high gas flow rate, whereas VHF PECVD (60 MHz) has a high excitation frequency, lower ion energy and high ion density. The various analytical techniques have been established to analyze the improvements in the materials and devices.

In this review paper, about 48 research papers published in the last decade and 4 books were consulted mainly to summarize the advances in fabrication and characterization technologies for a-Si: H/ c-Si heterojunction cells.

2. Advancement in Heterojunction cell development and efficiency

Song et al. [2] has investigated the carrier transport mechanisms in undoped a-Si: H/p-type c-Si heterojunctions with and without a microcrystalline (mc)-Si buffer layer for their photovoltaic properties. It has been shown that the conduction at the junction largely depends on the defect state distribution and band offset at the hetero-interface. The two mechanisms at the junction or interface control the conduction behavior, the recombination process at the low forward bias (V<0.3V) and the multistep tunneling capture emission (MTCE) at the higher bias region (0.3<V<0.55 V). Their effects become negligible after the conduction attained a space charge limited condition (V>0.55 V). A 200 Aº thick mc-Si buffer layer deposited in between the a-Si:H (700Aº)/c-Si interface, improved both the carrier transport and shorter wavelength response and so using an anti-reflecting coating, efficiency has reached to 10%. An amorphous silicon/crystalline silicon hetero solar cell measured for its current–voltage under the illumination condition and quantum efficiency characteristics before and after exposure to high-energy (1.7 MeV) protons as in [3]. The effective electron diffusion length of the crystalline silicon was found 430 mm after irradiation by 5 × 1012 cm-2 protons compared to the previous value 434 mm. The measured and simulated results using a finite-element simulation program DIFFN have shown good agreement of 30% efficiency degradation after irradiation dose of protons for heterojunction solar cells.

Tucci and Cesare [4] has described the process for high efficiency amorphous/crystalline silicon heterostructure solar cells on p-type crystalline silicon. On the top of c-Si wafer intrinsic amorphous silicon used as a buffer layer and n-type amorphous emitter have been deposited using the 13.56 MHz PECVD process. The chemical treatments by chromium, KOH and 1% HF solutions on the n-a-Si:H layer, have increased the conductance and reduced of the activation energy of the layers. The I-V characteristics under AM 1.5 condition have shown an efficiency of 17% on 2.25 cm2 area for p-type c-Si substrate. By applying a high hydrogen diluted gas mixture, n-type mc emitters were deposited on the intrinsic a-Si:H buffer layer by RF PECVD as in [5]. The optical spectra of n/i double layers has confirmed that the i-a-Si:H layer is unaffected on c-Si substrate after deposition. The n-type mc-Si:H emitters increasing the short circuit current (Jsc) and efficiency by a factor 1.24 and 1.38 respectively, compared to a-Si:H emitters for solar cells. An effect of the Back surface field (BSF) was investigated by Goldbach et al. [6] using a p++ μc-Si:H layer on highly doped i-μc-Si:H layers for various activation energy on a glass. The activation energy was evaluated against the Trimethylboron (TMB)/SiH4 flow for the deposition on glass and i-μc-Si:H layers. The drastically reduced activation energy was found as Ea = 0.08 ± 0.01 eV compraed to 0.15 ± 0.01 eV. The results showed that incorporation of such BSF enhances Voc by 22.4 mV and Jsc by 4.6 mA/cm2 and leads to high efficiency to 14.87% compared to the reference cell efficiency 11.86% without a back surface field.

Lacoste et al. [7] has reported the efficiency limits of heterojunction solar cells in terms of the sensitivity of open circuit voltage Voc for an intrinsic layer and various recombination mechanisms. Different characterization methods were used for studying the HJ cells, namely quasi-steady-state photoconductance, capacitance verses temperature and frequency, capacitance–voltage (C-V), quantum efficiency and current–voltage (I-V) measurements. The solar cells were then modeled by a new simulation code and the best heretojunction cell has achieved 15.20% efficiency without texturing the substrate. For textured p-type substrates, the Voc was recorded 677 mV and found that the intrinsic layer and recombination at the interface have no effect for optimized cells. This is due to the stronger conduction band offset at the interface for p/n single heterojunction than n/p ones. A triple paradox was observed as the Voc was found to be more sensitive to interface recombination for n/p single HJ than for p/n one. The intrinsic layer has increased Voc by 35 mV for p/n single HJ and negligible effect on Voc for n/p ones. The best Voc is obtained for the most resistive wafer (NA = 9 × 1014 cm-3) by the AFORS-HET simulations.

The influence of the interface quality was studied by Mavdell et al.[8], which was based on the output characteristics of a-Si:H/c-Si HJ solar cells. A simulation study found that the solar cell efficiency is greatly depending on the interface states as the open circuit voltage is varied in accordance with the density of states. The photoluminescence measurements showed that the interface quality can be optimized by changing the deposition conditions of the thin a-Si:H films. The electronic properties by the photoelectron yield spectroscopy (PEYS) have observed the upward shifts in Fermi-level and Urbach energy as a function of [PH3]/ [SiH4] flow ratio. A new cell concept was proposed to illuminate the back side of the conventional a-Si:H/c-Si solar cell for proper utilization of the light absorption in a highly doped emitter as in [9]. In this configuration, a-Si:H emitter will have only a fraction of light as mostly absorbed by c-Si substrate. In addition, the charge carrier took the longer path to reach the junction, so the lifetimes of minority carrier have been increased. Application of a thin 70 nm Si3N4 film as an anti-reflecting coating has added a good passivation. In the final stage, this new cell produced 11% efficiency in the first attempt.

The properties of hydrogenated nanocrystalline silicon (nc-Si:H) n-layers have been studied by Xu et al.[10] using Raman spectroscopy, activation energy of dark-conductivity and optical transmittance. These layers have been used to develop heterojunction solar cell on flat p-type c-Si wafers by RF PECVD. These wide bandgap nc-Si:H layers have fine grained nanocrystallines integrated into the amorphous structure and low activation energy. The HJ cells were formed on Ag (100 nm)/IT0 (80 nm)/n-nc-Si:H (15 nm)/buffer a-Si:H/p-c-Si (300 lm)/Al (200 nm) configuration with a very thin i–a-Si:H as a buffer layer. Before the deposition on nc-Si:H layer, the p-c-Si substrate was given H2 plasma treatment after passivation by the thin i- layer. Due to these surface preparations, a 14.1% efficiency was found in the hetererojunction cells of size 2.43 cm2. Fuhs et al.[11] has studied the material and device parameters of a-Si:H/c-Si heterojunctions for their applications of solar cells and light emitting diodes (LEDs). Band offsets are used to characterize the electronic properties of these structures in the p/n and n/p configurations. The band bending ΔEC and ΔEV have been found 0.14 eV and 0.45 eV, respectively at the conduction and valence bands. The efficiency of a textured a-Si:H(p)/c-Si(n)/a-Si:H(n) solar cell was obtained 19.8% without any i-a-Si:H layers.

The effectiveness of silicon surface passivation was studied on Si <100> and <111> wafers based on the effective minority carrier lifetime (τeff) measurements by Das et al. [12]. The correlation of the passivation in front of emitter structure and interdigitated back contact (IBC) structure have shown the τeff >1 msec and high efficiency performances of the silicon heterojunction (SHJ) cell. By the deposition of the buffer layer using the DC plasma, Voc of 694 mV was found on n-type textured substrate. In an IBC heterojunction structure, Voc is obtained 683 mV and it showed the possibility of further exploration of fill factor in order to improve the efficiency. The effects of texturing and surface passivation have been investigated in terms of the carrier lifetime by Edwards et al. [13]. With the correct preparation of silicon wafers, the heterojunction solar cells produced very high Voc and Isc by deposition of a-Si:H layers. The effective wafer lifetimes increase by NaOH texturing of wafers and by further thinning. By optimizing the deposition conditions of RF PECVD and low temperature annealing, the lifetimes were found maximum of 1 ms range, which were measured using an inductively coupled photoconductance bridge. The efficiencies have found about 17.6% for these solar cells due to low reflectance.

From dispersive hydrogen diffusion or retrapping hydrogen motion in the interface passivation kinetics, Wolf et al. [14] has shown that the properties of a-Si:H films have stretched-exponential-behavior at the interface of a-SiH/c-Si structure. The amphoteric interface state (or Si dangling bond) reduction influenced the carrier injection and recombination rate at the interface instead by a field effect. The study proved that the obtained interface electronic properties are same as of the a-Si:H bulk material and having similar amount of defects. Mora-Sero et al. [15] has developed the heterojunction solar cells as a thin a-Si:H films deposited on crystalline silicon (c-Si) wafers and configured as ac equivalent circuits. The carrier lifetime is defined in terms of the electron capture time tn and was found same as the Shockley–Read–Hall (SRH) recombination time tSRH. The capture rate of electrons and holes at the interface was determined by modeling the recombination process as the simple RC circuits.. The impedance spectra results showed that the longer time constants t»300μs can be found with the electron capture process. By the effect of Al annealing, the electron concentration is decreased in the region near the back contact c-Si. Also tn steeply rises with the increase of temperature whereas tp is having a minor reduction under the forward bias condition.

To achieve high efficiency solar cells, the epitaxial growth at the interface should be low as much as possible in case of heterojunction cells. Fujiwara et al. [16] has demonstrated that this epitaxial growth could completely removed by depositing the intrinsic a-SiO: H layer on n-type and p-type c-Si substrates at high growth temperatures and low RF powers. The real time spectroscopic ellipsometry (SE) and infrared attenuated total reflection (ATR) spectroscopy results have confirmed that the application of the wider band gap material like a-SiO:H reduces the epitaxial growth to the heterojunction solar cells in comparison to a-Si:H materials. So for a-SiO: H/c- Si solar cells, the obtained efficiencies were 16.0% and 14.8%, respectively in p/n and n/p configurations. Korte et al. [17] has reported the progress in a-Si: H/c-Si heterojunction solar cell technology in terms of fabrication and characterization. Maximum cell efficiency is dependent on four factors for minimization of recombination at the junction, (1) wet chemical based pre-treatment of c-Si wafer, (2) optimum doping of a-Si:H materials by RF PECVD, (3) thermal and (4) plasma based post treatments of the a-Si:H/c-Si cell. With the combination of these processes, the efficiencies for the n- a-Si: H/p-c-Si and p) a-Si: H/n-c-Si cells have obtained 18.5% and 19.8%, respectively.

The effect of Au surface Plasmon resonance has been investigated for Au nanoparticles (NPs) /(n-type) a-Si:H/(p-type)c-Si heterojunctions by Losurdo et al. [18]. The heterojunctions have been developed using PECVD followed by Au sputtering for contacts. The use of Au NPs improved the absorption of the light due to the surface plasmon resonance using SiF4-H2 plasmas. It has been proved that the Au NPs with a density of 1.3 × 1011 cm-2 enhances the n-type a-Si:H/p-type c-Si heterojunction performance deposited for 20 nm diameter. The resonance results process have shown the 20% increase in Jsc, 25% in power output Pmax and 3% in the fill factor FF. The enhanced absorption of light by the plasmon resonance is correlated with the cell performance by means of spectroscopic ellipsometry, atomic force microscopy (AFM) and I–V measurements. Stangl et al. [19] has proposed a new design called a planar rear emitter back contact silicon heterojunction (PreBC-SHJ) solar cell design. This concept is a combination of point contacts, and back contacts with the silicon heterojunctions for high efficiency advantages. A planar a-Si:H emitter layer is deposited on the rear side of the device at low temperature and point or stripe contacts to the solar cell absorber were built inside the emitter, which are insulated electrically. This new design has advantages of less structuring, allowing comparatively a larger sizes and easy application of low-cost patterning. The numerical modelling of the BC-SHJ has shown the potential of 24% efficiency and the reported Pre BC-SHJ solar cells have achieved 13.9% practically.

The correlation between efficiency and emitter- deposition temperature was studied by Barrio et al. [20] for a single silicon-heterojunction solar cells. The two methods have been used to find out the surface-recombination velocities, first by fitting the current–voltage characteristics to a theoretical model and second, by the Quasi-Steady-State Photoconductance Technique (QSSPC). The effective diffusion lengths of the minority carriers have been estimated from internal quantum efficiencies for better understanding of bulk and back-interface recombination. By optimizing the various deposition conditions for emitter and back surface field at the real Al contact, a cell with efficiency 12% has been developed. In conclusion, efficiency degraded due to the increase of dangling bond density at higher deposition temperatures i the developed cells. For full dry fabrication of heterojunction solar cells, Moreno et al. [21] studied the low temperature process (Tsub >200 °C) for the c-Si substrate cleaning and its passivation. The SiO2 was etched from c-Si wafer by means of H2–SiF4 plasmas in a standard RF PECVD reactor. The process conditions were optimized by using the results of In-situ ellipsometry in order to get the well passivated surface. Prior to the deposition of a-Si:H layers, a number of plasma pre-treatments were applied on c-Si wafer for the reduced recombination rate. These treatments result the generation of minority carriers of high effective lifetimes (teff »1.55 ms), lower surface recombination rate (Seff ≤ 9 cms-1) and high open circuit voltages (Voc » 0.713 V).

The relationship between the passivation quality of thin a-Si:H layers and the plasma conditions was investigated by Descoeudres et al. [22] . The films were deposited using a 40.68 MHz PECVD reactor, which was having a plasma impedance probe between the matching network and the electrode power feed-in for plasma diagnostics. In situ measurements have shown that the silane depletion fraction is important during deposition for the good interface passivation. Based on this analysis, 4 cm2heterojunction cells with efficiencies upto 20.3% have been produced. Ji et al. [23] has analyzed the crystalline behavior of a-Si:H thin films deposited using the effective medium approximation (EMA) method of a spectroscopic ellipsometer (SE) on n-type Si substrates. The passivation quality of these films has been studied in terms of simultaneous measurements of the effective carrier lifetime (teff) and Voc by QSSPC technique. The deposition of a-Si:H layers can be controlled precisely to obtain the doping level in the range of 0% (amorphous phase) to 90% (polycrystalline phase) on RF PECVD. The crystallinity is found more important for passivation in p-a-Si:H layers than n-a-Si:H as the sentitive nature of crystallinity towards the deposition rate for n-a-Si:H. The results have shown that crystallinity less than about 5% for p-a-Si:H and 20% for n-a-Si:H have given the same Voc of 650 mV. The HRTEM has established the effectiveness of SE measurements in accordance with the EMA modeling i.e. the major part of crystallinity has an epitaxial growth configuration at the a-Si:H/c-Si interface. With the optimized deposition conditions using this analysis, a cell efficiency of 17.17% has been achieved on a non-textured substrate.

The hydrogen plasma treatment is performed for improving the efficiency of heterojunctions cells and its effect on the performance of cells were studied by Descoeudres et al. [24]. After the H2 plasma treatment, the bulk a-Si:H has became more disordered and the hydrogenation of interface was improved in terms of high carrier lifetimes. For the polished and textured n-type substrate of area 4 cm2, the lifetimes were obtained upto 11.2 ms and 7.2 ms respectively, after the proper H2 treatments. Using RF and VHF PECVD, the fabicated solar cells have shown an efficiency of 20.6% and 21.0%, respectively due to increased Voc. Haschke et al. [25] has compared the experimental results of back-contacted a-Si:H/c-Si heterojunction solar cells having FF upto 78.8 % with thier calculated J–V characteristics. The recombination currents obtained from the lifetime measurements were added and used in the calculation of J-V characteristics. The effects of intrinsic buffer layer property were also investigated by deposition on the p-type a-Si:H emitter for the solar cell structures. From the J-V measurements, it was concluded that the fill factor reduction was dominated by the charge-carrier transport due to the i- a-Si:H buffer layer and the solar cells with efficiency about 20% were developed.

3. Advancement in HIT development and efficiency

Tanaka et al. [26] has introduced an a-Si/c-Si heterojunction solar cell with a thin intrinsic a-Si:H layer at the interface, which was given the name, the HIT (Heterojunction with Intrinsic Thin-layer) solar cell. This cell has shown the conversion efficiency more than 14.8% at a low temperature <200 °C. By applying textured substrate and back surface field technologies, the short circuit current Isc increased upto 37.9 mA/cm2 and fill factor (FF) of more than 0.8 was found. The efficiency of this modified ACJ-HIT was obtained 18.1% and its output characteristics were remained stable after 10 hours. A bifacial HIT cell with a total area conversion efficiency of 20.7% and high open circuit voltage (Voc) of 719 mV was fabricated on n-type solar-grade CZ-Si wafer of size 100.5 cm2 as in [27]. The excellent surface passivation of the a-Si:H/c-Si heterointerface was proved by the measured effective carrier lifetime of the Si-wafer closer to the bulk lifetime using the microwave photo conductivity decay (mPCD) method. The details for the model HIT Power 21 of 18.3% efficiency with its temperature characteristics and symmetrical structure were specified at the mass level of production. Using the current-voltage characteristics (IV), photoluminescence (PL) and ultraviolet photo electron spectroscopy (UPS), a simple structure TCO/a-Si: H (n) /c-Si (p) heterojunction solar cells with vane emitters have been studied as in [28]. The cells have been prepared with and without intrinsic a-Si:H(i) buffer layer between n-a-Si:H and p-c-Si wafer substrate. An enhancement in the PL signal confirmed a better passivation by i-a-Si:H layer and UPS results have proved a reduction in defect state density in ultra thin a-Si: H (I) compared to a-Si: H (n) layers. These effects finally contributed to the increase in efficiency to 16.2% compared to lower efficiency without i-a-Si:H layer.

Tanaka et al. [29] hs reported the HIT cell with a highest conversion efficiency of 21.3% over a practical cell size of 10 x 10 cm2. To achieve such performance, core technologies were applied for the improvement of a-Si/c-Si heterojunction, enlargement of effective area, reduction in optical losses inside a-Si:H and TCO layers. As a result of better heterojunction, Voc was obtained greater than 700 mV. Also the deposition parameters of a-Si:H and TCO layers were optimized to reduce the absorption loss. In addition, the random texture on c-Si by the wet chemical process has improved the efficiency at short-wavelength region. Fabricating fine electrodes helped to utilize their effective areas which reduced the resistive losses. Based on these modifications, 200W HIT solar cell modules with 19.5% efficiency have been commercialized in mass production by Sanyo Electric Co. Ltd. Taguchi et al. [30] has shown that due to the improvement in the carrier lifetimes, the 100.3 cm2 HIT cell has exhibited a high open circuit voltage Voc of 712 mV and produced 21.5% efficiency. For high-quality a-Si films with low plasma damage processes, the studies have reported that at the heterointerface, the strong electric field reduced the recombination and it was generated by lowering the interface state density achieved by good c-Si cleaning and high quality a-Si:H films. To collect the minority carriers efficiently, the deposition conditions were optimized to control the band offset in the valence band at the interface. Also these cells have shown a better temperature coefficient of – 0.25%/°C than the previously reported – 0.33%/°C due to high Voc.

The recombination rate at the amorphous/crystalline silicon interface was studied by developing a physical model as reported by Garin et al. [31] for HIT structure. The interface recombination rate was calculated in terms of the effective lifetime teff against the average excess minority carrier concentration (Dn) under illumination. The QSSPC technique was used to measure the effective lifetime teff for a number of prepared HIT structures. The interface parameters and the doping density of the a-Si:H layer were then found by comparing the physical model with the experimental data. It was observed that the a-Si:H(p)/a-Si:H(i)/c-Si interfaces has reduced recombinations due to its Fermi-level position than that of the a-Si:H(n)/a-Si:H(i)/c-Si counterparts. It means that p-a-Si:H films have low doping concentration due to improper activation of boron.

Wolf and Kondo [32] has studied the surface passivation quality of the i-am-Si: H films against the temperature variation. The depositions of these films were carried on low resistivity (~3 Ωcm) p-type float-zone silicon substrates by 13.56 MHz RF PECVD. The maximum temperature of deposition have optimized to the value of temperature where epitaxial interface starts growing. Further annealing of these films improved the passivation of the interface due to the structural relaxation with time. For various deposition conditions, it was found that the passivation quality improves exponentially over a low temperature range (120 ºC to 260 ºC). Taguchi et al. [33] has evaluated the conduction mechanism and temperature dependence of HIT structure solar cells against the thickness of the undoped amorphous silicon layer. The carrier transport property of this device was obtained using the diffusion model at the high-forward-bias region (0.4 <V< 0.8 V), whereas the current transport was found using the multistep tunneling model at the low-bias region (0.1 <V< 0.4 V). The tunneling through the localized states in a-Si:H and surface recombination velocity have reduced by the high-quality i-a-Si:H layer at the heterointerface. The change in conductivity of a-Si: H layer decides the FF and high Voc leads to a highly suppressed saturation current in HIT structure. These all improved parameters have led to stable output power against the temperature variation and the variations occurred due to increasing series resistance with temperature.

Kim et al. [34] has deposited the intrinsic a-Si:H layer between a doped emitter and a c-Si wafer using PECVD and investigated its properties due to H2 dilution. It was observed that a low H2 dilution i.e. H2/SiH4 ratio of 2 and 4 have improved the passivation performance during the deposition of i-a-Si:H layer and so the quality of this layer was enhanced in comparison to a-Si:H film without H2. The performance of cell degraded for higher H2 dilution ratio due to more carrier recombinations. However, an efficiency variation was obtained from 10.3% to 12.3% for low H2 dilution of i-a-Si:H layer. Tsunomura et al. [35] has developed a 100.5 cm2HIT solar cell with a conversion efficiency of 22.3% (Voc: 0.725 V, Isc: 3.909 A, FF: 0.791) confirmed by National Institute of Advanced Industrial Science and Technology (AIST), Japan. The improvements in heterointerface properties and optical confinement in the layers have led to this higher efficiency. High quality intrinsic layer has been developed to reduce the tunneling and the interface recombination velocity in the back-surface field structure. Process parameters of the screen-printing and properties of silver paste were optimized to have fine and higher grid electrodes for the enhancement in the Isc and FF of the cell. High quality wide-gap alloys and TCO with high carrier mobility have reduced the absorption in the layers significantly. To reduce the power generating cost of such high efficiency cells, thinner HIT cell with over 70 mm c-Si was developed.

Hayashi et al. [36] has studied an n-c-Si/i-n-a-Si:H heterojunction cell using the current-voltage characteristics. The method of electrical measurements has been discussed for the back-side heterojunction of HIT cells. The variation in the Fermi level of n-c-Si had measured by a scanning Kelvin force microscope (KFM) at the heterointerface. It was shown that the n-cSi/i-n-aSi:H junction has an ohmic interconnection between the photovoltaic part of the solar cell and the back electrodes of the cell. The KFM measurements proved that the electrons have gathered in n-c-Si due to smaller conduction band near the back-side hetero-junction. As reported by Sakata et al. [37], further improvement of passivation capability of the interface had increased Voc upto 747 mV for very thin HIT solar cell. By increasing the Hall mobility of TCO by 1.3 times, efficiency have reached to 23.0 % from the previous value of 22.8% . The passivation capability of cell has enhanced Voc by lowering the surface recombination loss, while the higher Isc was achieved by reducing the optical absorption loss and refining the grid electrode.

Zhao et al. [38] has performed a comparative study of the surface passivation on c-Si wafers using a-Si:H thin films for different structures. These structures were characterized by Raman spectroscopy and Fourier transform infrared (FTIR) spectroscopy for investigation. Compared to the deposition of microcrystalline (mc-Si) silicon and nanocrystalline silicon (nc-Si), the passivation by the a-Si:H layers had provided higher carrier lifetimes because of the H content. It has been concluded that the passivation of c-Si surface was more effective by forming Si-H bonds rather than Si-H2 bonds. Lee et al. [39] has experimentally studied that the effect of H2 plasma treatment on the performance of HIT solar cells. The Voc was found increasing with the H2 treatment time, and started decreasing after 80 seconds, i.e. the optimum time is 80s for H2 treatment. The cell performance remained almost constant with and without a thin i-a-Si:H layer, when 80s plasma treatment is applied on the c-Si. Due to optimum H2 plasma treatment, a conversion efficiency of 14.04% was achieved for one of HIT cells.

Mishima et al. [40] has investigated the special technologies for the development of high-efficiency HIT solar cells at Sanyo Electric Co. Ltd. For thinner substrates, the standard HIT solar cell has shown a efficiency of 23.0% on a practical size of 100.4cm2 substrate. On a 98-mm-thick substrate, the Voc of 743 mV was found which produced a high conversion efficiency of 22.8%. This cell was having a good temperature coefficient <0.3%/°C, which means that more than 50% thickness of the substrate can be reduced, while maintaining the comparable efficiency. The performance of stability against temperature and use of thinner cell have validated the possibility of further reduction in the development cost of these cells. Wei and Lin [41] reported the application of the high-efficiency HIT solar-cell structure as photodetectors. The relationship between responsivities and thicknesses of active layers has been investigated along with the top i-a-Si:H and bulk c-Si. The desired detection wavelength is obtained by optimizing the thickness of a HIT photodetector. It was shown that the responsivities were 0.511, 0.529, and 0.641 A/W at 450, 650, and 850 nm wavelengths respectively, for a typical HIT structure with a 5-nm-thick top i-a-Si:H layer. In the year 2013, Panasonic Corporation announced the achievement of a record conversion efficiency of 24.7% at the research level, for HIT cell with 98 μm thickness over the area 101.8 cm2 beating their own record of 23.9% [42-43]. The same efficiency was reported by Sanyo Electric Co. Ltd. [44]. The core technologies developed for the reduction in recombination loss, optical and resistive loss, which have enhanced Voc, Jsc and fill factor, respectively to produce efficiency about 24%.

4. Discussions

Shah, Platz and Keppner [48] calculated the theoretical efficiency for solar cells made using individual semiconductor materials as shown in Fig.2. The measured efficiency ~26% of GaAs cell is highest and near to maximum theoretical efficiency of 28%. A great determination and continuous efforts led to the drastic improvements in efficiency more than 20% in HJ and HIT cells during the last decade. Fig. 3 and 4 represent the reported status of efficiencies for HJ and HIT cells at the laboratory stages, respectively.

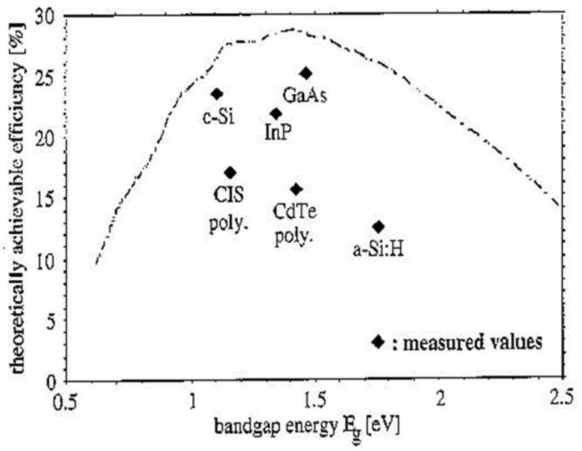


Fig.2. Maximum theoretical efficiency and individual efficiencies obtained for cells made by various semiconductors. Reprinted from Shah et al. [48].

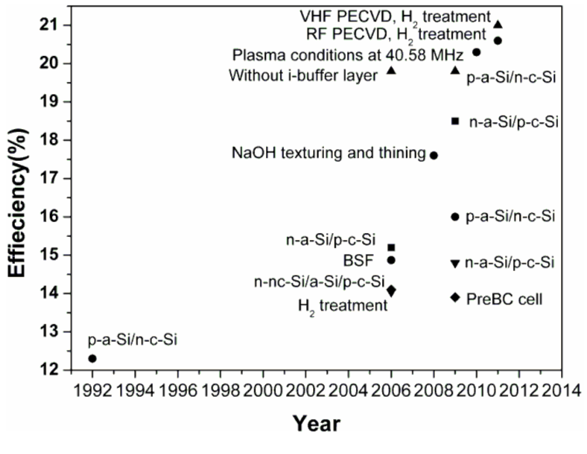


Fig.3. Yearwise progress in the efficiencies of heterojunction solar cells

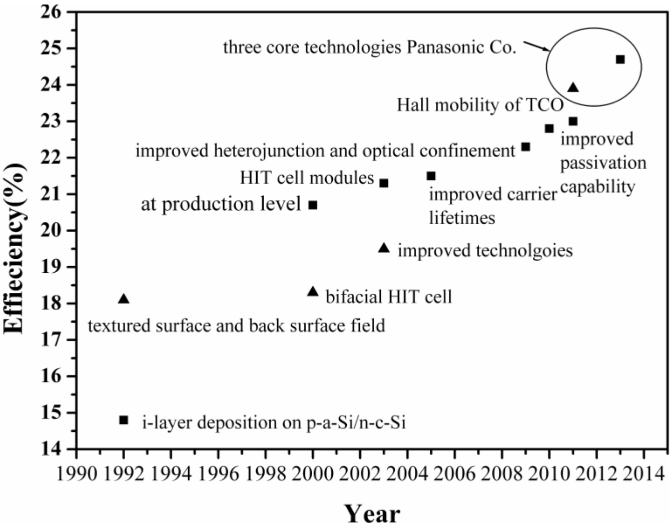


Fig.4. Yearwise progress in the efficiencies of HIT solar cells

We have classified the modifications in fabrication and characterization technologies for the efficiency improvements in HJ and HIT cells into three major categories. These categories are discussed in the following subsections:

4.1 Improvements through design and fabrication

1) Textured surfaces for optical confinement effect: Two methods namely- wet chemical etching and reactive ion etching are being used for texturing the surface of c-Si wafer [45].
2) Back surface field: It is created by depositing n+-type a-Si: H on the rear surface of c-Si substrate in HIT cells. This field reduces the activation energy of Si wafers [46]
3) Band gap engineering: Band gap engineering of i-a-Si: H layer is performed by altering the hydrogen content. This band gap controls the absorption of incident and backscattered photons into the c-Si substrate [46].
4) Creation of Internal electric field: Deposition of thin layer between p-a-Si: H and i-a-Si: H increases the internal electric field in the cell. This provides a thinner layer with high light trapping i-layer thickness, textured TCO and textured back reflector [46].
5) Microdoping: It is performed at the p/i and i/n interfaces by doping with a small amount of B- and P+ to compensate the light induced D+ and D- space charged [47].
6) Si-H bonding: Variations in Si-H bonding configurations for controlling the Si-H bonding in the cells.
7) Thermal and plasma based post treatments: To remove any impurity introduced during the deposition process and to improve the stability in the efficiency, such treatments are applied [17].

The effects of these improvements were observed by the real time spectroscopic ellipsometry (SE) and infrared attenuated total reflection (ATR) spectroscopy [16]. The results showed the wider band gap material like a-SiO: H reduces the epitaxial growth at high growth temperatures and low RF powers. Fermi level of n-c-Si is measured by a scanning Kelvin force microscope (KFM), which proved that electron have gathered near the back-side heterojunction due to smaller conduction band in n-c-Si [36].

4.2 Improvements through passivation and deposition

For the passivation on the surface of c-Si substrate, an i-layer of amorphous silicon was deposited over Si wafers before doped a-Si: H layer, which contributes in,

1) The reduction of dangling bonds: The charge trapping on the surface will become less.
2) The reduction of surface recombination (velocities): Additional charge carriers entered into the active layer c-Si.
3) The increase of minority carrier lifetime

Carrier lifetime is a measure of interface passivation and the recombination rates of electron-hole pair at the surface. Greater carrier lifetime contributes to increase the amount of current flow inside the cell and in the external circuit, which further enhances the efficiency.

Current-voltage characteristics (IV), photoluminescence (PL) and ultra violet photoelectron spectroscopy (UPS) were used to characterize passivation and deposition processes [28], which provide reduction in defect states density compared to n-a-Si: H layers. In addition, photoelectron yield spectroscopy (PEYS) [8], Raman spectroscopy, optical transmittance, activation energy of dark-conductivity [10] techniques were utilized. Different HIT cells are studied using Raman spectroscopy and Fourier transform infrared (FTIR) spectroscopy, whereas the lifetime measurements was carried out by the microwave photoconductive decay (µPCD) method [38]. To study the crystalline behaviour of a-Si: H thin films on n-type Si substrates, an effective medium approximation (EMA) method of a spectroscopic ellipsometer (SE) was used as in [23].

4.3. Improvement through the cleaning processes and carrier lifetime enhancements

The cleaning of c-Si substrates is performed,

1) To remove the crystalline silicon wafers from any surface impurity and oxides
2) To control the lattice dimension at the c-Si surface

These processes improve the quality of a-Si: H/c-Si interface and further reduce the recombination rate at the amorphous/crystalline silicon interface.

The effects of these processes have been studied by developing a physical model for HIT structure. The effective lifetime teff was measured by Quasi-state photoconductance technique [31]. In addition, the lifetimes were found in 1 ms range measured using an inductively coupled photoconductance bridge [13]. The impedance spectroscopy at forward bias and illumination conditions was able to detect the longer time constant t » 300 ms [15]. It provides that the electron capture time steeply rises with temperature, whereas the hole capture time slightly falling.

A low H2 dilution improves HIT cell properties specially the H2/SiH4 ratio of 2 and 4 due to passivation effect. An efficiency varied from 10.3% to 12.3% was found for low H2 dilution of i-a-Si: H layer [34]. Plasma pre-treatments provide the high effective lifetimes (teff »1.55 ms), lower surface recombination rate (≤ 9 cms-1) and high Voc (» 0.713 V) [21]. In pre-treatment, SiO2 was etched from c-Si wafer by means of H2–SiF4 plasmas. For the polished and textured n-type substrate, a hydrogen plasma treatment increased the lifetimes obtained upto 11.2 ms and 7.2 ms respectively. This treatment produces HIT cells with an efficiency of 20.6% and 21.0% using RF and VHF PECVD, respectively as in [24].

5. **Conclusion**

Establishment of core technologies and developments of analytical methods for layer and devices helped the progress in HJ and HIT cell performances. Since the initiation of research in these kind of cells, the efficiencies are almost twice over in comparison to the first reported values. Most of research activities in such cells have been focussed at the improvements at the layer depositions and contacts during the fabrication of cells. So, in this paper, the efforts were made to compile the major outcomes of fabrication methods, process parameters and characterization techniques in order to gather the reported performance of heterojunction silicon solar cells. The PECVD process is still a vital and favourite method for the development of high efficiency heterojunction and HIT solar cells due to its flexibility to generate various forms of materials from the amorphous to polycrystalline. The operating basic frequency remains 13.56 MHz in the developments, although other higher frequencies have equally investigated for the deposition of microcrystalline and nano crystalline silicon films on the glass and c-Si substrates. The studies performed by the researchers have shown that the deposition process, surface treatments of c-Si wafers and control on TCO properties play an important role in achieving the remarkable high efficiency solar cells.

In this section, we summarized the core technologies along with their aim and means of achievements. Further, new possibilities in these research areas have been explored.

5.1 Core technologies developed

A. Improving the a-Si: H/c-Si heterojunction:

Aim: high-quality intrinsic a-Si layers and excellent a-Si/c-Si interfaces for better passivation and lower recombination loss.

Process:

1) Use of a clean c-Si surface before a-Si deposition and textured substrate
2) Deposition of a high-quality intrinsic a-Si layer

3) Lower plasma and/or thermal damage to the c-Si surface during a-Si, TCO and conductive electrode fabrication

4) Reduction in i-a-Si: H layer without compromising VOC

B. Reducing the absorption in the a-Si: H and TCO layers:

Aim: For a higher ISC, the optical losses should be reduced in a-Si and TCO layers.

Process:

1) High-quality widegap alloys such as a-SiC

2) High-quality TCO with high carrier mobility to better the electrical conductivity and the optical transmittance.

C. Improving the grid electrode:

Aim: Aspect ratio of the grid electrode should be higher to minimize the resistance and shadow losses. Also the spreading area should be reduced to minimize the optical loss.

Process:

1) The viscosity and rheology of the silver paste to develop lower resistance material.

2) The process parameters in the screen-printing

The maximum reported efficiencies are now in the range of 22 - 24 % in the HJ and HIT cells, where these core technologies were gradually utilized [40-44]. Even at this stage of reported efficiency, the researchers are still continuing their journey to higher and higher efficiency, but at the reduced fabrication cost. So that, it will cater the large requirements of these high efficiency solar cells for the general public. Therefore, this scope is offering a new thrust in thin film silicon solar cells. We have divided the core research areas into the three categories.

5.2 Core research areas

A. Cell technologies

1) New cell concepts: Introduction of modified window layers and a unique combination of semiconductor materials can be introduced in the development of a novel kind of cell.

2) Cell developments: Increasing a stack of semiconductors or modifying the order of the depositions of various layers can be attributes to cost effective technology and increase the maximum absorption of photons in the cells.

3) Process technology: Control of process parameters in the fabrication of cells may led to more efficient cells at a lower cost. Also, further comparison of different fabrication technologies can be explored to develop cheaper cells.

B. Layer deposition improvements

At the present scenario, we still have a scope for the enhancements in the properties of TCO layers, interfaces and absorber layers in the cells.

C. Solar cell characterization and modelling

To utilize any new material as a photovoltaic material, its material properties can modelled as an equivalent solar cell and parameters. Also, with the development of large area cells in different compositions, one can establish compatible characterization tools and verify them by comparing with the standard cells.

The future R & D in these areas will definitely help in crossing the 25 % mark in HJ cell or may be reached beyond 28% in HIT cells, however, the technological cost will also increase. So now, the researchers are developing HIT solar cell technologies with the thin c-Si substrate to have a cell at the reduced material cost. In addition, the photovoltaic research activities are aiming the self-sustain indigenous and cost effectiveness in silicon-based heterojunction and HIT solar cells developed in future. At the same time, the researchers are now developing new fabrication facilities for large area solar cells and their characterization techniques to perform the fast analysis of such cells.

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