International Journal Of Renewable Energy Research, IJRER
A.Ibrahim, Vol.1, No3, pp.60-65 ,2011

Dark Current -Voltage Characteristics and Lock-in Thermography Techniques as Diagnostic Tools for Monocrystalline Silicon Solar Cells

Ali Ibrahim

Physics department, Faculty of Science, Tanta University, 31 527 Tanta, Egypt

Tel: 0020403344352 - Fax : 0020403404914

E-mail: ali_02us@yahoo.com

Received : 30.05.2011 Accepted : 01.07.2011

Abstract - In this paper, a highly sensitive lock-in thermography system has been used, enabling the detection of periodic surface temperature oscillations below 10 µK (r.m.s). Spatially resolved power loss images obtained by Lock-In Thermography (LIT) for a single crystalline silicon solar cell carried out. A significant difference is shown for the solar cell with shunts, while series resistance and charge carrier recombination cause only minor differences in the images. This system has been used to investigate edge leakage shunts currents in silicon solar cells of the construction $n^{+}pp^{++}$ PESC Passivated Emitter Solar Cell (silicon wafers doped with Boron) after 4000 hrs of thermal stress at 400 K. The dark I-V characteristics of the solar cell, as a diagnostic tool, are studied and analysed. A decrease of the electrical parameters of the solar cell has been obtained after thermal stress.

Keywords - Shunts defects, lock-in-thermography, dark I-V characteristics and silicon solar cells.

1. Introduction

Lock-in thermography has been established to be a reliable tool to locate shunts in all kinds of solar cells [1–3]. Solar cells always show degradation in their characteristic parameters (Voc, Isc, FF and efficiency) due to the defects introduced by multistep processing or material quality. Shunts are one of the loss mechanisms which are caused by defects [4, 5] . They are divided into two categories: volume and edge shunts. Volume shunts which account for 20% [6] of this loss mechanism are hard to remove without destroying the cell.

Shunts can heavily reduce the solar cell's conversion efficiency and decrease the module performance. The efficiency of a cell is affected because shunts reduce the Fill Factor (FF) and the Open Circuit Voltage (Voc). This effect becomes more dominant under low light conditions [4]**.** A low shunt resistance can lead to hot-spots in reverse biased cells, especially when the power dissipation occurs in a small area [5]. The long-term stability of solar cells is crucial for their success as a source of renewable energy. Encapsulated silicon solar cells/modules have shown stable performance over many years under outdoor conditions for most of their electrical parameters. Unencapsulated circuits and cells, however, show decreases in fill factor and open circuit voltage after accelerated stress testing, i.e. at high temperature ($85\,^{0}C$) and humidity (85%).The acceleration factor of this stress test relative to a field test is presently still unknown. It would be needed for reliable extrapolations of the module lifetime based on stress test results.

The aim of this work is to investigate analytically the effect of thermal stress (at 400K for a period of 4000 hrs) on the electrical parameters of a single crystalline silicon solar cell. In addition**,** the present research aims at studying the shunts in monocrystalline silicon solar cells n+pp++ PESC (Boron heavy doped silicon wafer) by using both the LIT technique and dark I-V characteristics.

This paper is organized as follows: section 1 discuses shunts in crystalline silicon solar cells. Section 2 includes the experiment set up. Results and its discussion is given in section 3 followed by the conclusion and the cited references.

1.1 Shunts in Crystalline Silicon Solar Cells

The dark forward current of a solar cell maybe increased due to shunts process. The material defects of the solar cell construction can cause this current increase or it can be a process of simulation. Material induced shunts can occur due to a high density of dislocations, voids or impurities as well as metal-decorated small angle grain boundaries, grow-in macroscopic inclusions and inversion layers crossing the wafer**.** Shunts can be created during processing by residues of the emitter at the cell edge, as a result of cracks and holes, by scratches and by aluminum particles at the cell surface. Schottky type shunts can also occur below grid lines. Shunts have already been found and identified in silicon screen printed crystalline solar cells by Lock-in Thermography [7**].** They differ in their I-V characteristic (linear/ohmic or non-linear) and physical origin. Generally, the infrared lock-in thermography not only allows one to image shunts very sensitively in all kinds of solar cells, but also measure dark currents flowing in certain regions of the cell quantitatively [8-12].

2. Experimental set up

The aim of the development of the new lock-in thermography system was to achieve detection sensitivity as high as possible during an acceptable measuring time. And the Lock-in thermography system is based on an LN_2-cooled 128x128 pixel InSb local plane array thermocamera AE 4128 (Amber), having a noise equivalent temperature difference in the order of 10 mK (NETD) at a frame rate of 217 Hz. The digital output of the camera is fed to a computer, where a two-phase (sin/cos) lock-in correlation procedure is performed with the incoming frames on-line during the measurement. Since at least four frames per lock-in period are necessary to perform the lock-in correlation, the maximum possible lock-in frequency of this system is 54 Hz. The computer delivers the lock-in reference signal, which is used to trigger the bias of the cell. After the measurement the computer storage contains the n-phase and the quadrature image, which can be converted into the amplitude and the phase- image of the surface temperature modulation. The noise level of the amplitude signal falls with (measuring time)$^{-1/2}$ and reaches an effective value of 10 μK after 1/2 hr measuring time for black surfaces [9]. Using a 25 mm focal length objective and a special microscope objective, together with different lens extender rings, any pixel resolution down to 5μm can be chosen. The description of the experimental set up was shown in Ref.7. For current - voltage characteristics a schematic diagram of the system used is discussed in Ref. [13].

3. Discussion of results

3.1 Dark forward I-V characteristics

The forward current consists of the components with exponential dependence on the junction voltage, Vj, across the Space Charge Region (SCR). Figure 1 shows a typical I-V characteristic. Such qualitative descriptions of a forward I-V characteristic of single cascade solar cells (SC) were studied; however, no quantitative consideration has been made. An analytical description of the shape of a I-V characteristic should take into account the voltage IR_s across the ohmic series resistance of the p-n structure, with the result that the voltage V measured exceeds the voltage across the SCR (Vj), i.e.,$V_j = V - IR_s$. Unity should be subtracted from each of the components to ensure zero current at zero voltage across the SCR.

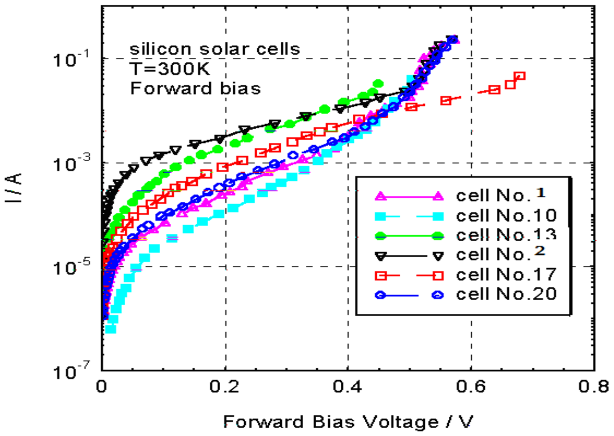


Fig. 1. I-V characteristics for monocrystalline Si solar cells $n^+ pp^{++}$ of area 100 cm^2 at room temperature in forward direction based on silicon wafer doped with Boron.

I-V measurements have been made using a computerized system for the silicon solar cells. Fig. 1 illustrates the current – voltage characteristics for a group of monocrystalline silicon solar cells, made from a silicon wafer. The two chosen cells among that under test are cells numbers 1 and 2 only. From the figure it is shown that cell 1 is better than cell 2, where cell 2 has an excess generation - recombination current. At forward voltage biasing of 0.2 V solar cell 1 has a current of about $5x10^{-4}$ A, while cell 2 has more an excess current of about $5x10^{-3}$A. Where for an ideal diodes (solar cells) the I-V characteristics does not account for carrier generation and recombination events in the depletion region. However, in practical solar cells, there are trap levels in the depletion region, which make such events possible. Carrier generation and recombination causes an excess current for both, forward and reverse bias. In the forward bias regime, the excess current is due to the recombination of minority carriers in the depletion region. This recombination current occurs only at low voltages and gives an ideality factor of 2.0. At higher voltages, the diffusion current dominates resulting in an ideality factor of 1.0. While in reverse bias regime, the excess current is due to the generation of carries in the depletion region. The generated carriers are driven by the electric field in the depletion region to the neutral regions. This generation current keeps increasing with the reverse voltage due to the increasing depletion width.

3.2 Shunt Characterizations

The shunt types that could be identified in 102x102 mm mono-crystalline silicon solar cells are described bellow: A cell with edge shunts is visualized in Figs. 2 and 3. Where a computerized system is used to identify these measurements. The effect of an edge shunt in the cell output will depend on the amount of emitter remaining on the cell edges and the affected area .The figures explain the lock-in thermograms of sections of a standard monocrystalline silicon solar cell (cell **1** and cell **2**). All images have been taken at a lock-in frequency of 3.4 Hz, applying a pulsed forward bias of 0.55 V in the dark. Bright contrasts indicate shunting activities. The dark spot at the bottom of all thermograms is due to the electrical contact attached to the samples. The cell thickness is about 300 µm. The section in Fig. 2 is a corner section with original cell edges at the top and the left hand side and laser scribed and cleaved edges at the right and the bottom. The sample additionally contains one vertical and one horizontal laser scribe at the back, both in the center of the area, which are not yet cleaved. The cutting depth of the vertical laser cuts was about 150 µm, but that of the horizontal ones was nearly the wafer thickness so that this cell was partly perforated at the horizontal cutting lines before cleavage.

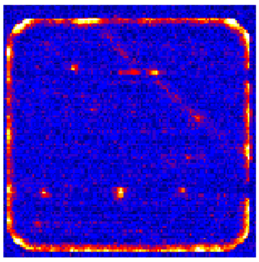


Fig. 2, Lock-in thermograms of a standard monocrystalline silicon solar cell of the construction $n^{+} pp^{++}$ PESC (cell **1**), at 0.55 forward biasing voltages.

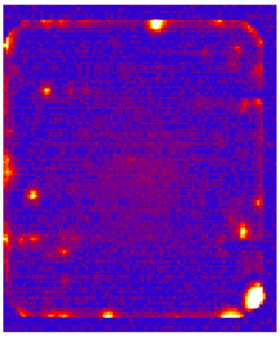


Fig. 3. Lock-in thermograms of a standard monocrystalline silicon solar cell of the construction $n^{+}pp^{++}$ (cell **2**) at room temperature, at forward biasing voltage of 0.55 V.

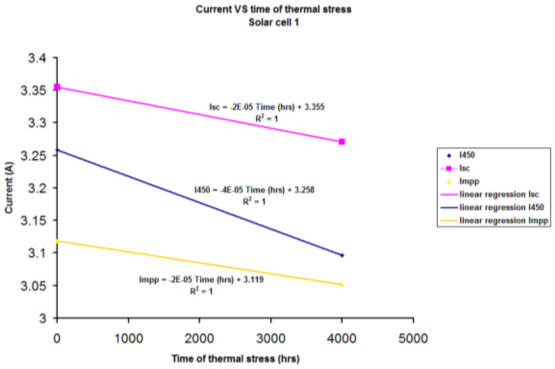
It is clear that cell No. **1** has shunts at the edges only while all cell area is clear and no shunts are existing. Fig. 2 and 3 show a lock-in thermogram measured at 0.55 V shown with extended contrast. These indicate to the fact that the dark forward current, which is reflected in the thermograms, is increased by the presence of recombinative crystal defects.

The efficiency of silicon solar cells (SC's) can be dramatically degraded by shunts which are usually localized at the edge area. These shunts are introduced during the different production steps of SC's. In shunt-free SC's the leakage current increases with temperature as would be expected for a p-n-junction, where by temperature stress for 4000 hrs (not continuous) at 400K increase the excess recombination current in SC's so the shunts along the whole cell area increases. For cell **1** it is clear that the efficiency, maximum power and fill factor decreased by 7.84%, 7.86 and 4.95% after thermal stress respectively. While that for cell **2** is 5.69%, 6.05% and 4.70% respectively.

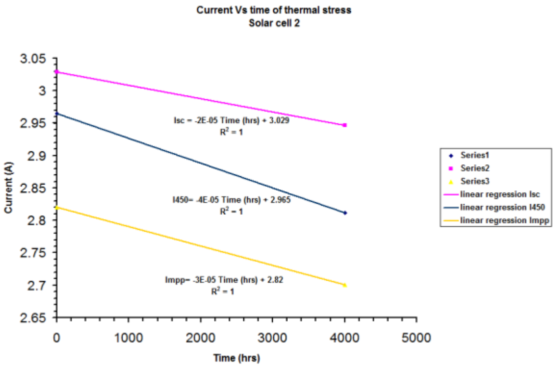
The correlation between the time of thermal stress and the solar cell electrical parameters are shown in Figures (4 –6) that illustrate the percentage of the decreasing in the solar cell electrical parameters after 4000 hrs of thermal stress at 400K. Moreover, not all electrical characteristics have the same trend of decreasing with time of thermal stress. The solar cells under study have been chosen among two groups of solar cells (good and bad ones)

3.3 Effect of thermal stress on the electrical parameters of solar cells

Thermal stress is performed on monocrystalline silicon solar cells to investigate their electrical parameters. Also, to determine the reliability attributes of terrestrial solar cells. Fig.4(a and b) shows the relation between Isc, I_{450}, and Impp for both silicon solar cells, No. 1 and No. 2 which represent the good and bad cells respectively, and the time of thermal stress. It is evident that the linear regression of the results shows the rate of decreasing of Isc, given by $2x10^{-5}$/hour of stress for both solar cells No. 1 and No.2. At the same time, nearly the same rate has been obtained for I_{450} and Impp.



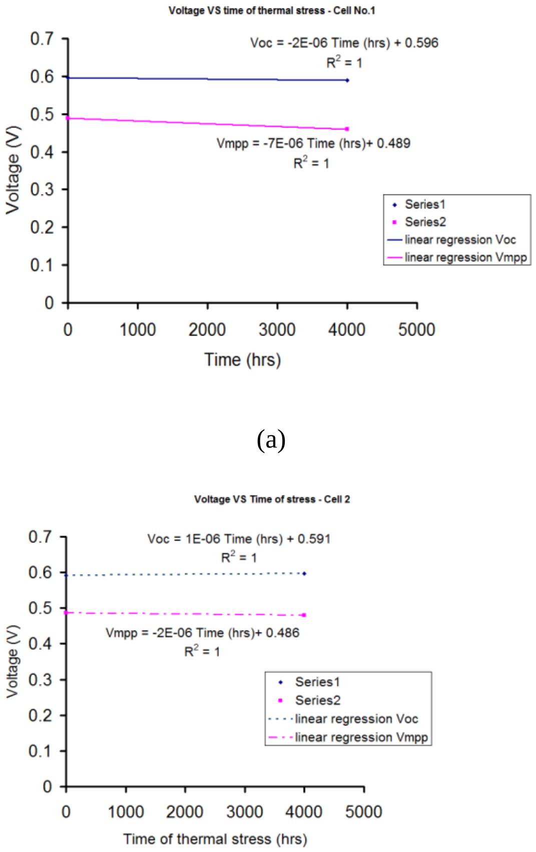
(a)



(a)

(b)

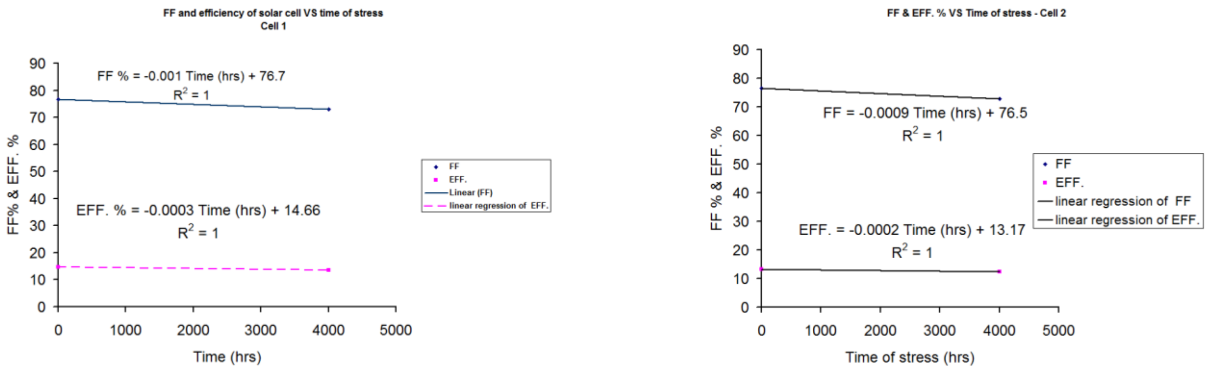
Fig. 4. Short circuit current Isc , current at 450 (I_{450}), and current at a maximum power point Impp with time of thermal stress for both (a) solar cell 1 and (b) silicon solar cell No.2.



(a)

(b)

Fig. 5. Open circuit voltage Voc and voltage at a maximum power point Vmpp with time of thermal stress for both: (a) solar cell 1, and (b) solar cell 2 .



(a) (b)

Fig. 6. Fill Factor FF and the efficiency EFF. with time of thermal stress for both: (a) solar cell 1, and (b) solar cell 2

On the other hand, from the cell voltage point of view, Fig. 5(a & b) show that both Voc and Vmpp for cells numbers 1 and 2 has the same rate of decreasing of nearly 10^{-6} /hour of thermal stress.

For both Fill Factor FF and the cell efficiency (EFF.) of both solar cells 1 and 2 Fig.6. (a & b) explain the obtained results. For solar cell fill factor (cells 1 and 2) the obtained rate of decreasing was 0.001 to 0.0009 /hour of stress respectively. But, for the cells efficiency (EFF.), the rate of decreasing was 0.0003/hour to 0.0002 /hour for cells 1 and 2 respectively.

4. Conclusion

The paper summaries that lock-in thermography allows one to perform a quantitative and qualitative analysis of the spatial distribution of the dark forward current density of solar cells. Thus it is possible to measure thermally the I-V characteristic of point shunts in a non destructive way of evaluation. Shunt analysis using single crystalline silicon solar cell enabled the effective detection of both process and material induced shunt. The causes of the shunts in a production line where identified. They could be reduced with improvements in cell handling, reduction of contaminations and process optimization. Shunt control and prevention resulted in a cell efficiency increase. Also, silicon solar cell electrical parameters, Isc, Voc, FF, and η will be affected by the time of thermal stress.

Acknowledgements

The author is greatly appreciated to thank Prof. O. Breitenstein {Max. Planck Institute for microstructure physics-(Halle-experimental physics II - Germany)}, especially for his help during lock-in- thermography measurements for the solar cells.

References

[1]G. Busse, D. Wu, W. Karpen, Thermal wave imaging with phase sensitive modulated thermography, *J. Appl. Phys.* 71 (1992) 3962-3965.

[2]O. Breitenstein, M. Langenkamp, Lock-in contact thermography investigation of lateral electronic inhomogeneities in semiconductor devices, *Sensors and Actuators A* 71 (1998) 46-50.

[3]O. Breitenstein , J. Heydenreich, Non-ideal I-V-characteristics of block-cast silicon solar cells, *Solid State Phenomena*, Vols. 37-38 (1994)139-144.

[4]O. Breitenstein, W. Warta, and M. Langenkamp, Lock-in thermography: Basics and use for evaluating electronic devices and materials, *1th ed., Springer*; Augest 2003.

[5]P. Grunow, S. Lust, D. Sauter, V. Hoffman, C. Beneking, B. Litzenburger, L. Podlowsk, "Weak light performance and annual yield of PV modules and systems as a result of the basic parameters set of industrial solar cells", *19th European Photovoltaic Solar Energy Conference* 2004, *Paris* , 2190-2193.

[6]M C. Alonso Garcia, W. Herrmann, W. Bömer, B. Proisy, Thermal and electrical effects caused by outdoor hot-spot testing in an associations of photovoltaic cells, *Prog. Photovoltaics: Research and Applications*, Vol. 11 (2003) 293–307.

[7]M. Langenkamp, O. Breitenstein, Classification of shunting mechanisms in crystalline silicon solar cells, *Solar Energy Materials & Solar Cells*, Vol. 72 (2002) 433-440.

[8]O. Breitenstein, J. P. Rakotoniaina, M.H. Al Rifai, M. Werner, Shunts types in crystalline silicon solar cells, *Progress in Photovoltaics: Research and Applications*, Vol. 12 (2004) 529-538.

[9]O. Breitenstein, M. Langenkamp, O. Lang, and A. Schirrmacher, Shunts due to laser scribing of solar cells evaluated by highly sensitive lock-in thermography, *11th International Photovoltaic Science and Engineering Conference (PVSEC-11)*, Sapporo, Japan (1999) Technical Digest, 285-286.

[10]O. Breitenstein, M. Langenkamp, Lock-in contact thermography investigation of lateral electronic inhomogeneities in semiconductor devices, *Sensors and Actuators* A 71 (1998) 46-50.

[11]J.P. Rakotoniaina, M.H. Al Rifai, O. Breitenstein, Quantitative analysis of the influence of shunts in solar cells by means of lock-in thermography, *Photovoltaic Energy Conversion 2003 Proceedings of 3rd World Conference* , Volume 2, Issue, 12-16 (2003) 1065 - 1068 .

[12]O. Breitenstein, M. Langenkamp, K.R. Mcintosh, C.B. Honsberg, and M. Rinio, Localization of shunts across the floating junction of DSBC solar cells by lock-in thermography, *29 th IEEE PVSC Conf. (2000*) 124-127.

[13]A. Ibrahim, Z. Chobola, "Invited paper” " Effect of illumination on 1/f noise and transport characteristics of a monocrystalline silicon solar cells,' *Proceedings of Seminar Noise 2000, Gdansk, Poland*, 2000, p.10.