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Electrical Characterization of CdO Based Au/p-Si Rectifier

Mehmet YILMAZ[1]*

ABSTRACT: Cadmium oxide (CdO) film was developed using a chemical spray pyrolysis technique on the p-type silicon (p-Si) substrate. The solution of the CdO was obtained by dissolving cadmium acetate salt in a mixture of distilled water and methanol. High-quality Au and Al contacts were evaporated on the polished and unpolished side of p-Si, respectively to create 4Au/CdO/p-Si/Al device architecture. In this context, four Au/CdO/p-Si/Al devices that were arbitrarily favored were analyzed and compared in depth. Current-Voltage (I-V) measurements were carried out to find out the performance of the CdO interlayer in the Au/p-Si device. The obtained data were analyzed using the Thermionic emission theory, Norde, and Cheung approach. Results indicated that CdO films grown by simple chemical spray pyrolysis technique could be used as barrier modifiers in Au/p-Si rectifier device.

Keywords: CdO, Spray pyrolysis, Schottky Junction, rectifier

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INTRODUCTION

In recent years, TCO films (such as ITO and SnO_2) have gained attention due to their low resistance and high transparency (Ferro, 1999). Besides, indium's recently included as critical raw material and it's being very expensive has forced researchers to work on materials alternative to ITO (Ylä-Mella et al., 2016). At this stage, the electrical resistance of the CdO film is between 10^{-2}–10^{-4} Ω.cm, and the optical band gap between 2.2 and 2.7 eV. These behaviors highlight the potential of CdO to be used as an alternative to ITO in device applications. Moreover, native defects such as oxygen vacancies and cadmium interstitials are responsible for the electrical conduction of pure CdO. Controllable of conductivity and optical properties of CdO films by controlling natural defects makes CdO films interesting in hetero-junction applications. Although these properties can be adjusted for the desired application with external effects such as doping, they can also be changed depending on the experimental method (Sankarasubramanian et al., 2015). In this context, depending on the growth method, the natural defect rates that affect the characteristics of CdO films can be changed by controlling some process parameters such as the concentration of the solution, the temperature of the substrate and the solution flow rate, the pressure of the growth condition (Gupta et al., 2008; Murthy et al., 1999).

According to the literature, the CdO films are obtained with many growth methods. Among them, pulsed laser deposition (Menazea et al., 2020), radiofrequency magnetron sputtering (Saha et al., 2008), metalorganic chemical vapor deposition (MOCVD) (Jin et al., 2004) are frequently used to obtain high-quality CdO films, which are suitable for many applications. However, these techniques require a lot of time to reach the desirable vacuum rate as well as being expensive can be thought the disadvantages of these techniques (Wang et al., 2018). Recently, the spray pyrolysis technique provides an easy way to obtain high-quality metal oxide-based thin films (Khodair et al., 2020; Mahesh et al., 2020). The chemical spray pyrolysis technique (CST), one of the important production methods, provides one-stage production and homogeneous particle composition. In CST, the primary preparation conditions affecting film properties are precursors and solvents (Afify et al., 2014). Therefore, it is important to investigate the performance of CdO films obtained by CST in device applications in order to reveal the performance of the CST.

This article examines the performance of the CdO thin film made by the solution-based CST in Au/p-Si device as an alternative to the CdO films growth by vacuum-requiring growth methods mentioned above. The obtained Au/CdO/p-Si/Al was characterized by current-voltage (I-V) analyses at room temperature.

MATERIALS AND METHODS

To obtain better performance, the p-Si wafer was firstly cleaned up by a cleaning procedure called the RCA (Kern, 1990). The Al contact (100 nm) was then vaporized to the unpolished side of the p-Si and thermally annealed at 500 ° C for 5 minutes for ohmic contact. A simple experimental setup was used to perform the deposition of CdO thin films by the CST. As source material, the cadmium acetate ($Cd(CH_3COO)_2 \cdot 2H_2O$) was preferred and it was dissolved in a mixture of deionized water and methanol (volumetric ratio of deionized water/methanol was adjusted as 1: 1). The final solution was sprayed onto the p-Si substrate at a flow rate of 2 mL/min at 250°C substrate temperature. The properties of the p-Si substrate were given in our previous publications (Turgut et al., 2021),. Finally, Au dot contacts were evaporated by thermal evaporation onto the CdO films to create Au/CdO/p-Si/Al device architecture. Electrical evaluations were made by taking into account the current-voltage (I-V) measurements obtained using the KEITHLEY 487 Picoammeter/Voltage Source and the results were discussed in detail.

RESULTS AND DISCUSSION

Semi-logarithmic I-V plots of the Au/p-Si/Al (reference) and Au/CdO/p-Si/Al device points have been given in Fig.1. According to the semi-logarithmic I-V curves of the samples, the fabricated devices exhibited strong rectifying properties, but the rectifying properties changed from device to device. Variations in I-V graphs can be due to metallic contacts or measurement errors as well as non-uniform interface layers, as we noted in our previous publication (Kocyigit et al., 2019).

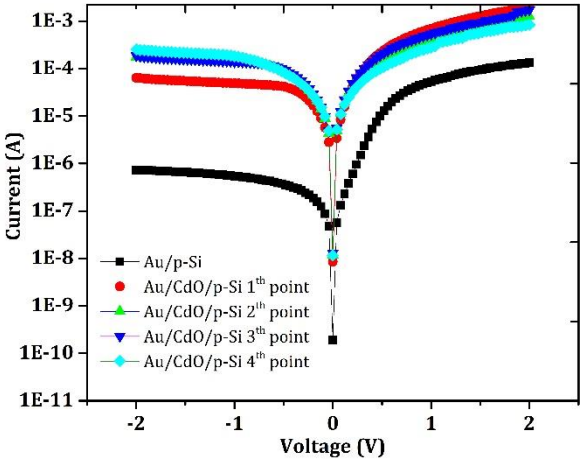

Fig.1. I-V plot of the various Au/p-Si/Al and Au/CdO/p-Si/Al device points

We performed I-V analysis considering the thermionic emission theory to obtain detailed information regarding the influence of layer inhomogeneity on the properties of Au/CdO/p-Si/Al device. In the presence of the interfacial layer of CdO, the correlations between current and voltage can be associated with Eq.(1), taking into account the thermionic emission (TE) principle (Karataş et al., 2003).

$$I = I_0[\exp\left({}^{qV}/_{nkT}\right) - 1] \quad (1)$$

where, I_0 is the current of saturation and given via the following formula:

$$I_0 = AA^*T^2\exp({}^{-q\varphi_b}/_{kT}) \quad (2)$$

Some of the notations seen in Eqs,(1-2) such as *q, T,* φ_b *V, k, A*, Rs, A,* and *n* are electron charge, temperature, height of the zero bias barrier, applied voltage, Boltzmann constant, Richardson constant (32 A/(cm^2.K^2) for p-Si), series resistance, diode area, and, ideality factor, respectively. If *V >3kT/q*, the ideality factor may be organized from eq.(1) as below (Karataş et al., 2007):

$$n = {}^{q}/_{kT}\left[{}^{dV}/_{d(lnI)}\right] \quad (3)$$

The meaning of the ideality factor "*n*" is unity for the ideal device according to simple TE theory.

However, variation from the unity is inevitable because of certain factors such as the presence of the oxide layer between the materials of the junctions and the decrease in IRs caused by the effect of series resistance R_s (Grilli et al., 2016). Also, this behavior is called a non-ideal diode feature. For the non-ideal diode, zero bias barrier height values can be calculated using Eq. (4):

$$\varphi_b = \frac{kT}{q}\ln({}^{AA^*T^2}/_{I_0}) \quad (4)$$

Table 1 provides the measured barrier height values and ideality factor obtained from the standard I-V approximation for the Au/p-Si/Al and Au/CdO/p-Si/Al device points.

Table 1. Comparing device points of Au/p-Si/Al and Au/CdO/p-Si/Al' s characteristics

Sample	Saturation Current (I_0)	n (TE)	φ_b (eV) (TE)	Cheung		Norde	
				n	φ_b (eV)	φ_b (eV)	R_s (kΩ)
Ref.	$7.80X10^{-8}$	7.73	0.68	8.12	0.63	0.71	1.29
1th point	$4.04X10^{-8}$	1.52	0.70	3.86	0.56	0.61	1.48
2 th point	$5.19x10^{-8}$	1.55	0.69	3.90	0.35	0.60	1.02
3 th point	$6.55x10^{-8}$	1.54	0.69	4.02	0.54	0.60	0.93
4 th point	$4.38x10^{-8}$	1.57	0.70	6.57	0.48	0.58	2.13

According to Table 1, it is seen that the values of the ideality factor for different device points are larger than the unity. This situation demonstrates that, as stated before, the fabricated devices exhibit non-ideal diode behavior. Besides, it has been found that the ideality factor's value of the reference sample is very high. In the literature (Gupta et al., 2009a, 2009b), a higher ideality factor is seen for devices with different device architectures, especially in calculations using data in the high forward bias area. The high ideality factor may be attributed to many factors, such as the rapid recombination of electrons and holes in the area of depletion, interface state density effect, and the presence of imperfections between metal/semiconductor interlayer (Akinn et al., 2019; Yeganeh et al., 2010). Moreover, a considerable decrease in the ideality factor has been observed with the use of CdO as the interface material in the Au/p-Si device. This situation can be shown as evidence that CdO affects the barrier height of conventional Au/p-Si contacts. As for the CdO/p-Si contact, the silicon and CdO electron affinities are 4.05 eV and 3.45 eV, respectively. Therefore, the Schottky barrier occurs at the CdO/p-Si junction (Bagal et al., 2016; Soylu et al., 2012). The values shown in Table 1 shows the correlation between the barrier height and the ideality factor. Hence, the barrier inhomogeneities can be seen with a slight difference with the change of diode points. The fact that all the φ_b values are similar to each other indicates the barrier height's homogeneous nature. Thus, the small inconsistency in the CdO diodes' barrier heights is thought to be because of the difference in the carrier concentration of CdO in the studied area because of CdO film is not homogeneously distributed on the surface.

An alternative way of calculating the diode parameters like the barrier height value of these types of devices is the Norde method. The following equation can be applied to compute the barrier height of four Au/CdO/p-Si devices (Lien et al., 1984):

$$F(V) = \frac{V}{\gamma} - \frac{kT}{q}\ln[\frac{I(V)}{AA^*T^2}] \quad (5)$$

where, γ indicates an integer that should be higher than the n defined by the TE, and the I(V) indicates bias based on current. The F (V)-V diagram of four Au/CdO/p-Si devices have been shown in Fig. 2 and Table 1 provides these curves' estimated parameters have been given. From the values shown in Table 1, it can be concluded that the obtained values of φ_b differ slightly from the values obtained from other methods. Series resistance is another significant parameter for similar devices. Therefore, calculating the series resistance is essential in determining the performance of such devices (Ocak et al., 2009).

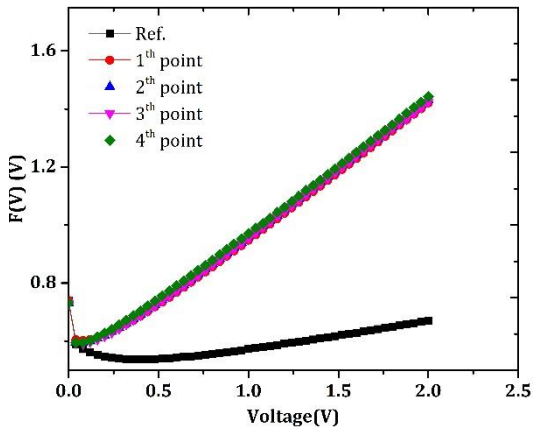

Fig.2. The Norde plot of the Au/p-Si/Al and Au/CdO/p-Si/Al device points

$$R_s = \frac{\gamma - n}{I}\left(\frac{kT}{q}\right) \quad (6)$$

The calculated series resistance values are given in Table 1, and values of k(Ω) order have been obtained with the differences for each diode point. As mentioned earlier, the observed difference in both barrier height and series resistance values may be due to measurement errors as well as to the CdO interface growing inhomogeneously on the p-Si wafer.

According to Cheung method, the current expression of diode can be represented as follows depending on R_s (Kocyigit et al., 2019; Singh et al., 2015).

$$I = I_0 exp\left(-\frac{q(V - IR_s)}{nkT}\right) \quad (7)$$

The IR_s is the drop at voltage because of the series resistance. Hence, diode parameters such as ideality factor and barrier height can be obtained using Cheung approximations under the effect of series resistance. For this, the equations known as Cheung approximations can be used.

$$\frac{dV}{d(lnI)} = \frac{nkT}{q} + IR_s \quad (8)$$

$$H(I) = V - \left(\frac{nkT}{q}\right)\ln\left(\frac{I}{AA^*T^2}\right) \quad (9)$$

$$H(I) = n\varphi_b + IR_s \quad (10)$$

By considering Eqs. (8-10), *dV/dln(I) vs.(I)* and *H(I) vs.(I)* curves can be drawn with a linear nature. In addition, some diode parameters such as series resistance, barrier height, and ideality factor are given by the slope and y-axis intercept of these curves. The *dV/dln(I) vs.(I)* and *H(I) vs.(I)* plots of the Au/p-Si/Al and Au/CdO/p-Si/Al device points have been shown in Fig. 3 and calculated diode parameters have been listed in Table 1. From the values given in Table 1, it is seen that the *n* and φ_b values obtained by the Cheung approach are not in good agreement with those derived from values of thermionic emission theory. Non-ideal device configurations may be correlated with discrepancies between n and φ_b values for the same device. (Yıldırım, 2019).

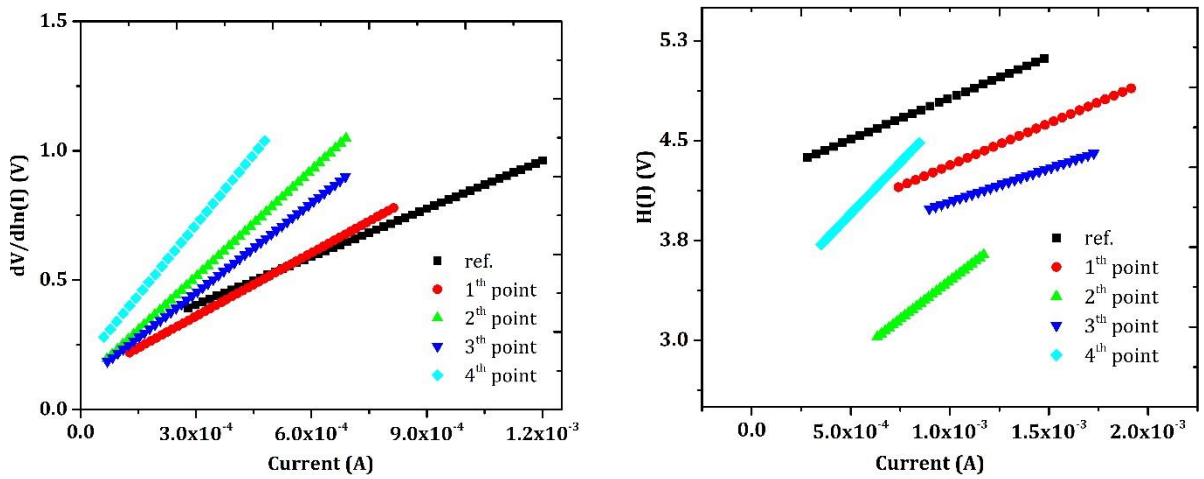

Fig.3. A plot of dV/dln(I) vs.(I) and H(I) vs.(I) of the Au/p-Si/Al and Au/CdO/p-Si/Al device points

Actually, this difference can be explained by taking differences in calculations into consideration. While the TE approach uses the data of the I-V plot in the linear region to measure the diode parameters, the Cheung method uses the data in the nonlinear region of the I-V curves where the interface states and R_s are efficient. Similar interpretations have been by other researchers to explain the differences between Norde, Cheung, and TE approximations (Sağlam et al., 2004; Tataroğlu et al., 2009; Yilmaz, 2019).

CONCLUSION

The CdO thin film was grown on the p-type Si by the CST. To examine the device performance of the CdO film in the Au/p-Si device, Au gold contacts were evaporated on the CdO film and the 4 Au/CdO/p-Si/Al device structure was completed. In this context, the device parameters of 4 Au/CdO/p-Si/Al devices were determined using different methods depending on I – V analysis and compared in terms of various device point effects. Accordingly, while the ideality factor varied between 1.52-1.57, the barrier height varied between 0.70-0.69 eV, indicating the homogeneous nature of the barrier height. The small differences here were attributed to the difference in carrier concentration of CdO in the device being studied because the CdO film is not homogeneously distributed over the p-Si backing.

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Conflict of Interest

I declare that there is no conflict of interest during the planning, execution and writing of the article.

Author's Contıibutions

I hereby declare that the planning, execution and writing of the article was done by me as the sole author of the article.

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